innodisk

The Total Solution For Industrial Flash Storage

iCF 1SE2

Standard

Customer: _____

Customer Part Number: _____

Innodisk Part Number: _____

Innodisk Model Name: _____

Date: _____

Innodisk Approver	Customer Approver

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REVISION HISTORY

Revision	Description	Date
Rev 1.0	First release version	March. 2014
Rev 1.1	Modify device parameter	June. 2014
Rev 1.2	Modify PN rule.	August. 2014
Rev 1.3	1. Add 128GB 2. Add E-mark certification 3. Add SAEJ1113 Report	September. 2014
Rev 1.4	Add Toshiba 15nm Flash support & performance Add TBW table	DEC. 2015
Rev 1.5	Edit Pin assignment	Aug. 2016
Rev 1.6	Revised Capacity	Dec. 2016
Rev 1.7	Updated CE/FCC certification (EN 55032)	Apr. 2017
Rev 1.8	Revised LBA info	Aug. 2017
Rev 1.9	Modify 15nm MLC Performance	July 2018
Rev 1.10	1. Remove 19nm MLC 2. Update RoHS / REACH / MSL	Mar. 2019
Rev 1.11	Add 1CH info. Remove appendix Revise storage temperature	Sep. 2021
Rev 1.12	Revise True IDE Mode I/O Decoding info.	Oct. 2021
Rev 1.13	Revise PN rule	Feb. 2022
Rev 1.14	Revise TBW	Sep. 2022
Rev 1.15	Update Mechanical Drawing Remove Write Protect Function	Oct., 2024
Rev 1.16	Update Mechanical Drawing	Mar., 2025

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1. Introduction

The Innodisk Industrial CompactFlash® 1SE2 Memory Card (iCF 1SE2) products provide high capacity solid-state flash memory that electrically complies with the True IDE Mode that is electrically compatible with an IDE disk drive. The original CF form factor card can be used in any system that has a CF slot. Designed to replace traditional rotating disk drives, Innodisk Industrial CompactFlash® 1SE2 Memory Cards are embedded solid-state data storage systems for mobile computing and the industrial work place. The Industrial CompactFlash® features an extremely lightweight, reliable, low-profile form factor. Industrial CompactFlash® 1SE2 (iCF 1SE2) support advanced PIO (0-6), Multiword DMA (0-4), Ultra DMA (0-7) transfer mode, multi-sector transfers, and LBA addressing.

2. Features

The Industrial ATA products provide the following system features:

- Capacities:
  - 512MB/1GB/2GB/4GB/8GB16GB/32GB/64GB
- Fully compatible with CompactFlash® specification version 6.0
- Fully compatible with PC Card Standard.
- Fully compatible with the IDE standard interface, ATA Standard
- Three access modes
  - True IDE Mode
  - PC Card Memory Mode
  - PC Card I/O Mode
- ECC (Error Correction Code) function: 72 bits/ per 1 Kbyte
- +3.3V/+5V single power supply operation
- Support Auto Stand-by and Sleep Mode.
- Power Consumption
  - Active mode
  - 5V:

    Read: 270mA(typ)

    Write : 280mA(typ)

    Idle : 165mA(typ)
- Support transfer modes: PIO(0-6), Multiword DMA (0-4) and Ultra DMA(0-7)

- R/W performance:

Table 1: Performance - 24nm SLC

Flash type	Capacity	Unit	Max. Read	Max. Write
24nm SLC	1GB(2CH)	MB/s	60	40
	2GB(2CH)		60	40
	4GB(2CH)		65	50
	8GB(2CH)		65	50
	16GB(2CH)		85	70
	32GB(2CH)		85	70
	64GB(2CH)		85	70
	512MB(1CH)	MB/s	30	20
	1GB(1CH)		30	20
	2GB(1CH)		35	25
	4GB(1CH)		35	30

- Operating temperature range:

  Standard Grade: 0°C ~ +70°C

  Industrial Grade: -40°C ~ +85°C

- Storage temperature range: -40°C ~ +85°C

3. Pin Assignment

See Table 1 for iCF 1SE2 pin assignments.

Table 2: iCF 1SE2 Pin Assignments

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	**Name**	**I/O**	**Pin No.**	**Name**	**I/O**	**Pin No.**	**Name**	**I/O**
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10[2]	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09[2]	I
11	A08	I	11	A08	I	11	A08[2]	I
12	A07	I	12	A07	I	12	A07[2]	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	I	14	A06[2]	I
15	A05	I	15	A05	I	15	A05[2]	I
16	A04	I	16	A04	I	16	A04[2]	I
17	A03	I	17	A03	I	17	A03[2]	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	-IOIS16	O	24	-IOCS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	O
27	D11[1]	I/O	27	D11[1]	I/O	27	D11[1]	I/O
28	D12[1]	I/O	28	D12[1]	I/O	28	D12[1]	I/O
29	D13[1]	I/O	29	D13[1]	I/O	29	D13[1]	I/O
30	D14[1]	I/O	30	D14[1]	I/O	30	D14[1]	I/O

31	D15[1]	I/O	31	D15[1]	I/O	31	D15[1]	I/O
32	-CE2[1]	I	32	-CE2[1]	I	32	-CS1[1]	I
33	-VS1	O	33	-VS1	O	33	-VS1	O
34	-IORD HSTROBE[10] HDMARDY[11]	I	34	-IORD HSTROBE[10] HDMARDY[11]	I	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I
35	-IOWR STOP[10,11]	I	35	-IOWR STOP[10,11]	I	35	-IOWR[7] STOP[8, 9]	I
36	-WE	I	36	-WE	I	36	-WE[3]	I
37	READY	O	37	-IREQ	O	37	INTRQ	O
38	VCC		38	VCC		38	VCC	
39	-CSEL[5]	I	39	-CSEL[5]	I	39	-CSEL	I
40	-VS2	O	40	-VS2	O	40	-VS2	O
41	RESET	I	41	RESET	I	41	-RESET	I
42	-WAIT -DDMARDY[10] DSTROBE[11]	O	42	-WAIT -DDMARDY[10] DSTROBE[11]	O	42	IORDY[7] -DDMARDY[8] DSTROBE[9]	O
43	-INPACK -DMARQ[12]	O	43	-INPACK -DMARQ[12]	O	43	DMARQ	O
44	-REG -DMACK[12]	I	44	-REG DMACK[12]	I	44	-DMACK[6]	I
45	BVD2	O	45	-SPKR	O	45	-DASP	I/O
46	BVD1	O	46	-STSCHG	O	46	-PDIAG	I/O
47	D08[1]	I/O	47	D08[1]	I/O	47	D08[1]	I/O
48	D09[1]	I/O	48	D09[1]	I/O	48	D09[1]	I/O
49	D10[1]	I/O	49	D10[1]	I/O	49	D10[1]	I/O
50	GND		50	GND		50	GND	

Note:

1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.

2) The signal should be grounded by the host.

3) The signal should be tied to VCC by the host.

4) The mode is optional for CF+ Cards, but required for CompactFlash Storage Cards.

5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.

6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal,

including a floating condition

7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.

8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.

9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.

10) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active.

11) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.

12) Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active.

13) Signal is a totem-pole output during Ultra DMA data bursts in True IDE mode.

4. Pin Description

Table 2 describes the pin descriptions for iCF 1SE2

Table 3: iCF 1SE2 Pin Description

Pin Name	Pin No.	I/O	Description
A10-A00 (PC Card Memory Mode) A10 – A00 (PC Card I/O Mode) A10 – A00 (PC Card I/O Mode)	8,10,11,12, 14,15,16,17, 18,19,20 18.19.20	I	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, only A[02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode) -STSCHG (PC Card I/O Mode) Status Changed -PDIAG (True IDE Mode)	46	I/O	This signal is asserted high, as BVD1 is not supported. This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode) -SPKR (PC Card I/O Mode)	45	I/O	This signal is asserted high, as BVD2 is not supported. This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.

-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode) -CD1, -CD2 (PC Card I/O Mode) -CD1, -CD2 (True IDE Mode)	26, 25	O	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket. This signal is the same for all modes. This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable -CE1, -CE2 (PC Card I/O Mode) Card Enable -CS0, -CS1 (True IDE Mode)	7, 32	I	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 30, Table 33, Table 35, Table 39, Table 41 and Table 42. While (-) DMACK is asserted, -CE1 and -CE2 shall be held negated and the width of the transfers shall be 16 bits. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode)	39	I	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode) D15 - D00 (PC Card I/O Mode)	2,3,4,5,631, 30,2928,27,4948,47,2322, 21	I/O	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. This signal is the same as the PC Card Memory Mode signal.

D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode) GND (PC Card I/O Mode) GND (True IDE Mode)	1, 50	-	Ground. This signal is the same for all modes. This signal is the same for all modes.
-INPACK (PC Card Memory Mode except Ultra DMA Protocol Active) -INPACK (PC Card I/O Mode except Ultra DMA Protocol Active) Input Acknowledge			This signal is not used in this mode. The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU. Hosts that support a single socket per interface logic, such as for Advanced Timing Modes and Ultra DMA operation may ignore the –INPACK signal from the device and manage their input buffers based solely on Card Enable signals.
-DMARQ (PC Card Memory Mode - Ultra DMA Protocol Active) -DMARQ (PC Card I/O Mode - Ultra DMA Protocol Active) DMARQ (True IDE Mode)	43	O	This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with (-)DMACK, i.e., the device shall wait until the host asserts (-)DMACK before negating (-)DMARQ, and re-asserting (-)DMARQ if there is more data to transfer. In PCMCIA I/O Mode, the -DMARQ shall be ignored by the host while the host is performing an I/O Read cycle to the device. The host shall not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1) and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits.

			If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode operation. A host that does not support DMA mode and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode except Ultra DMA Protocol Active) -IORD (PC Card I/O Mode except Ultra DMA Protocol Active) -IORD (True IDE Mode – Except Ultra DMA Protocol Active) -HDMARDY (All Modes - Ultra DMA Protocol DMA Read) HSTROBE (All Modes - Ultra DMA Protocol DMA Write)	34	I	This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface. In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer. In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (PC Card Memory Mode – Except Ultra DMA Protocol Active) -IOWR (PC Card I/O Mode – Except Ultra DMA Protocol Active) -IOWR (True IDE Mode – Except Ultra DMA Protocol Active)	35	I	This signal is not used in this mode. The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge). In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before

STOP (All Modes – Ultra DMA Protocol Active)			entering Ultra DMA mode protocol. In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.
-OE (PC Card Memory Mode) -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode)	9	I	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode) -IREQ (PC Card I/O Mode) INTRQ (True IDE Mode)	37	O	In Memory Mode, this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. I/O Operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.

-REG (PC Card Memory Mode – Except Ultra DMA Protocol Active) Attribute Memory Select -REG (PC Card I/O Mode – Except Ultra DMA Protocol Active) -DMACK (PC Card Memory Mode when Ultra DMA Protocol Active) DMACK (PC Card I/O Mode when Ultra DMA Protocol Active) -DMACK (True IDE Mode)	44	I	This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device. This is a DMA Acknowledge signal that is asserted by the host in response to (-)DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-)DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PC Card and True-IDE modes of operation need not alter the PC Card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode) RESET (PC Card I/O Mode) -RESET (True IDE Mode)	41	I	The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode)	13, 38	-	+5 V, +3.3 V power. This signal is the same for all modes. This signal is the same for all modes.

-VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode)	33, 40	O	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode – Except Ultra DMA Protocol Active) -WAIT (PC Card I/O Mode – Except Ultra DMA Protocol Active) IORDY (True IDE Mode – Except Ultra DMA Protocol Active) -DDMARDY (All Modes – Ultra DMA Write Protocol Active) DSTROBE (All Modes – Ultra DMA Read Protocol Active)	42	O	The -WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer. In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.
-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	36	I	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O	24	O	Memory Mode – The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation – When the CompactFlash Storage Card or CF+ Card is

Mode) -IOCS16 (True IDE Mode)			configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

5. Specifications

5.1 CE and FCC Compatibility

iCF 1SE2 conforms to CE and FCC requirements.

5.2 RoHS Compliance

iCF 1SE2 is fully compliant with RoHS directive.

5.3 Environmental Specifications

5.3.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade: 0°C to +70°C
- Industrial Grade: -40°C to +85°C

Storage Temperature Range: -40°C to +85°C

5.3.2 Humidity

Relative Humidity: 10-95%, non-condensing

5.3.3 Shock and Vibration

Table 4: Shock/Vibration Test for iCF 1SE2

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2 KHz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500G, 3 axes	IEC 68-2-27

5.3.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various iCF 1SE2 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF):** A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 5: iCF 1SE2 MTBF

Product	Condition	MTBF (Hours)
iCF 1SE2	Telcordia SR-332 GB, 25°C	>3,000,000

5.3.5 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the erase cycle limit or write endurance limit and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device. iCF 1SE2 uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

5.3.6 TBW

Parameter	Value
Read Cycles	Unlimited Read Cycles
Wear-Leveling Algorithm	Support
Bad Blocks Management	Support
Error Correct Code	Support
Thermal Sensor	Support
TBW*(Total Bytes Written)	Unit: TB
512MB	29
1GB	59
2GB	117
4GB	234
8GB	469
16GB	938
32GB	1875
64GB	3750
*Total bytes written is based on JEDEC 218. (Solid-State Drive Requirements and Endurance Test Method) **Lifespan is calculated by device written per day.	

5.3.7 Mechanical Dimensions

Mechanical Dimension: 42.80 x 36.40 x 3.30mm (W/T/H)

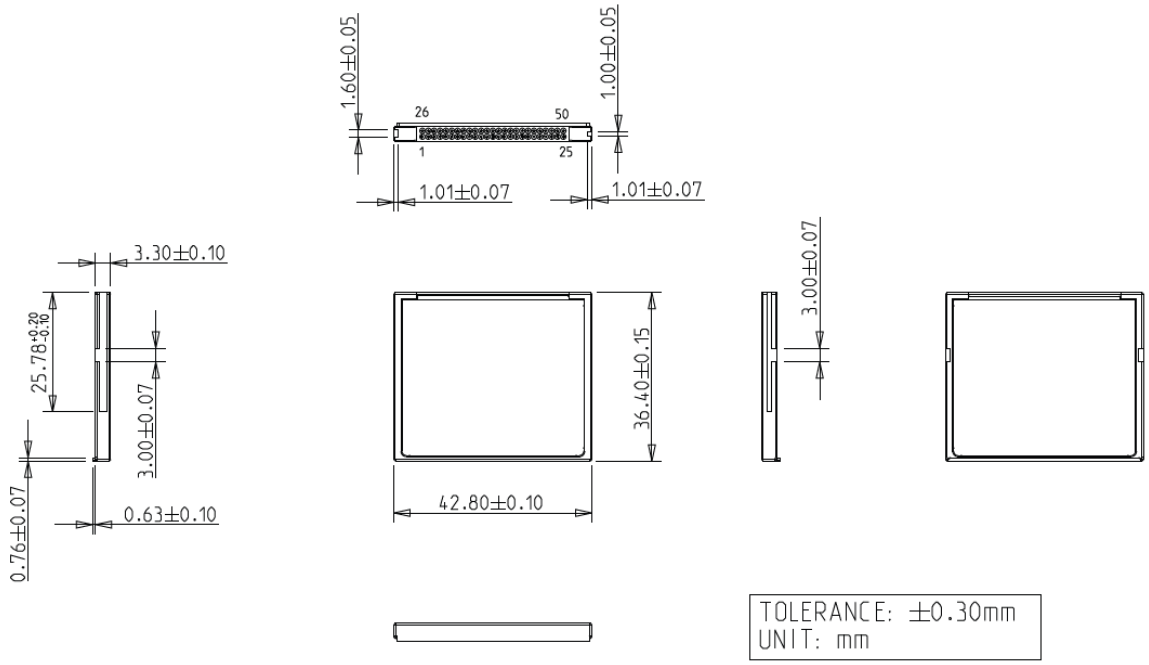

Figure 1: Mechanical Dimension of iCF 1SE2

5.4 Electrical Specifications

5.4.1 DC Characteristic

Power supply requirement: 5V±0.5V DC or 3.3±0.3V

5.4.2 Timing Specifications

5.4.2.1 True IDE PIO Mode Read/Write Timing Specification

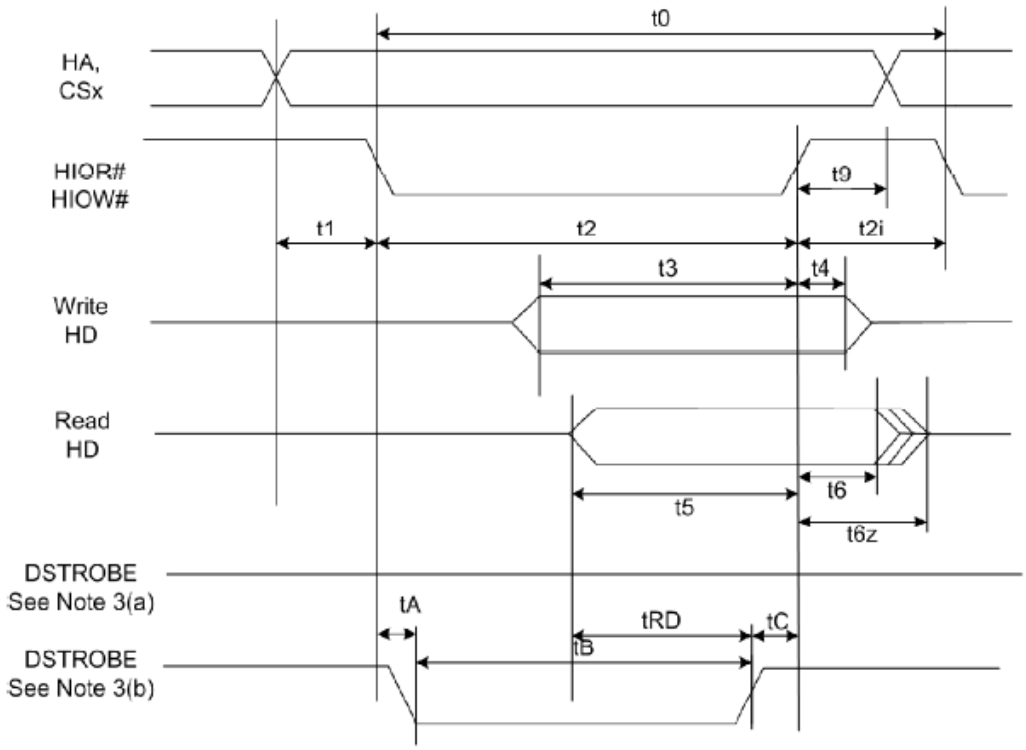

Figure 2: Read/Write Timing Diagram, PIO Mode

Note:

1. Device address comprises CS1#, CS0#, and HA[2:0].
2. Data comprises HD[15:0] (16-bit) or HD[7:0] (8-bit).
3. The negation of DSTROBE by the device is used to lengthen the PIO cycle. Whether the cycle is to be extended is determined by the host after Ta from the assertion of HIOR# or HIOW#. The assertion and negation of DSTROBE is described in the following three cases. (a) The device never negates DSTROBE: No wait is generated. (b) Device drives DSTROBE low before Ta: a wait is generated. The cycle is completed after DSTROBE is reasserted. For cycles in which a wait is generated and HIOR# is asserted, the device places read data on D15-D00 for Trd before DSTROBE is asserted.

Table 6: True IDE PIO Mode Read/Write Timing

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_0	Cycle time (min.)	600	383	240	180	120
t_1	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25
t_2	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70
t_2	HIOR-/HIOW- Register 8-bit (min.)	290	290	290	80	70
t_{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25
t_3	HIOW- data setup (min.)	60	45	30	30	20
t_4	HIOW- data hold (min.)	30	20	15	10	10
t_5	HIOR- data setup (min.)	50	35	20	20	20
t_6	HIOR- data hold (min.)	5	5	5	5	5
t_{6z}	HIOR- data tri-state (max.)	30	30	30	30	30
t_9	HIOR-/HIOW- to address valid hold	20	15	10	10	10
t_{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0
t_A	IORDY setup time	35	35	35	35	35
t_B	IORDY pulse width (max.)	1250	1250	1250	1250	1250
t_C	IORDY assertion to release (max.)	5	5	5	5	5

5.4.2.2 True IDE Multiword DMA Mode Read/Write Timing Specification

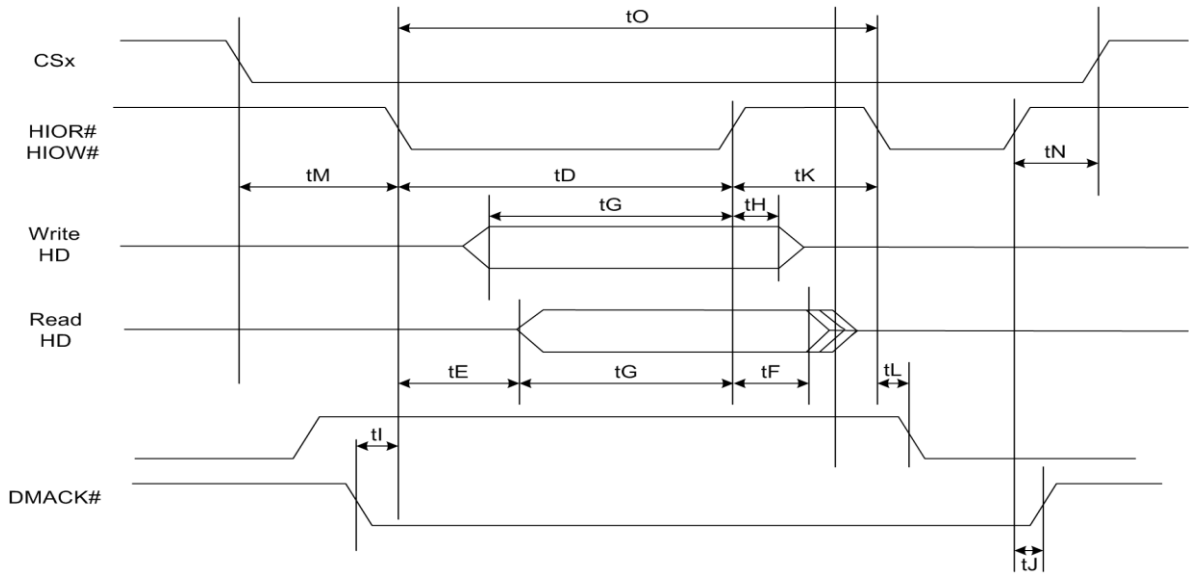

Figure 3: True IDE Multiword DMA Mode Read/Write Timing

Note:

1. If a card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ during the time from the start of a DMA transfer cycle (to suspend DMA transfers in progress) and reassertion of the signal at a relatively later time to continue DMA transfer operations.
2. The host may negate this signal to suspend the DMA transfer in progress.

Table 7: True IDE Multiword DMA Read/Write Timing

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2
t_0	Cycle time (min.)	480	150	120
t_D	HIOR-/HIOW- assertion width (min.)	215	80	70
t_E	HIOR- data access (max.)	150	60	50
t_F	HIOR- data hold (min.)	5	5	5
t_G	HIOR-/HIOW- data setup (min.)	100	30	20
t_H	HIOW- data hold (min.)	20	15	10
t_I	DMACK to HIOR-/HIOW- setup (min.)	0	0	0
t_J	HIOR-/HIOW- to DMACK hold (min.)	20	5	5
t_{KR}	HIOR- negated width (min.)	50	50	25
t_{KW}	HIOW- negated width (min.)	215	50	25
t_{LR}	HIOR- to DMARQ delay (max.)	120	40	35
t_{LW}	HIOW- to DMARQ delay (max.)	40	40	35
t_M	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25
t_N	CS1-, CS0- hold	15	10	10

5.4.2.3 True IDE Ultra DMA Mode Data Burst Timing Specification

Table 8: Timing Diagram, Ultra DMA Mode 0-6

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Mode 6	
		Min.	Max.	Min.	Max.	Min.	Min.	Max.	Min.	Max.	Max.	Max.	Min.	Max.	Max.
t_{2CYC}	Typical sustained average two cycle time	240	-	160	-	90	-	60	-	60	-	40	-	30	-
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to	112	-	73	-	39	-	25	-	25	-	16.8	-	13	-

	STROBE edge)														
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	153	-	86	-	57	-	57	-	38	-	29	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	5	-	5	-	4	-	2.6	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-	4.6	-	3.5	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	20	-	6.7	-	6.7	-	4.8	-	4	-
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-	4.8	-	4	-
t_{LI}	Limited interlock time	0	150	0	150	0	100	0	100	0	100	0	75	0	60
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-	20	-	20	-
t_{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10	-	10	-	10
t_{ZAH}	Minimum delay time required for output drivers to assert or negate (from released state)	20	-	20	-	20	-	20	-	20	-	20	-	20	-
t_{ZAD}		0	-	0	-	0	-	0	-	0	-	0	-	0	-
t_{ENV}	Envelope time (from	20	70	20	70	20	55	20	55	20	55	20	50	20	50

	DMACK- to STOP and HDMARDY- during data out burst initiation)														
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	70	-	60	-	60	-	60	-	50	-	50
t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-	85	-	85	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	50	-	50	-	50	-	50	-
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	230	-	200	-	130	-	120	-	120	-	90	-	80

5.5 Transfer Function

5.5.1 True IDE Mode I/O Transfer Function

The iCF 1SE2 can be configured in a True IDE Mode of operation. The iCF 1SE2 is configured in this mode only when –OE input signal is grounded by the host during the power off to power on cycle.

Table 9: True IDE Mode I/O Function

Function Code	-CS1	-CS0	-A0~A2	-DMACK	-IORD	-IOWR	D15~D8	D7~D0
Invalid Mode	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined In	Undefined In
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data In
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte In	Even-Byte In
Ultra DMA Data Register Write	H	H	X	L	See Note 1		Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	X	L	See Note 2		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address	L	H	7h	H	L	H	High Z	Data Out

Note1: In Ultra DMA Data Register Write mode the signals –IORD, -IOWR and IORDY are

redefined and used as follows: -IORD as HSTROBE, -IOWR as STOP and IORDY as –DDMARDY. Data transfers with each edge of HSTROBE.

Note2: In Ultra DMA Data Register Read mode the signals –IORD, -IOWR and IORDY are redefined and used as follows: -IORD as –HDMARDY H, -IOWR as STOP and IORDY as DSTROBE. Data transfer with each edge of DSTROBE.

5.6 Configuration Register

5.6.1 Configuration Option Register (200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the iCF 1SE2.

Table 10: Configuration Option Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevelREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Table 11: Information for Configuration Option Register

Name	Description
SRSET	Soft Reset: Setting this bit to one (1), waiting the minimum reset time and returning to zero(0) places the iCF 1SE2 in the reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the iCF 1SE2 in the same un-configured, Reset state as following power-up and hardware reset. Contrast with Soft Reset in the Device Control Register.
LevelREQ	This bit is set to one (1) then Level Mode Interrupt is selected, and zero (0) then Pulse Mode is selected. Set to zero (0) by Reset.
Conf5-0	Configuration Index: Set to zero (0) by reset. It is used to select operation mode of the iCF 1SE2 as shown below

Note: Conf5 and Conf4 are reserved for CompactFlash Storage cards and shall be written as zero(0).

5.6.2 Pin Replacement register (204h in Attribute Memory)

Table 12: Pin Replacement Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	Cready	0	1	1	Rready	0
Write	0	0	Cready	0	0	0	Mready	0

Table 13: Information for Pin Replacement Register

Name	Description
Cready	This bit is set to one (1) when the bit Rready changes state. This bit can also be written by the host.
Rready	This bit is used to determine the internal state of the READY signal. This bit may be used to determine the state of the READY signal as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask (Mready) for writing the corresponding bit Cready.
Mready	This bit acts as a mask for writing corresponding bit Cready.

5.6.3 Socket and Copy Register (206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register. This register is used for identification of the card from the other card.

Table 14: Socket and Copy Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	0	Obsolete (Drive #)	0	0	0	0
Write	0	0	0	Obsolete (Drive #)	X	X	X	X

Table 15: Information for Socket and Copy Register

Name	Description
Obsolete(Drive #)	This bit is obsolete and should be written as 0.

5.7 Software Interface

5.7.1 True IDE Mode Addressing

When the iCF 1SE2 is configured in the True IDE mode, the I/O decoding is as follows:

Table 16: True IDE Mode I/O Decoding

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0	Note
1	0	0	0	0	1	PIO RD Data	PIO WR Data	8 or 16 bit
1	1	X	X	X	0	DMA RD Data	DMA WR Data	16 bit
1	0	0	0	1	1	Error Register	Features	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select Card/Head	Select Card/Head	8 bit
1	0	1	1	1	1	Status	Command	8 bit
0	1	1	1	0	1	Alt Status	Device Control	8 bit

5.7.2 CF-ATA Register

The following section describes the hardware registers used by the host software to issue commands to the iCF 1SE2.

Note:

In True IDE Mode of operation, the size of the transfer is based solely on the register being addressed. All registers are 8 bit only except for the Data Register, which is normally 16 bits, but can be programmed to use 8 bit transfers for Non-DMA operations through the use of the Set Features command. The data register is also 8 bits during a portion of the Read Long and Write Long commands, which exist solely for historical reasons and should not be used.

5.7.2.1 Data Register

The Data Register is a 16 bit register, and it is used to transfer data blocks between the card and the host. This register overlaps the Error Register. This register can be accessed in word and byte mode.

Table 17: Data Register

Data Register															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

5.7.2.2 Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows.

Table 18: Error Register

BBK	UNC	0	IDNF	0	ABRT	0	AMNF
D7	D6	D5	D4	D3	D2	D1	D0

5.7.2.3 Feature Register

This register provides information regarding features of the card that the host can utilize. This register is also accessed in PC Card modes on data D15-D8 during a write operation to Offset 0 with –CE2 low and –CE1 high.

Table 19: Feature Register

Feature Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.7.2.4 Sector Count Register

This registers the number of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

Table 20: Sector Count Register

Sector Count Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.7.2.5 Sector Number Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for iCF 1SE2 data access for the subsequent command.

Table 21: Sector Number Register

Sector Number Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.7.2.6 Cylinder Low Register

This Register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

Table 22: Cylinder Low Register

Cylinder Low Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.7.2.7 Cylinder High Register

This Register contains the high order 8 bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

Table 23: Cylinder High Register

Cylinder High Register							
D7	D6	D5	D4	D3	D2	D1	D0

5.7.2.8 Device/Head Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing.

Table 24: Device/Head Register

1	LBA	1	DRV	HS3	HS2	HS1	HS0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is set 1.

Bit6: LBA is a flag to select either Cylinder/Head/Sector or Logical Block Address mode. When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected.

Bit5: this bit is set 1.

Bit4: DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected.

Bit3: When operation in the Cylinder/Head/Sector mode, this is bit 3 of the head number. It is bit 27 in the Logical Block Address mode.

Bit2: When operation in the Cylinder/Head/Sector mode, this is bit 2 of the head number. It is bit 26 in the Logical Block Address mode.

Bit1: When operation in the Cylinder/Head/Sector mode, this is bit 1 of the head number. It is bit 25 in the Logical Block Address mode.

Bit0: When operation in the Cylinder/Head/Sector mode, this is bit 0 of the head number. It is bit 24 in the Logical Block Address mode.

5.7.2.9 Status Register

These registers return the iCF 1SE2 status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not.

Table 25: Status Register

BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: the busy bit is set when the iCF 1SE2 has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit set to a 1.

Bit6: RDY indicates whether the device is capable of performing iCF 1SE2 operations. This bit is cleared at power up and remains cleared until the card is ready to accept a command.

Bit5: This bit, if set, indicates a write fault has occurred.

Bit4: This bit is set when the iCF 1SE2 is ready.

Bit3: The Data Request is set when the iCF 1SE2 requires that information be transferred either to or from the host through the Data register.

During the data transfer of DMA commands, the card shall not asserted DMARD unless either the BUST bit, the DRQ, or both are set to one.

Bit2: This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit1: This bit is always to 0.

Bit0: This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information description the error.

5.7.2.10 Device Control Register

This register is used to control the iCF 1SE2 interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY.

Table 26: Device Control Register

X	X	X	X	X	SW Rst	-Ien	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7-3: These bits are ignored.

Bit2: This bit is set to 1 in order to force the iCF 1SE2 to perform a Soft Reset operation. The Card remains in Reset until this bit is reset to '0'.

Bit1: the Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupt from the iCF 1SE2 are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.

Bit0: This bit is ignored.

5.7.2.11 Drive Address Register

This register is provide for compatibility with the AT disk drive interface.

Table 27: Drive Address Register

X	-WTG	-HS3	-HS2	-HS1	-HS0	-Nds1	-Nds0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is unknown.

Bit6: this bit is – when a write operation is in progress; otherwise, it is 1.

Bit5: this bit is the negation of bit 3 in the Drive/Head register.

Bit4: this bit is the negation of bit 2 in the Drive/Head register.

Bit3: this bit is the negation of bit 1 in the Drive/Head register.

Bit2: this bit is the negation of bit 0 in the Drive/Head register.

Bit1: this bit is 0 when drive 1 is active and selected.

Bit0: this bit is 0 when the drive 0 is active and selected.

5.8 Hardware Reset

Table 28: Timing Diagram, Hardware Reset

	Item	Min.	Max.	Normal	Unit
t_{SU}(RESET)	Reset Setup Time	20	-	-	ms
t_{REC}(VCC)	-CE Recover Time	1	-	-	us
t_{PR}	VCC rising up time	0.1	100	-	ms
t_{PF}	VCC falling down time	3	300	-	ms
t_{W}(RESET)	Reset pulse width	10	-	-	ms
t_{H}(Hi-ZRESET)		0	-	-	
t_{S}(Hi-ZRESET)		0	-	-	

5.9 Power on Reset

When the VCC power reaches to 2.7V, the disk drive will be reset.

Table 29: Timing Diagram, Power On Reset

	Item	Min.	Max.	Normal	Unit	Note
t_{SU}(RESET)	-CE Setup Time	20	-	-	ms	
t_{PR}	-VCC Rising Up Time	0.1	100	-	ms	

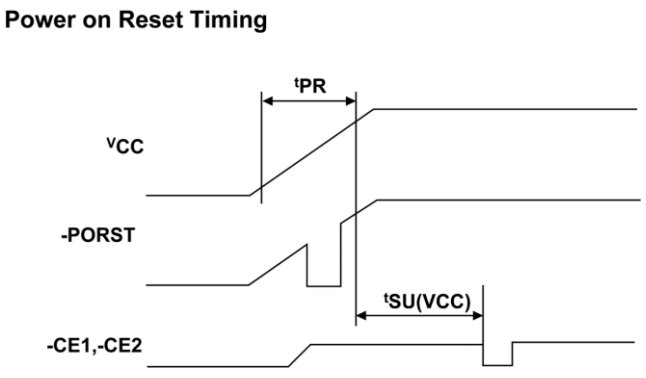

Figure 4: Timing Diagram, Power On Reset

5.10 Support IDE Commands

iCF 1SE2 supports the commands listed in Table 29.

Table 30: IDE Commands

Command	Code	FR	SC	SN	CY	DH	LBA
Check Power Mode	E5H	-	-	-	-	D	-
Execute Device Diagnostic	90H	-	-	-	-	D	-
Flush Cache	E7H	-	-	-	-	Y	-
Identify Device	ECH	-	-	-	-	D	-
Idle	E3H	-	Y	-	-	D	-
Idle immediate	E1H	-	-	-	-	D	-
Read Buffer	E4H	-	-	-	-	D	-
Read DMA	C8H	-	Y	Y	Y	Y	Y
Read Sector(s)	20H	-	Y	Y	Y	Y	Y
Read Verify Sector(s)	40H	-	Y	Y	Y	Y	Y
Set Features	EFH	Y	-	-	-	D	-
Set Multiple Mode	C6H	-	Y	-	-	D	-
Set Sleep Mode	E6H	-	-	-	-	D	-
SMART	B0h	Y	-	-	Y	Y	-
Standby	E2H	-	-	-	-	D	-
Standby Immediate	E0H	-	-	-	-	D	-
Write Buffer	E8H	-	-	-	-	D	-
Write DMA	CAH	-	Y	Y	Y	Y	Y
Write Multiple	C5h	-	Y	Y	Y	Y	Y
Write Sector(s)	30H	-	Y	Y	Y	Y	Y

Defines:

FR: Feature Register

SC: Sector Count Register

SN: Sector Number Register

CY: Cylinder Registers

DH: Card/Device/Head Register

LBA: LBA Block Address Mode Supported

Y: The register contains a valid parameter for this command. For Card/Device/Head Register Y means both the CompactFlash Storage Card and head parameter are used; D – only the CompactFlash Storage Card parameter is valid and not the head parameter; C – The register contains command specific data (see command description for use).

5.10.1 Check power mode -E5h

Table 31: Check power mode information

Register	7	6	5	4	3	2	1	0
Command(7)	E5h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command checks the power mode. If the CompactFlash Storage is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the 38ompactFlash Storage Card is in idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

5.10.2 Execute Device Diagnostic - 90h

Table 32: Execute device diagnostic information

Register	7	6	5	4	3	2	1	0
Command(7)	90h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card. When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices. The Diagnostic codes are shown in Table 34. Diagnostic Codes are returned in the Error Register at the end of the command.

Table 33: Diagnostic

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controller Microprocessor Error
8Xh	Slave Error in True IDE Mode

5.10.3 Flush Cache- E7h

5.10.3.1 Command Code

E7h

5.10.3.2 Protocol

Non-data

5.10.3.3 Inputs

Table 34: Flush cache command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E7h							

Device register–

DEV shall specify the selected device.

5.10.3.4 Normal Output

Table 35: Flush cache command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register-

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.10.3.5 Error Outputs

Table 36: Flush cache command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

5.10.3.6 LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register-

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.10.3.7 Prerequisites

DRDY will be set to one.

5.10.3.8 Description

This command is used by the host to request the device to flush the write cache. If there is data in write cache, that data shall be written to the SSD. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

5.10.4 Identify Device- Ech

Table 37: Identify device information

Register	7	6	5	4	3	2	1	0
Command(7)	Ech							
C/D/H(6)	X	X	X	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 35. All reserved bits or words are zero. Hosts should not depend in Obsolete words in Identify Device containing 0. Table 35 specifies each filed in the data returned by the Identify Device Command. In Table 35, X indicates a numeric nibble vale specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Table 38: IDENTIFY DEVICE information

Word	Description	Value
0	General configuration bit-significant information: 15 0 = ATA device 14-8 Retired 7 1 = removable media device 6 Obsolete 5-3 Retired 2 Response incomplete 1 Retired 0 Reserved	044Ah
1	Obsolete	XXXXh
2	Specific configuration	0000h
3	Obsolete	00XXh
4-5	Retired	XXXXh
6	Obsolete	XXXXh
7-8	Reserved for assignment by the CompactFlash™ Association	XXXXh

9	Retired	0000h
10-19	Serial number (20 ASCII characters)	20 ASCII characters
20-21	Retired	0002h
22	Obsolete	0004h
23-26	Firmware revision (8 ASCII characters)	8 ASCII characters
27-46	Model number (40 ASCII characters)	40 ASCII characters
47	15-8 80h 7-0 00h = Reserved 01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands	8001h
48	Reserved	0000h
49	Capabilities 15-14 Reserved for the IDENTIFY PACKET DEVICE command. 13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command. 11 1 = IORDY supported 0 = IORDY may be supported 10 1 = IORDY may be disabled 9 1 = LBA supported 8 1 = DMA supported. 7-0 Retired	0F00h
50	Capabilities 15 Shell be cleared to zero 14: Shall be set to one 13-2 Reserved 1 Obsolete 0 Shall be set to one to indicate a device specific Standby timer value minimum.	0000h
51	Obsolete	0200h
52	Obsolete	0000h
53	15-3 Reserved 2 1 = the fields reported in word 88 are valid Reserved 0 = the fields reported in word 88 are not valid	0007h

	1 1 = the fields reported in words (70:64) are valid 0 = the fields reported in words (70:64) are not valid 0 Obsolete	
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
59	15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command	01XXh
60-61	Total number of user addressable sectors	XXXXXXXXh
62	Obsolete	0000h
63	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected 9 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 8 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected 7-3 Reserved 2 1 = Multiword DMA mode 2 and below are supported 1 1 = Multiword DMA mode 1 and below are supported 0 1 = Multiword DMA mode 0 is supported	XX07h
64	15-8 Reserved 7-0 PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time 15-0 Cycle time in nanoseconds	0078h
67	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds	0078h
68	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds	0078h
69-70	Reserved (for future command overlap and queuing)	0000h
71-74	Reserved for the IDENTIFY PACKET DEVICE command.	0000h
75	Queue depth	0000h

	15-5 Reserved 4-0 Maximum queue depth - 1	
76-79	Reserved for Serial ATA	0000h 0000h 0000h 0000h
80	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA/ATAPI-14 13 Reserved for ATA/ATAPI-13 12 Reserved for ATA/ATAPI-12 11 Reserved for ATA/ATAPI-11 10 Reserved for ATA/ATAPI-10 9 Reserved for ATA/ATAPI-9 8 Reserved for ATA/ATAPI-8 7 1 = supports ATA/ATAPI-7 6 1 = supports ATA/ATAPI-6 5 1 = supports ATA/ATAPI-5 4 1 = supports ATA/ATAPI-4 3 Obsolete 2 Obsolete 1 Obsolete 0 Reserved	0080h
81	Minor version number 0000h or FFFFh = device does not report version 0001h-FFFEh = See 6.17.41	0000h
82	Command set supported. 15 Obsolete 14 1 = NOP command supported 13 1 = READ BUFFER command supported 12 1 = WRITE BUFFER command supported 11 Obsolete 10 1 = Host Protected Area feature set supported 9 1 = DEVICE RESET command supported 8 1 = SERVICE interrupt supported 7 1 = release interrupt supported	742Bh

	6	1 = look-ahead supported	
	5	1 = write cache supported	
	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.	
	3	1 = mandatory Power Management feature set supported	
	2	1 = Removable Media feature set supported	
	1	1 = Security Mode feature set supported	
	0	1 = SMART feature set supported	
83	Command sets supported.		5100h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = FLUSH CACHE EXT command supported	
	12	1 = mandatory FLUSH CACHE command supported	
	11	1 = Device Configuration Overlay feature set supported	
	10	1 = 48-bit Address feature set supported	
	9	1 = Automatic Acoustic Management feature set supported	
	8	1 = SET MAX security extension supported	
	7	See Address Offset Reserved Area Boot, INCITS TR27:2001	
	6	1 = SET FEATURES subcommand required to spinup after power-up	
	5	1 = Power-Up In Standby feature set supported	
	4	1 = Removable Media Status Notification feature set supported	
	3	1 = Advanced Power Management feature set supported	
	2	1 = CFA feature set supported	
	1	1 = READ/WRITE DMA QUEUED supported	
	0	1 = DOWNLOAD MICROCODE command supported	
84	Command set/feature supported extension		4003h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report	
	11	Reserved for technical report	
	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64-bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands	

	supported	
	5 1 = General Purpose Logging feature set supported	
	4 1 = Streaming feature set supported	
	3 1 = Media Card Pass Through Command feature set supported	
	2 1 = Media serial number supported	
	1 1 = SMART self-test supported	
	0 1 = SMART error logging supported	
85	Command and feature sets supported or enabled	
	15 Obsolete	0
	14 1 = NOP command enabled	0
	13 1 = READ BUFFER command enabled	0
	12 1 = WRITE BUFFER command enabled	0
	11 Obsolete	0
	10 1 = Host Protected Area feature set enabled	1
	9 1 = DEVICE RESET command enabled	0
	8 1 = SERVICE interrupt enabled	0
	7 1 = release interrupt enabled	0
	6 1 = look-ahead enabled	0
	5 1 = Write Cache enabled	1
	4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.	0
	3 1 = Power Management feature set enabled	0
	2 1 = Removable Media feature set enabled	0
	1 1 = Security Mode feature set enabled	X
	0 1 = SMART feature set enabled	X
86	Command set/feature enabled	1000h
	15-14 0 = Reserved	
	13 1 = FLUSH CACHE EXT command supported	
	12 1 = FLUSH CACHE command supported	
	11 1 = Device Configuration Overlay supported	
	10 1 = 48-bit Address features set supported	
	9 1 = Automatic Acoustic Management feature set enabled	
	8 1 = SET MAX security extension enabled by SET MAX SET PASSWORD	
	7 See Address Offset Reserved Area Boot, INCITS TR27:2001	
	6 1 = SET FEATURES subcommand required to spin-up after power-up	
	5 1 = Power-Up In Standby feature set enabled	
	4 1 = Removable Media Status Notification feature set enabled	

	3	1 = Advanced Power Management feature set enabled	
	2	1 = CFA feature set enabled	
	1	1 = READ/WRITE DMA QUEUED command supported	
	0	1 = DOWNLOAD MICROCODE command supported	
87	Command and feature sets supported or enabled		0003h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report-	
	11	Reserved for technical report-	
	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64 bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported	
	5	1 = General Purpose Logging feature set supported	
	4	1 = Valid CONFIGURE STREAM command has been executed	
	3	1 = Media Card Pass Through Command feature set enabled	
	2	1 = Media serial number is valid	
	1	1 = SMART self-test supported	
	0	1 = SMART error logging supported	
88	15	Reserved	XX7Fh
	14	1 = Ultra DMA mode 6 is selected	
		0 = Ultra DMA mode 6 is not selected	
	13	1 = Ultra DMA mode 5 is selected	
		0 = Ultra DMA mode 5 is not selected	
	12	1 = Ultra DMA mode 4 is selected	
		0 = Ultra DMA mode 4 is not selected	
	11	1 = Ultra DMA mode 3 is selected	
		0 = Ultra DMA mode 3 is not selected	
	10	1 = Ultra DMA mode 2 is selected	
		0 = Ultra DMA mode 2 is not selected	
	9	1 = Ultra DMA mode 1 is selected	
		0 = Ultra DMA mode 1 is not selected	
	8	1 = Ultra DMA mode 0 is selected	
		0 = Ultra DMA mode 0 is not selected	

	7 Reserved 6 1 = Ultra DMA mode 6 and below are supported 5 1 = Ultra DMA mode 5 and below are supported 4 1 = Ultra DMA mode 4 and below are supported 3 1 = Ultra DMA mode 3 and below are supported 2 1 = Ultra DMA mode 2 and below are supported 1 1 = Ultra DMA mode 1 and below are supported 0 1 = Ultra DMA mode 0 is supported	
89	Time required for security erase unit completion	0001h
90	Time required for Enhanced security erase completion	0000h
91	Current advanced power management value	0000h
92	Master Password Revision Code	FFFEh
93	Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset. 15 Shall be cleared to zero. 14 Shall be set to one. 13 1 = device detected CBLID- above ViH 0 = device detected CBLID- below ViL 12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows: 12 Reserved. 11 0 = Device 1 did not assert PDIAG-. 1 = Device 1 asserted PDIAG-. 10-9 These bits indicate how Device 1 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 8 Shall be set to one.	XXXXh

	7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows: 7 Reserved. 6 0 = Device 0 does not respond when Device 1 is selected. 1 = Device 0 responds when Device 1 is selected. 5 0 = Device 0 did not detect the assertion of DASP-. 1 = Device 0 detected the assertion of DASP-. 4 0 = Device 0 did not detect the assertion of PDIAG-. 1 = Device 0 detected the assertion of PDIAG-. 3 0 = Device 0 failed diagnostics. 1 = Device 0 passed diagnostics. 2-1 These bits indicate how Device 0 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 0 Shall be set to one.	
94	15-8 Vendor's recommended acoustic management value. 7-0 Current automatic acoustic management value.	0000h
95	Stream Minimum Request Size	0000h
96	Streaming Transfer Time - DMA	0000h
97	Streaming Access Latency - DMA and PIO	0000h
98-99	Streaming Performance Granularity	0000h
100-103	Maximum user LBA for 48-bit Address feature set.	0000h
104	Streaming Transfer Time - PIO	0000h
105	Reserved	0000h
106	Physical sector size / Logical Sector Size 15 Shall be cleared to zero 14 Shall be set to one 13 1 = Device has multiple logical sectors per physical sector. 12 1= Device Logical Sector Longer than 256 Words 11-4 Reserved 3-0 2^X logical sectors per physical sector	0000h
107	Inter-seek delay for ISO-7779 acoustic testing in microseconds	0000h
108	15-12 NAA (3:0) 11-0 IEEE OUI (23:12)	0000h
109	15-4 IEEE OUI (11:0) 3-0 Unique ID (35:32)	0000h

110	15-0 Unique ID (31:16)	0000h
111	15-0 Unique ID (15:0)	0000h
112-115	Reserved for world wide name extension to 128 bits	0000h
116	Reserved for technical report-	0000h
117-118	Words per Logical Sector	0000h
119-120	Reserved	0000h
121-126	Reserved	0000h
127	Removable Media Status Notification feature set support 15-2 Reserved 1-0 00 = Removable Media Status Notification feature set not supported 01 = Removable Media Status Notification feature supported 10 = Reserved 11 = Reserved	0000h
128	Security Status 15-9 Reserved 8 Security level 0 = high, 1 = Maximum 7-6 Reserved 5 1= Enhanced security erase supported 4 1= Security count expired 3 1 = Security frozen 2 1 = Security locked 1 1 = Security enabled 0 1 = Security supported	 0 X 0 0 0 X X X 1
129-159	Vendor specific	0000h
160	CFA power mode 1 15 Word 160 supported 14 Reserved 13 CFA power mode 1 is required for one or more commands implemented by the device 12 CFA power mode 1 disabled 11-0 Maximum current in ma	0000h
161-175	Reserved for assignment by the CompactFlash™ Association	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15-8 Checksum 7-0 Signature	XXXXh

5.10.5 Idle -97H or E3H

Table 1: Idle information

Register	7	6	5	4	3	2	1	0
Command(7)	97h or E3h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Timer Count (5 msec increments)							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

5.10.6 Idle immediate - 95H or E1H

Table 40: Idle immediate information

Register	7	6	5	4	3	2	1	0
Command(7)	95h or E1h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt.

5.10.7 Read Buffer - E4h

Table 41: Read buffer information

Register	7	6	5	4	3	2	1	0
Command(7)	E4h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

5.10.8 Read DMA - C8h

Table 42: Read DMA information

Register	7	6	5	4	3	2	1	0
Command(7)	C8h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16							
Cylinder Low(4)	Cylinder Low (LBA 15-8							
Sector Number(3)	Sector Numbe(LBA 7-0							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 request 256 sectors. The transfer begins at he sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, cleat BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 & sector –count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts –DMACK while it is ready to transfer data by DMA and asserts –IORD once for each 16 bit word to be

transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder, head, and sector number of the sector where the occurred. The amount of data transferred is indeterminate. When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

5.10.9 Read Sector(s) - 20h

Table 43: Read sector information

Register	7	6	5	4	3	2	1	0
Command(7)	20h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has buffer, sets DRQ, cleats BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder head, and sector number of the sector 2where the error occurred. The flawed data is pending in the sector buffer.

5.10.10 Read Verify Sector(s) - 40h

Table 44: Read verify sector information

Register	7	6	5	4	3	2	1	0
Command(7)	40h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY. When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified. If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

5.10.11 Set Features - Efh

Table 45: Set feature information

Register	7	6	5	4	3	2	1	0
Command(7)	Efh							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Config							
Feature(1)	Feature							

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the CompactFlash Storage Card shall return command aborted.

Table 46: Feature Supported

Command Name	Code	Sub Command
Set Transfer Mode	Efh	03h
Disable Read Look-ahead feature	Efh	55h
Enable write cache	Efh	02h
Disable reverting to power-on defaults	Efh	66h
Disable write cache	Efh	82h
Enable reverting to power-on defaults	Efh	CCh

5.10.12 Set Multiple Mode – C6h

Table 47: Set multiple mode information

Register	7	6	5	4	3	2	1	0
Command(7)	C6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command enables the CompactFlash Storage Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the CompactFlash Storage Card sets BSY to 1 and checks the Sector Count Register. If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write multiple disabled.

5.10.13 Set Sleep Mode –E6h

Table 48: Set sleep mode information

Register	7	6	5	4	3	2	1	0
Command(7)	E6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds.

5.10.14 Standby –E2h

Table 49: Standby information

Register	7	6	5	4	3	2	1	0
Command(7)	E2h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, cleat BSY and return interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

5.10.15 Standby Immediate –E0h

Table 50: Standby immediate information

Register	7	6	5	4	3	2	1	0
Command(7)	E0h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

5.10.16 Write Buffer – E8h

Table 51: Write buffer information

Register	7	6	5	4	3	2	1	0
Command(7)	E8h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfer 512 bytes.

5.10.17 Write DMA – Cah

Table 52: Write DMA information

Register	7	6	5	4	3	2	1	0
Command(7)	Cah							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low(LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512*sector count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the host asserts –DMACK while it is ready to transfer data by DMA and asserts –IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecovertable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The amount of data transferred is indeterminate. When a write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

5.10.18 Write Multiple- C5h

5.10.18.1 Command Code

C5h

5.10.18.2 Protocol

PIO data-out

5.10.18.3 Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 53: Write multiple command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C5h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

5.10.18.4 Normal Output

Table 54: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register-

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.10.18.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block register contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 55: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, include an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if an address outside of the range of user-accessible address is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device -

Shall be written with the address of first unrecoverable error.

Status register-

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.10.18.6 Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

5.10.18.7 Description

This command writes the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by the content of word 59 of the IDENTIFY DEVICE response.

When the WRITE MULTIPLE command is issued, the SECTOR Count register contains the number of sectors (not the number of blocks) requested. The device shall interrupt for each DRQ block transferred.

IF the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

N = Remainder (sector count / block count).

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

5.10.19 Write Sector(s) – 30h

Table 56: Write sector information

Register	7	6	5	4	3	2	1	0
Command(7)	30h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A

sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash Storage Card sets BST, then sets DRQ and clears BSDY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

5.10.20 Security Set Password- F1h

5.10.20.1 Command Code

F1h

5.10.20.2 Feature Set

Security Mode feature set

5.10.20.3 Protocol

PIO data-out

5.10.20.4 Inputs

Table 57: Security set password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F1h							

Device –

DEV shall specify the selected device.

Normal Outputs

Table 58: Security set password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

5.10.20.5 Error Outputs

Table 59: Security set password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.10.20.6 Prerequisites

DRDY set to one.

5.10.20.7 Description

This command transfer 512 byte of data from the host. Table 10 defines the content of this information. The data transferred controls the function of this command. Table 11 defines the interaction of the identifier and security level bits.

The revision code field shall be returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision Code is not supported.

Table 60: Security set password command's data content

Word	Content
0	Control Word Bit 0 Identifier 0=set User password 1=set Master password Bits (7:1) Reserved Bit(8) Security level 0=High 1=Maximum Bits(15:9) Reserved
1-16	Password(32 bytes)
17	Master Password Revision Code()
18-255	Reserved

Table 61: Security Set password command's identifier and security level bit interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall than be unlocked by either the User password it the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be unlock
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. Master password revision code set to the value in

		Master Password Revision Code field.

5.10.21 Security Unlock- F2h

5.10.21.1 Command Code

F2h

5.10.21.2 Feature Set

Security Mode feature set

5.10.21.3 Protocol

PIO data-out

5.10.21.4 Inputs

Table 62: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F2h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 63: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

5.10.21.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 64: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.10.21.6 Prerequisites

DRDY set to one.

5.10.21.7 Description

This command transfers 512 bytes of data from the host. Table13 defines the content of this information. If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device shall compare the supplied password with the stored User password. If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall decremented for each password mismatch when SECURITY UNLOCK and SECURITY ERASE UNIT commands shall be command aborted until a power-on

reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

5.10.22 Security Erase Prepare- F3h

5.10.22.1 Command Code

F3h

5.10.22.2 Feature Set

Security Mode feature set

5.10.22.3 Protocol

Non-data

5.10.22.4 Inputs

Table 65: Security erase prepare command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F3h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 66: Security erase prepare command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

5.10.22.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 67: Security erase prepare command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.10.22.6 Prerequisites

DRDY set to one.

5.10.22.7 Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental loss of data on the device.

5.10.23 Security Erase Unit- F4h

5.10.23.1 Command Code

F4h

5.10.23.2 Feature Set

Security Mode feature set

5.10.23.3 Protocol

PIO data-out.

5.10.23.4 Inputs

Table 68: Security erase unit command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F4h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 69: Security erase unit command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

5.10.23.5 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 70: Security erase unit command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.10.23.6 Prerequisites

DRDY set to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

5.10.23.7 Description

This command transfer 512 bytes of data from the host. Table12 defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device shall command abort the SECURITY ERASE UNIT command.

When Normal Erase mode is specified, the SECURITY ERASE UNIT command shall write binary zeroes to all user data areas. The Enhanced Erase mode is optional. When Enhanced Erase Mode is specified, the device shall write predetermined data patterns to all user areas. In Enhanced Erase mode, all previously written user data shall be overwritten, including sectors that are no longer in use due to reallocation.

This command shall disable the device Lock mode, however, the Master password shall still be stored internally within the device and may be reactivated later a new User password is

set.

Table 71: Security erase unit password information

Word	Content
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit 1 Erase mode 0=Normal Erase 1=Enhanced Erase Bit(15:2) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

5.10.24 Security Freeze Lock- F5h

5.10.24.1 Command Code

F5h

5.10.24.2 Feature Set

Security Mode feature set

5.10.24.3 Protocol

Non-data.

5.10.24.4 Inputs

Table 72: Security freeze lock for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	Na	Na	Na	Na	Na
Command	F5h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 73: Security freeze lock for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

5.10.24.5 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 74: Security freeze lock for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.10.24.6 Prerequisites

DRDY set to one.

5.10.24.7 Description

The SECURITY FREEZE LOCK command shall set the device to Frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset. If SECURITY FREEZE LOCK shall be issued when the device in Frozen mode, the command executes and the device shall remain in Frozen mode.

Command disabled by SECURITY FREEZE LOCK are:

- SECUIRTY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

5.10.25 Security Disable Password- F6h

5.11.25.1 Command Code

F6h

5.11.25.2 Feature Set

Security Mode feature set

5.11.25.3 Protocol

PIO data-out.

5.11.25.4 Inputs

Table 75: Security disable password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F6h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 76: Security disable password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

5.11.25.5 Error Outputs

The device shall return aborted if the device is in Locked mode, or device is in Frozen mode.

Table 77: Security disable password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.11.25.6 Prerequisites

DRDY set to one. Device shall be in Unlocked mode.

5.11.25.7 Description

The SECURITY DISABLE PASSWORD command transfer 512 bytes of data from the host. Table 13 defines the content of this information. If the password selected by word 0 matches the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password if set.

Table 78: Security disable password command content

Word	Content
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit(15:1) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

5.10.26 SMART

Individual SMART commands are identified by the value placed in the Feature register.

Table 79: SMART Feature register values

Value	Command
D0h	SMART Read Data
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS

5.10.27 SMART Read Data

5.10.27.1 Command Code

B0h with a Feature register value of D0h

5.10.27.2 Feature Set

Smart Feature Set

Operation when the SMART feature set is implemented.

5.10.27.3 Protocol

PIO data-in

5.10.27.4 Inputs

Table 80: SMART command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 81: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.10.27.5 Prerequisites

DRDY set to one. SMART enabled.

5.10.27.6 Description

This command returns the Device SMART data structure to the host.

Table 82: SMART data structure

BYTE	Description
0-1	Revision code
2-361	Vendor specific
362	Off-line data collection status

363	Self-test execution status byte
364-365	Total time in seconds to complete off-line data collection activity
366	Vendor specific
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability *7-1 Reserved *0 1 = Device error logging supported
371	Vendor specific
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374	Conveyance self-test routine recommended polling time (in minutes)
375-385	Reserved
386-395	Firmware Version/Date Code
396-399	Reserved
400-406	Controller name
407-511	Reserved
511	Checksum

5.10.28 SMART ENABLE OPERATIONS

5.10.28.1 Command Code

B0h with a Feature register value of D8h

5.10.28.2 Feature Set

Smart Feature Set

5.10.28.3 Protocol

Non-data

5.10.28.4 Inputs

Table 83: SMART Enable command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

5.10.28.5 Normal Outputs

Table 84: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.10.28.6 Prerequisites

DRDY set to one.

5.10.28.7 Description

This command enables access to all SMART capabilities within device.

5.10.29 SMART DISABLE OPERATIONS

5.10.29.1 Command Code

B0h with a Feature register value of D9h

5.10.29.2 Feature Set

Smart Feature Set

5.10.29.3 Protocol

Non-data

5.10.29.4 Inputs

Table 85: SMART DISABLE Command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							

Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

5.10.29.5 Normal Outputs

Table 86: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.10.29.6 Prerequisites

DRDY set to one. SMART enabled.

5.10.29.7 Description

This command disables all SMART capabilities within device.

6. Device Parameters

iCF 1SE2 device parameters are listed in Table 87.

Table 87: Device parameter

Capacity	Cylinders	Heads	Sectors	LBA	Capacity(MB)
512MB	991	16	63	998928	487.8
1GB	1,966	16	63	1981728	967.64
2GB	3,900	16	63	3931200	1,919.53
4GB	7,785	16	63	7847280	3,831.68
8GB	15,338	16	63	15662304	7,647.61
16GB	31,045	16	63	31293360	15,279.96
32GB	62,041	16	63	62537328	30,535.80
64GB	16,383	16	63	125059072	61,064.00

7. Innodisk Part Number Rule

CODE	1	2	3	4	5		6	7	8	9	10	11	12	13	14	15	16		17
	D	**E**	**C**	**F**	**C**	**-**	**0**	**8**	**G**	**D**	**5**	**3**	**A**	**C**	**2**	**D**	**B**	**-**	**X**
Description	Disk	iCF 1SE2				-	Capacity			Controller			Flash Mode	Operation Temp.	Internal Control	Ch.	Flash Type	-	Customized Code

Definition	
Code 1st (Disk)	**Code 13th (Operation Temperature)**
D : Disk	C : Standard Grade (0 ~ +70 ℃)
	W : Industrial Grade (-40 ~ +85 ℃)
Code 2nd ~ 5th (Form Factor)	**Code 14th (Internal Control Code)**
ECFC : CF, Type I	1~9 TSOP PCB version
Code 6th ~8th (Capacity)	**Code 15th (Channel of data transfer)**
512: 512MB	S: Single Channel
01G: 1GB	D: Dual Channels
02G: 2GB	
04G: 4GB	**Code 16th (Flash Type)**
08G: 8GB	B: Toshiba SLC
16G: 16GB	
32G: 32GB	**Code 17th (Customized/Internal Code)**
64G: 64GB	
Code 9th ~ 11th (Controller)	
D53 : ID232	
Code 12th (Flash Mode)	
A: Async Flash	