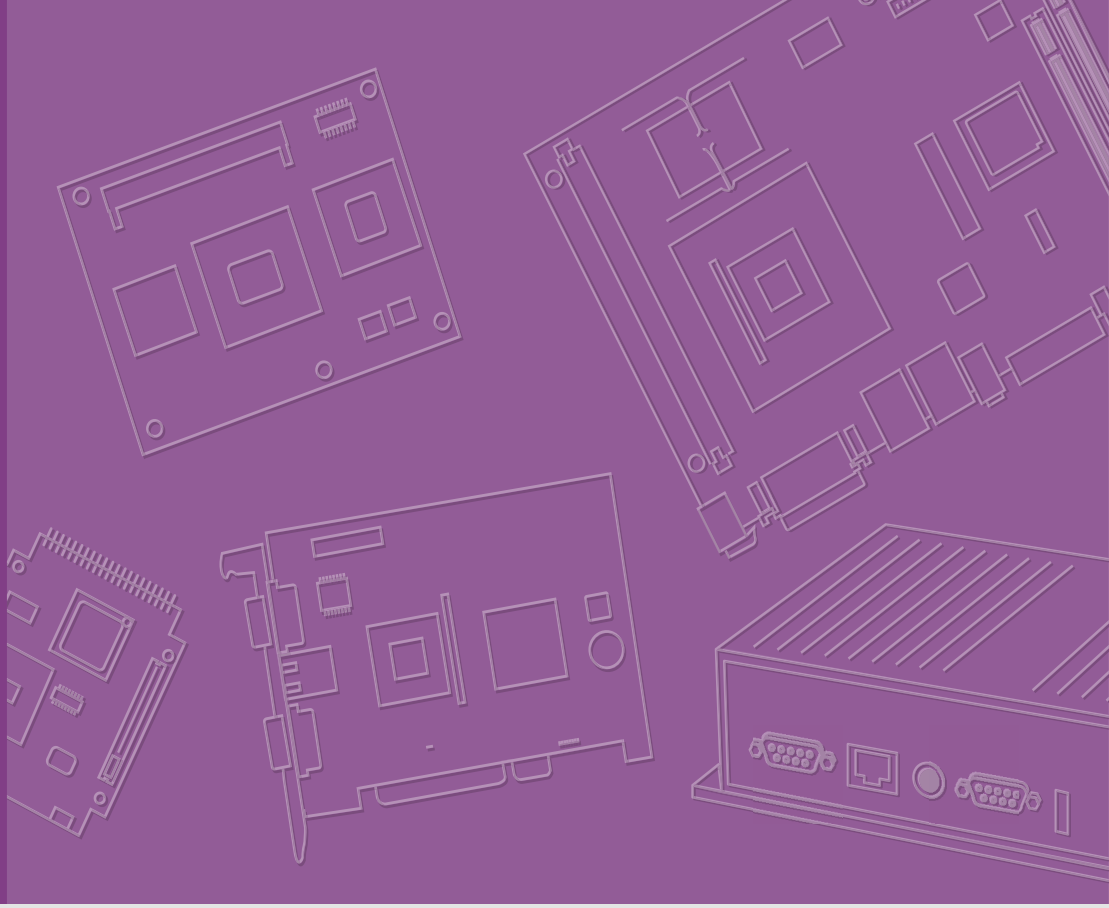

User Manual

SOM-E780

AMD EPYC™ 7003 Processor
COM-HPC® Server Size E
Module with Proprietary Pinout

ADVANTECH

Enabling an Intelligent Planet

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Acknowledgments

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Product Warranty (2 Years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Test conditions for passing also include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

FM

This equipment has passed FM certification. According to the National Fire Protection Association, work sites are categorized into different classes, divisions, and groups based on hazard considerations. This equipment is compliant with the specifications for Class I, Division 2, Groups A, B, C, and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions, and Notes

Warning! *Warnings indicate conditions that could cause personal injury if not observed!*

Caution! *Cautions are included to help prevent hardware damage and data loss. For example,*

"Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions."

Note! *Notes provide additional and/or optional information.*

Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all feedback in writing to support@advantech.com.

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- SOM-E780 CPU module

Selection Guide w/ P/N

Part No.	CPU	Cores	Base Freq.	Max Turbo Freq.	CPU TDP	CPU Threads	DDR4 RDIMM/ LRDIMM	Thermal Solution	Operating Temp.
SOM-E780S64-U0A1	EPYC™ 7713P	64	2.0GHz	3.675GHz	225W	128	3200 MHz	Active * Optional Accessories	0 ~ 60°C
SOM-E780S32-U8A1	EPYC™ 7543P	32	2.8GHz	3.7GHz	225W	64	3200 MHz	Active * Optional Accessories	0 ~ 60°C
SOM-E780S24-U8A1	EPYC™ 7443P	24	2.85GHz	4.0GHz	200W	48	3200 MHz	Active * Optional Accessories	0 ~ 60°C
SOM-E780S16-H0A1	EPYC™ 7313P	16	3.0GHz	3.7GHz	155W	32	3200 MHz	Active * Optional Accessories	0 ~ 60°C

* Other combinations are supported by project. Please contact sales for details.

A thermal solution is not included in the standard package. Please remember to place an order for a thermal solution.

Development Board

Part No.	Description
SOM-DH7000-00A1	COM-HPC Size E proprietary Dev. Board A1

Optional Accessories

Part No.	Description
1970005652T001	One piece heatsink, 225W, 119.3 x 78.9 x 22.6 mm
1970005648N000	C.L R3, 200 x 160 x 100.96 mm, SC SOM-E780

Safety Precautions - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
- Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped and damaged.
    - The equipment shows obvious signs of breakage.
15. Do not leave the equipment in an environment with a storage temperature of below -20°C (-4°F) or above 60°C (140°F) as this may damage the components. The equipment should be kept in a controlled environment.
16. CAUTION: Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
17. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position should not exceed 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Acronyms

Term	Define
AC'97	Audio CODEC (Coder-Decoder)
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PC-AT systems
BIOS	Basic Input Output System – firmware in a PC-AT system that is used to initialize system components before handing control over to the operating system
CAN	Controller-area network (CAN or CAN bus) is a vehicle bus standard designed to allow microcontrollers to communicate with each other within a vehicle without a host computer
DDI	Digital Display Interface – containing DisplayPort, HDMI/DVI, and SDVO
EAPI	Embedded Application Programmable Interface Software interface for COM Express® specific industrial function ■ System information ■ Watchdog timer ■ I2C Bus ■ Flat Panel brightness control ■ User storage area ■ GPIO
GbE	Gigabit Ethernet
GPIO	General purpose input output
HDA	Intel High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio that is capable of playing back more channels at higher quality than AC'97
I2C	Inter Integrated Circuit – 2-wire (clock and data) signaling scheme allowing communication between integrated circuit, primarily used to read and load register values
ME	Management Engine
PC-AT	"Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel-based personal computer in 1990s
PEG	PCI Express Graphics
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information
TPM	Trusted Platform Module, chip to enhance the security features of a computer system
UEFI	Unified Extensible Firmware Interface
WDT	Watchdog Timer

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Chapter 1

General Information

This chapter details background information on the SOM-E780 CPU Computer on Module.

Sections include:

- Introduction
- Functional Block Diagram
- Product Specifications

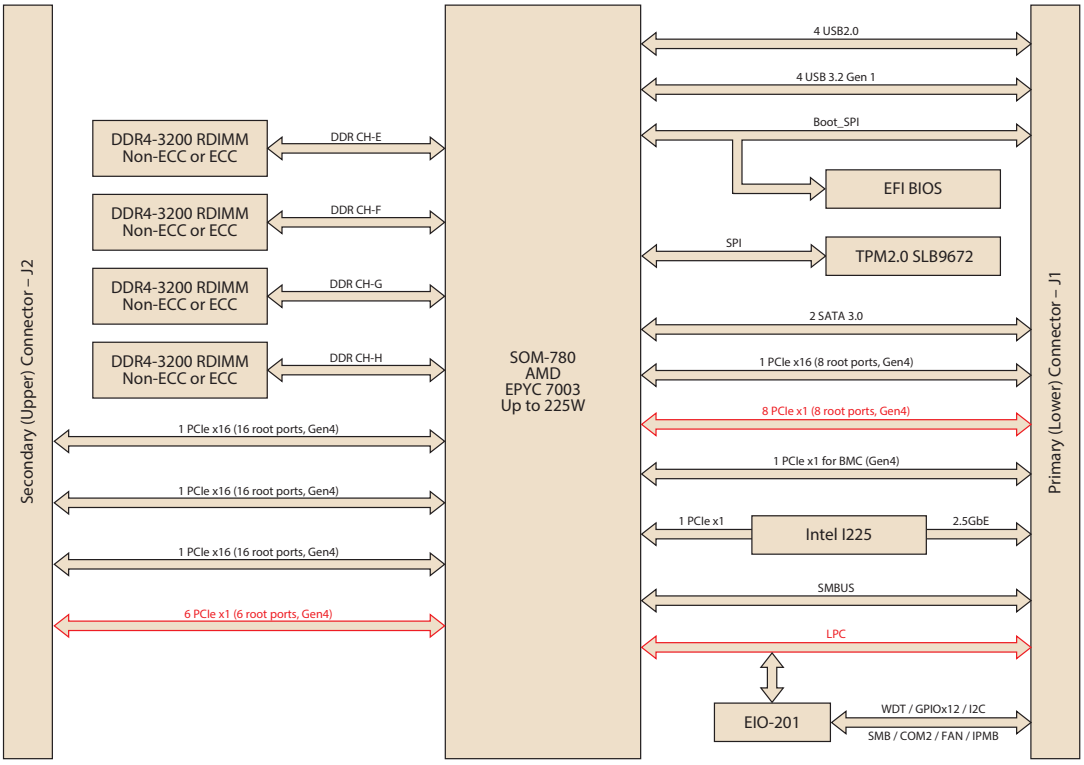
1.1 Introduction

The Advantech SOM-E780 is a COM-HPC CPU Module powered by an AMD EPYC 7003 server-grade CPU. It conforms to the COM-HPC Server Size E module with a proprietary pinout and can accommodate up to 512 gigabytes of DDR4 memory. What sets it apart is that it offers an impressive 79 PCIe Gen4 lanes, which is 14 more lanes than the standard COM-HPC configuration.

In terms of connectivity, the SOM-E780 is designed to support 1 Intel i225, 2 SATA 3.0 ports, 4 USB 3.2 Gen1 ports, 4 USB 2.0 ports, 2 COM ports (4-wire), and TPM 2.0 functionality. It can operate in temperatures ranging from 0 to 60°C with fan-equipped cooling (QFCS).

The Advantech iManager (SUSI 4) suite is a comprehensive management solution that caters to various needs. It offers support for multi-level watchdog timers, voltage and temperature monitoring, thermal protection and mitigation, LCD backlight control (on/off and brightness), and embedded storage control. It's worth noting that all Advantech COM-HPC modules come integrated with iManager and WISE-PaaS/RMM, enhancing their management capabilities.

1.2 Functional Block Diagram



1.3 Product Specifications

1.3.1 Compliance

- PICMG COM-HPC Revision 1.10 (proprietary pinout)
- Size E 200 x 160 mm
- Pin-out Server Type compatible (proprietary pinout)

1.3.2 Feature List

Table 1.1: Feature List

Feature Type	Connector	Feature	COM HPC Definition		SOM-E780
			Max.	Min.	
Display	J1	eDP	0	0	0
	J1	DDI0	0	0	0
	J1	DDI1	0	0	0
	J2	DDI2	0	0	0
Expansion	J1	PCI Express	25	0	25
	J2	PCI Express	54	0	54
Serial	J1	SMBus	1	0	1
	J1	I^2C Bus	2	0	2
	J1	IPMB	1	0	1
	J1	UART	2	0	2
I/O	J1-J2	NBASE-T (max. 10G)	1	0	1
	J2	ETH KR (max 25G)	0	0	0
	J2	ETH KR CEI	0	0	0
	J1	USB 2.0	8	0	4
	J1-J2	USB 3.2 Gen 1	4	0	4
	J1	USB C PD I2C	1	0	0
	J1	Soundwire/DMIC	0	0	0
	J1	I2S/2xSNDW	0	0	0
	J1	HD Audio	0	0	0
	J1	SATA	2	0	2
	J1	LPC	1	0	1
	J1	BOOT_SPI	1	0	1
	J1	GP_SPI	1	0	0
	J1	GPIO	12	0	12
	J1	MISC	1	0	0
	J1	Functional Safety	1	0	0
	J1	Fan PWM/Tachometer	2	0	2
	J1	Trusted Platform Modules	1	0	1
Power	J1-J2	Power	50	0	50
	J1-J2	Standby Power	4	0	4
	J1-J2	GND	227	0	227
	J1	RSVD	10	0	10

1.3.3 Processor System

Table 1.2: Processor System

CPU	Cores	Core Base	Max Turbo Freq.	Cache (MB)	TDP(W)
EPYC™ 7713P	64	2.0GHz	3.675GHz	256	225W
EPYC™ 7543P	32	2.8GHz	3.7GHz	256	225W
EPYC™ 7443P	24	2.85GHz	4.0GHz	128	200W
EPYC™ 7313P	16	3.0GHz	3.7GHz	128	155W

1.3.4 Memory

There are a total of 4 memory sockets on the SOM-E780. These support 128GB max capacity with 288-pin SODIMM sockets (dual-channel).

4 x RDIMM, 1 DPC, 3200 MT/s, max DIMM capacity 64GB, up to 256GB

4 x LRDIMM, 1 DPC, 3200 MT/s, max DIMM capacity 128GB, up to 512GB

1.3.5 Expansion Interfaces

1.3.5.1 PCIe Gen4 x16

PCI Express x16: Supports default 3 Groups to have 4 ports PCIe x16 compliant to PCIe Gen4 (16.0 GT/s) specifications, configurable to PCIe x16, x8, x4. Several configurable combinations may need BIOS modification. Please contact Advantech sales or FAE for more details.

1.3.5.2 PCIe Gen4 x8 (Proprietary*1)

PCI Express x8: Supports default 1 port PCIe x8 compliant to PCIe Gen4 (16.0 GT/s) specifications, configurable to PCIe x8 or PCIe x4. Several configurable combinations may need BIOS modification. Please contact the Advantech sales or FAE for more details.

1.3.5.3 PCIe Gen4 x4 (Proprietary*1)

PCI Express x4: Supports default 1 port PCIe x4 compliant to PCIe Gen4 (16.0 GT/s) specifications, configurable only to PCIe x4.

1.3.5.4 PCIe Gen4 x1 (Proprietary *2, BMC *1)

PCI Express x1: Supports by default 3 ports PCIe x1 compliant to PCIe Gen4 (16.0 GT/s) specifications.

Table 1.3:

Group	PCIe Lane	Source	Port	Default
Group 0 Low (J1)	PCIe0	PCIE G2 group	#0	PCIe x16_Slot1
	PCIe1		#1	
	PCIe2		#2	
	PCIe3		#3	
	PCIe4		#4	
	PCIe5		#5	
	PCIe6		#6	
	PCIe7		#7	
Group 0 High (J1)	PCIe8		#8	
	PCIe9		#9	
	PCIe10		#10	
	PCIe11		#11	
	PCIe12		#12	
	PCIe13		#13	
	PCIe14		#14	
	PCIe15		#15	

Table 1.4:

Group	PCIe Lane	Source	Port	Default
Group ADD (J1)	PCIeA0	PCIE G1 group	#0	PCIe x8_Slot1
	PCIeA1		#1	
	PCIeA2		#2	
	PCIeA3		#3	
	PCIeA4		#4	
	PCIeA5		#5	
	PCIeA6		#6	
	PCIeA7		#7	

Table 1.5:

Group	PCIe Lane	Source	Port	Default
Group 1 (J2)	PCIe16	PCIE P2 group	#0	PCIe x16_Slot3
	PCIe17		#1	
	PCIe18		#2	
	PCIe19		#3	
	PCIe20		#4	
	PCIe21		#5	
	PCIe22		#6	
	PCIe23		#7	
	PCIe24		#8	
	PCIe25		#9	
	PCIe26		#10	
	PCIe27		#11	
	PCIe28		#12	
	PCIe29		#13	
	PCIe30		#14	
	PCIe31		#15	

Table 1.6:

Group	PCIe Lane	Source	Port	Default
Group 2 (J2)	PCIe32	PCIE P0 group	#0	PCIe x16_Slot2
	PCIe33		#1	
	PCIe34		#2	
	PCIe35		#3	
	PCIe36		#4	
	PCIe37		#5	
	PCIe38		#6	
	PCIe39		#7	
	PCIe40		#8	
	PCIe41		#9	
	PCIe42		#10	
	PCIe43		#11	
	PCIe44		#12	
	PCIe45		#13	
	PCIe46		#14	
	PCIe47		#15	

Table 1.7:

Group	PCIe Lane	Source	Port	Default
Group 3 (J2)	PCIe48	PCIE P3 group	#0	PCIe x16_Slot4
	PCIe49		#1	
	PCIe50		#2	
	PCIe51		#3	
	PCIe52		#4	
	PCIe53		#5	
	PCIe54		#6	
	PCIe55		#7	
	PCIe56		#8	
	PCIe57		#9	
	PCIe58		#10	
	PCIe59		#11	
	PCIe60		#12	
	PCIe61		#13	
	PCIe62		#14	
	PCIe63		#15	

Table 1.8:

Group	PCIe Lane	Source	Port	Default
Group ADD (J1)	PCIeA8	PCIE P1 group	#0	PCIe x4_Slot1
	PCIeA9		#1	
	PCIeA10		#2	
	PCIeA11		#3	
	PCIeA12		#4	PCIe x1_Slot2
	PCIeA13		#5	PCIe x1_Slot3

1.3.6 Serial Bus

1.3.6.1 SMBus

Supports the SMBus 2.0 specification.

1.3.6.2 I^2C Bus

Supports I2C bus 7-bit address modes. Supports standard mode up to 100 Kb/s, fast mode up to 400 Kb/s.

1.3.7 I/O

1.3.7.1 Gigabit Ethernet

Ethernet: Intel I225 Gigabit LAN supports 10/100/1000 Mbps & 2.5 Gbps Speed.

1.3.7.2 SATA

Supports 2 ports SATA Gen3 (6.0 Gb/s), backward compliant to SATA Gen2 (3.0 Gb/s) and Gen1 (1.5 Gb/s). The maximum data rate is 600 MB/s. It supports AHCI 1.3.1 mode (it does not support IDE mode).

1.3.7.3 USB 3.2 / USB 2.0

COM-HPC supports USB 3.2, but SOM-E780 supports 4 USB 3.2 Gen1 (5 Gbps) ports and 4 USB 2.0 (480 Mbps) ports.

Notice: Advantech strongly recommends using a certified cable to maximize USB 3.2 Gen1 performance.

1.3.7.4 USB 3.2 Gen1

Table 1.9: USB 3.2 Gen1

Server Type	P00	P01	P02	P03
SoC	P0	P1	P2	P3
Server Type	OC_01		OC_23	
SoC USB_OC#	OC_01		OC_23	

1.3.7.5 USB 2.0

Table 1.10: USB 2.0

Server Type	P00	P01	P02	P03
SoC	P0	P1	P2	P3
Server Type	OC_01		OC_23	
SoC USB_OC#	OC_01		OC_23	

1.3.7.6 SPI Bus

Supports BIOS flash only. SPI clock can be 50MHz, with a capacity up to 256Mb, 1.8V.

1.3.7.7 GPIO

12 programmable general purpose input or output (GPIO).

1.3.7.8 Watchdog

Supports multi-level watchdog time-out output. Provides 1-65535 levels, from 100ms to 109.22 minute intervals.

1.3.7.9 Serial port

2 x 2-wire serial ports (Tx/Rx) are 16550 UART compliant.

- Programmable FIFO or character mode
- 16-byte FIFO buffer on transmitter and receiver in FIFO mode
- Programmable serial-interface characteristics: 5-, 6-, 7-, or 8-bit characters
- Even, odd, or no parity bit selectable
- 1, 1.5, or 2 stop bits selectable
- Baud rate up to 115.2K

1.3.7.10 TPM

Supports a TPM 2.0 module.

1.3.7.11 Smart Fan

Supports 1 Fan PWM control signal and 1 tachometer input for fan speed detection. There is support for 2 fans on-module with a connector and the other to the carrier board following PICMG COM HPC R1.10 specifications.

1.3.7.12 BIOS

The BIOS chip is on the module by default. Users can place the BIOS chip on the carrier board with the appropriate design and jumper setting in BSEL#[2:0]

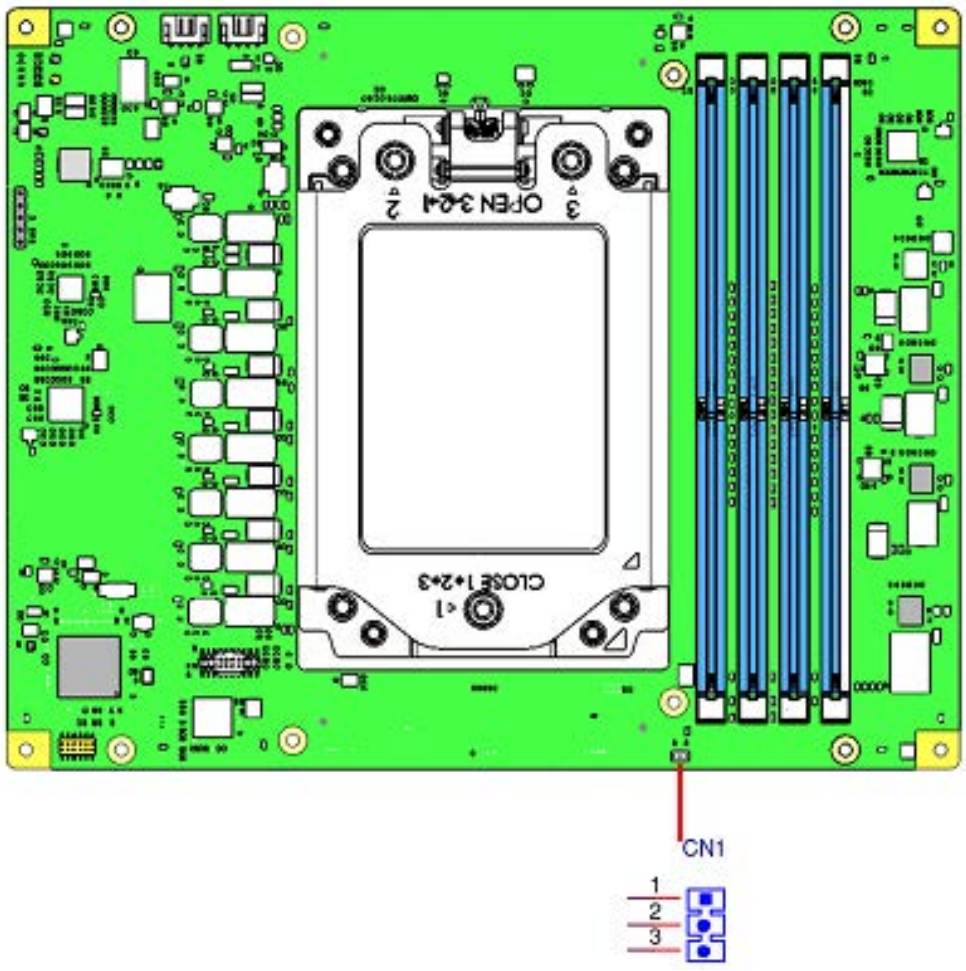
Table 1.11:

BSEL #2	BSEL #1	BSEL S#0	Boot up destination/function
NA	NA	Open	Boot from Module's SPI BIOS
NA	NA	GND	Boot from Carrier SPI BIOS

The standard module has no jumper at CN1, so BIOS settings are kept without an RTC coin battery. If you need to restore the BIOS to default settings, follow the steps below:

Table 1.12:

CN1	BIOS Settings Restore default
Pin	Function
1-X	Keep BIOS Settings [default]



1. Remove the coin battery.
2. Put a jumper on CN1 pins 2-3.

3. Turn on the power supply.
4. The system will boot up a few times.
5. The BIOS will load the default settings.

1.3.8 Power Management

1.3.8.1 Power Supply

There is support for both ATX and AT power modes. VSB is for suspended power and can be optional if not required by standby (suspend-to-RAM) support. The RTC battery may be optional if date/timekeeping is not required.

- Vin: 12V +/- 5%
- VSB: 5V +/- 5% (suspend power)
- RTC Battery Power: 2.0V - 3.3V

1.3.8.2 PWROK

Power is good from the main power supply. A high value indicates the power level is good. This signal can be used to postpone module startup allowing carrier-based FPGAs or other configurable devices time to be programmed.

1.3.8.3 Power Sequence

According to COM-HPC® Module Base specification.

1.3.8.4 Wake Event

Various wake event support allows users to apply different scenarios.

- Wake-on-LAN(WOL): Wake to S0 from S5
- PCIe Device Wake: depends on user inquiry and may need customized BIOS

1.3.9 Advantech S5 ECO Mode (Deep Sleep Mode)

Advantech iManager provides additional features allowing the system to enter a very low suspended power mode - S5 ECO mode. In this mode, the module will cut all power, including suspended and active power to the chipset, and keep an on-module controller active. Only power under 50mW will be consumed, meaning user battery packs can last longer. While this mode is enabled in the BIOS, the system (or module) only allows power button boot-up instead of other methods such as WOL.

1.3.10 Environmental Specifications

1.3.10.1 Temperature

- Operating: 0 ~ 60°C (32 ~ 140°F)
- Storage: -40 ~ 85°C (-40 ~ 185°F)

1.3.10.2 Humidity

- Operating: 40°C @ 95% relative humidity, non-condensing
- Storage: 60°C @ 95% relative humidity, non-condensing

1.3.10.3 Vibrations

IEC60068-2-64: Random vibration test under non-operation mode, 3.5 Grms. For operation, please contact the Advantech sales or FAE for more details.

1.3.10.4 Drop Test (Shock)

Federal Standard 101 Method 5007 test procedure with standard packing.

1.3.10.5 EMC

CE EN55032 Class B and FCC Certifications: validate with standard development boards on an Advantech chassis.

1.3.11 MTBF

Please refer to Advantech SOM-E780 Refresh Series Reliability Prediction report on the website: http://com.advantech.com

1.3.12 OS Support

The mission of Advantech Embedded Software Services is to "Enhance the quality of life with Advantech platforms and Microsoft Windows Embedded technology." We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows Embedded software solutions easily and widely available to the embedded computing community.

To install drivers, please connect to the website http://support.advantech.com.tw to download the setup file.

1.3.13 Advantech iManager

iManager supports APIs for GPIO, smart fan control, multi-stage watchdog timer, temperature sensor, and hardware monitoring. It follows PICMG EAPI 1.0 specifications with backward compatibility.

1.3.14 Power Consumption

Table 1.13: Power Consumption Table (Watts)

VCC=12V, VSB=5V	Active Power Domain			Suspend Power Domain		Mechanical Off
Power State	S0 Max. Load	S0 Burn-in	S0 Idle	S5	S5 Deep Sleep	RTC (uA)
SOM-E780S64-U0A1	261.34	251.34	39.39	1.12	0.3	4.43u

1.3.15 Hardware Configuration:

1. MB: SOM-E780S64-U0A1
2. DRAM: 32GB DDR5 3200MHz x 4pcs
3. Carrier board: SOM-DH7000-00A1

1.3.16 Test Conditions:

1. Test temperature: room temperature
2. Test voltage: ATX power
3. Test loading:
   - Maximum load mode: According to AMD thermal/power test tools.
   - Test software:
     1. AMD Validation Toolkit (AVT) 2.8.24.2094 AMD Confidential.
     2. Burn-In Test 10.1 (1004) for 64-bit Windows (CPU, RAM and Disk with 100%)
   - Idle mode: DUT power management off and not running any programs.

1.3.17 Performance

To compare performance or benchmark data with other modules, please refer to the “Advantech COM Performance & Power Consumption Table.”

1.3.18 Pin Descriptions

Advantech provides useful checklists for schematic design and layout routing. The schematic checklist will specify details about each pin’s electrical properties and how to connect them in different scenarios. The layout checklist will specify the layout constraints and recommendations for trace length, impedance, and other necessary information during design.

Please contact your nearest Advantech branch office or call to obtain the design documents and further advanced support.

Chapter 2

Mechanical Information

This chapter details mechanical information the SOM-E780 CPU Computer on Module.

Sections include:

- Board Information
- Mechanical Diagrams
- Assembly Diagram

2.1 Board Information

The figures below indicate the main chips on the SOM-E780 Computer-on-Module. Please be aware of these positions while designing your own carrier board to avoid mechanical issues and ensure thermal solution contact points for best thermal dissipation performance.

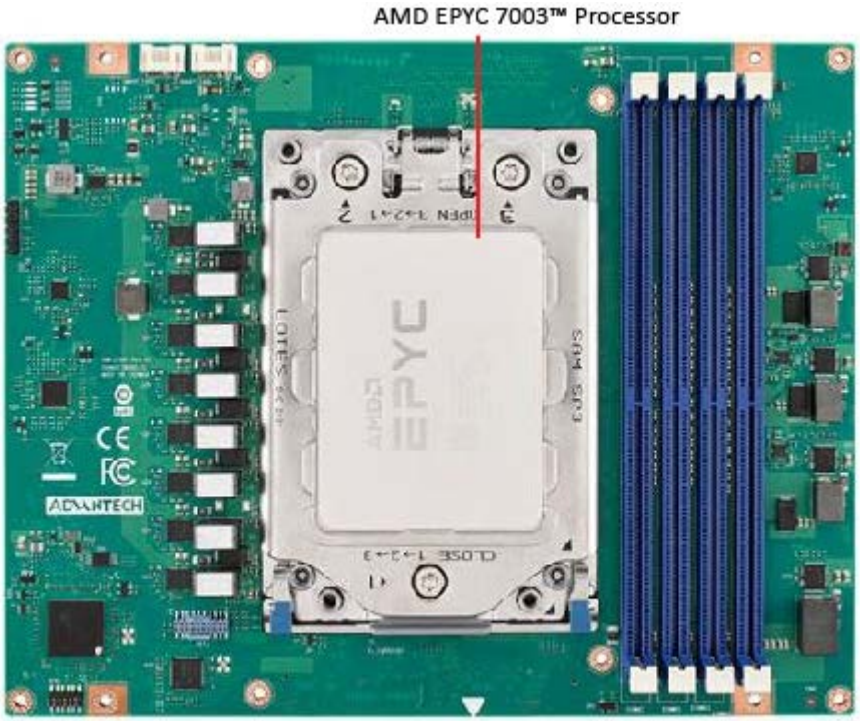


Figure 2.1 Board Chips ID – Front

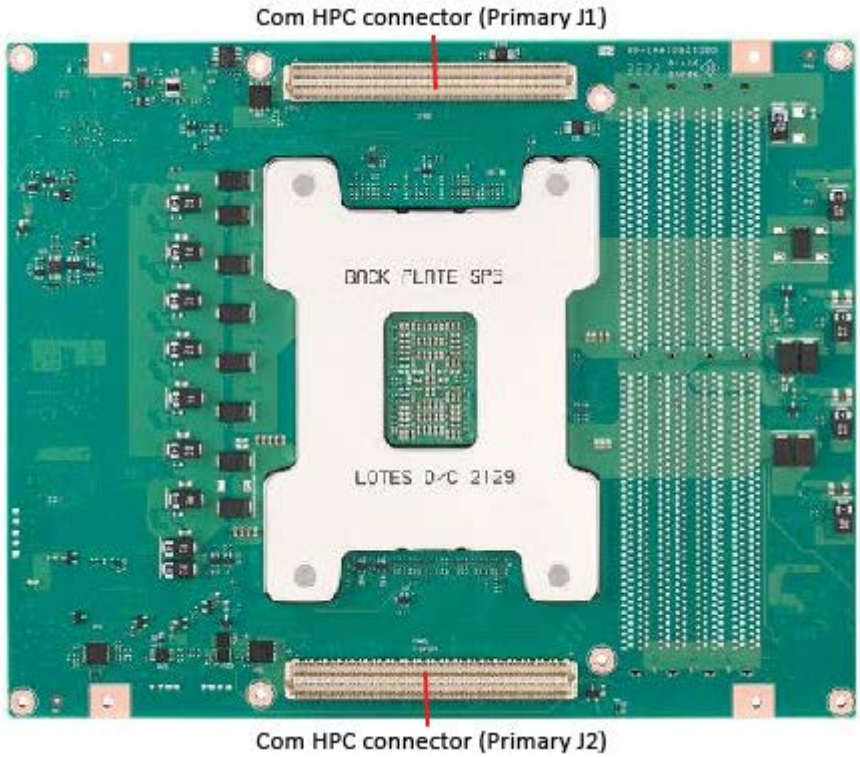


Figure 2.2 Board Chips ID – Rear

2.2 Mechanical Diagram

For more details about 2D/3D models, please find them on the Advantech COM support service website: http://com.advantech.com.

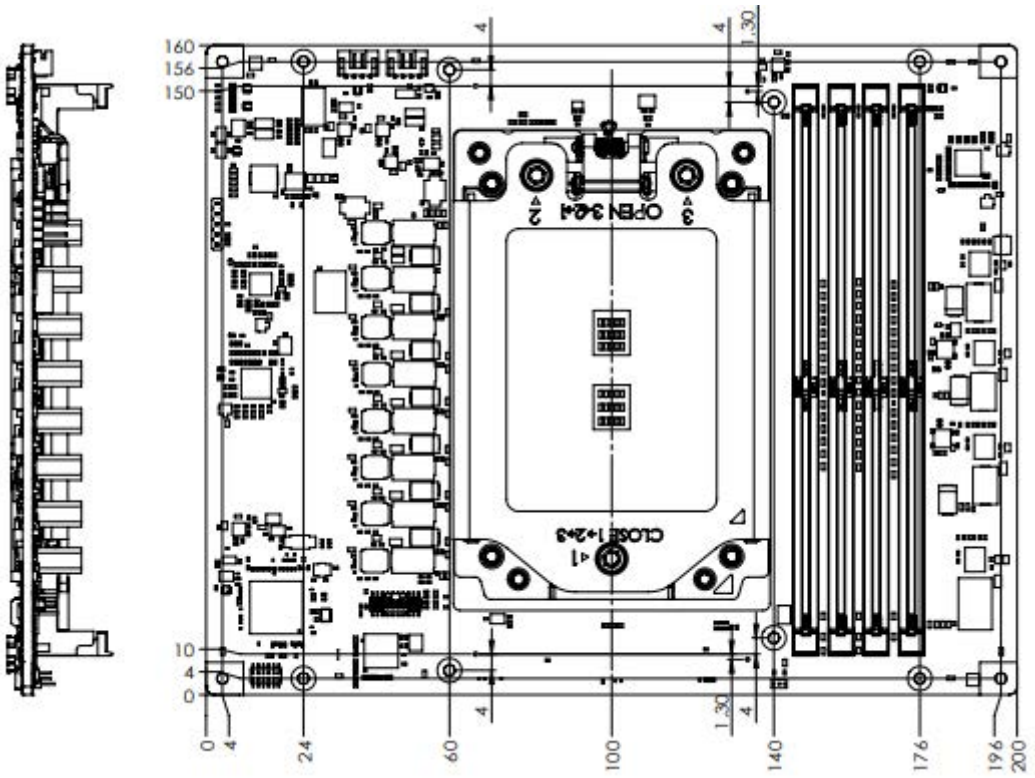


Figure 2.3 Board Mechanical Diagram - Front Side

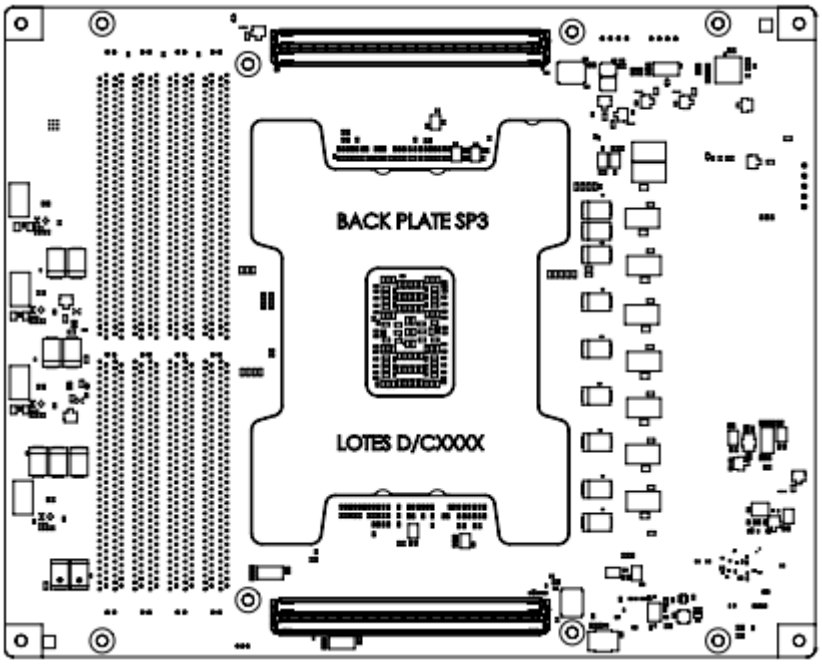


Figure 2.4 Board Mechanical Diagram - Rear Side

Figure 2.5 Atom Series Board Mechanical Diagram – Side

2.3 Assembly Diagram

These figures demonstrate the assembly order from the thermal module, to the COM module, to the carrier board.

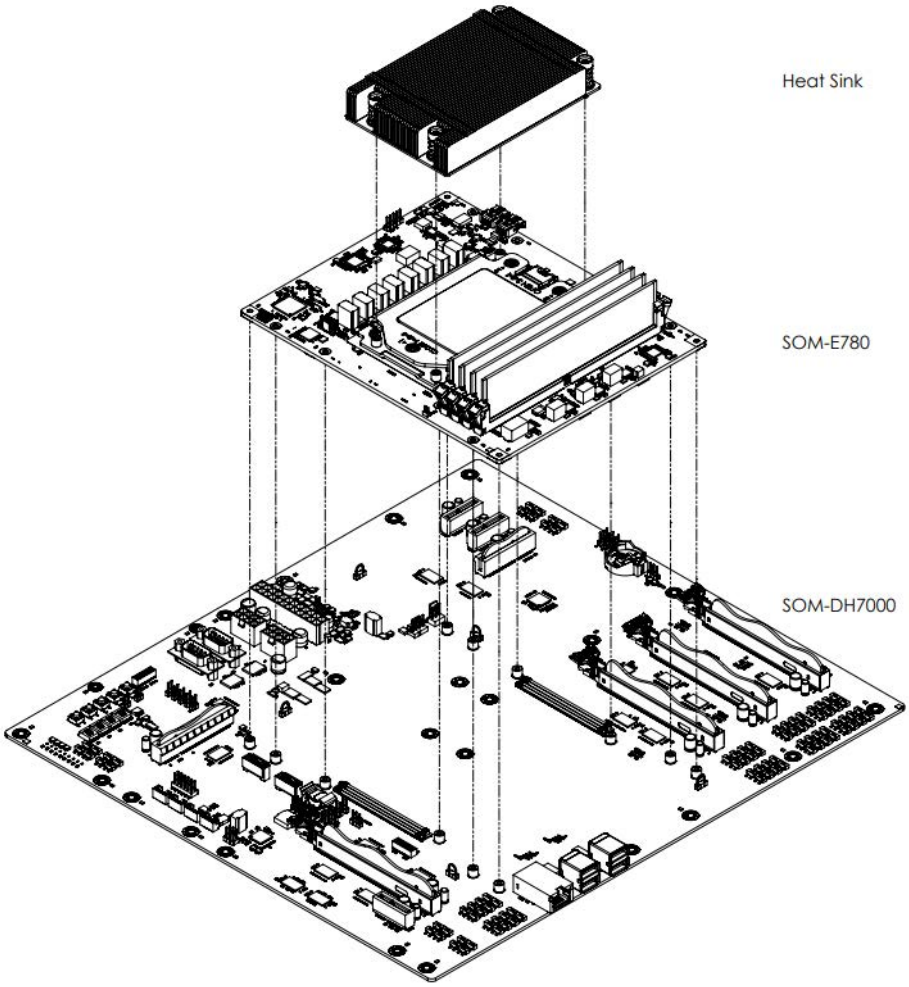


Figure 2.6 Assembly Diagram

There are 6 reserved screw holes for SOM-E780 to be pre-assembled with a heat spreader.

2.4 Assembly Diagram

To prevent damage to the 400-pin board-to-board connector for the COM-HPC, it's important to vertically assemble the module and carrier board and align them according to the specified angle demonstrated in the following figures.

Mating Angle Requirements:

2.4.1 Allowable Initial Angular Misalignment

TABLE 1	
ROW	"A"=DEG
4	9.05
6	5.84
8	4.63
10	3.56
16	2.22

TABLE 2			
NO OF POS	"B"=DEG	NO OF POS	"B"=DEG
10	11.97	60	2.37
20	6.88	70	2.00
30	4.82	80	1.71
40	3.63	90	1.49
50	2.88	100	1.31

TABLE 3			
NO OF POS	"C"=DEG	NO OF POS	"C"=DEG
10	3.69	60	1.46
20	2.82	70	1.30
30	2.29	80	1.17
40	1.92	90	1.07
50	1.66	100	0.98

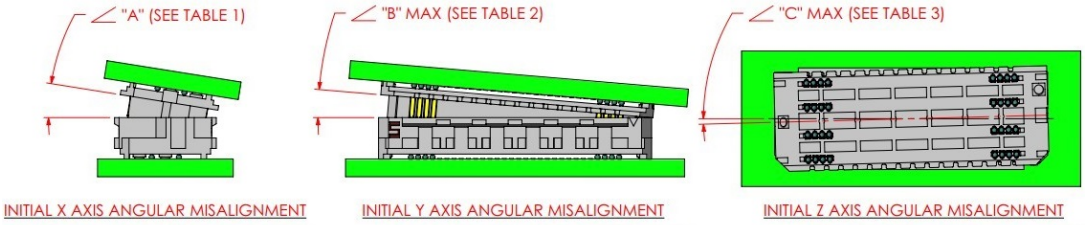


Figure 2.7 Initial Angular Misalignment

2.4.2 Allowable Final Angular Misalignment

TABLE 4	
ROW	"D"=DEG
4	3.95
6	2.56
8	1.89
10	1.50
16	0.92

TABLE 5			
NO OF POS	"E"=DEG	NO OF POS	"E"=DEG
10	3.30	60	0.79
20	2.02	70	0.69
30	1.46	80	0.61
40	1.14	90	0.54
50	0.93	100	0.49

TABLE 6			
NO OF POS	"F"=DEG	NO OF POS	"F"=DEG
10	1.12	60	0.27
20	0.69	70	0.23
30	0.50	80	0.21
40	0.39	90	0.19
50	0.32	100	0.17

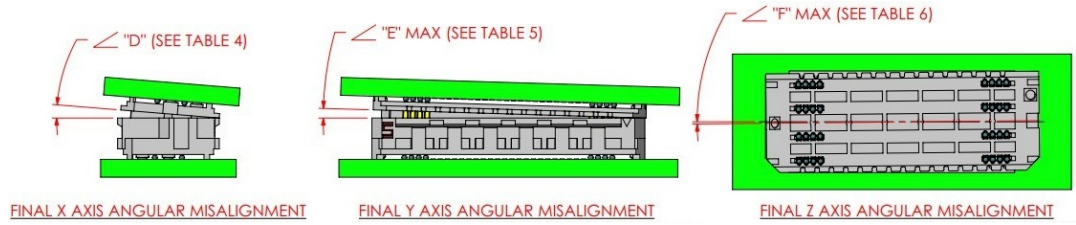


Figure 2.8 Final Angular Misalignment

2.5 CPU Package Design

Please consider the CPU and chip height tolerance when designing your thermal solution.

Table 2.1: CPU Package Design

Item	LGA
IHS to MB Height (validated range)	8.45 ~ 9.47 mm

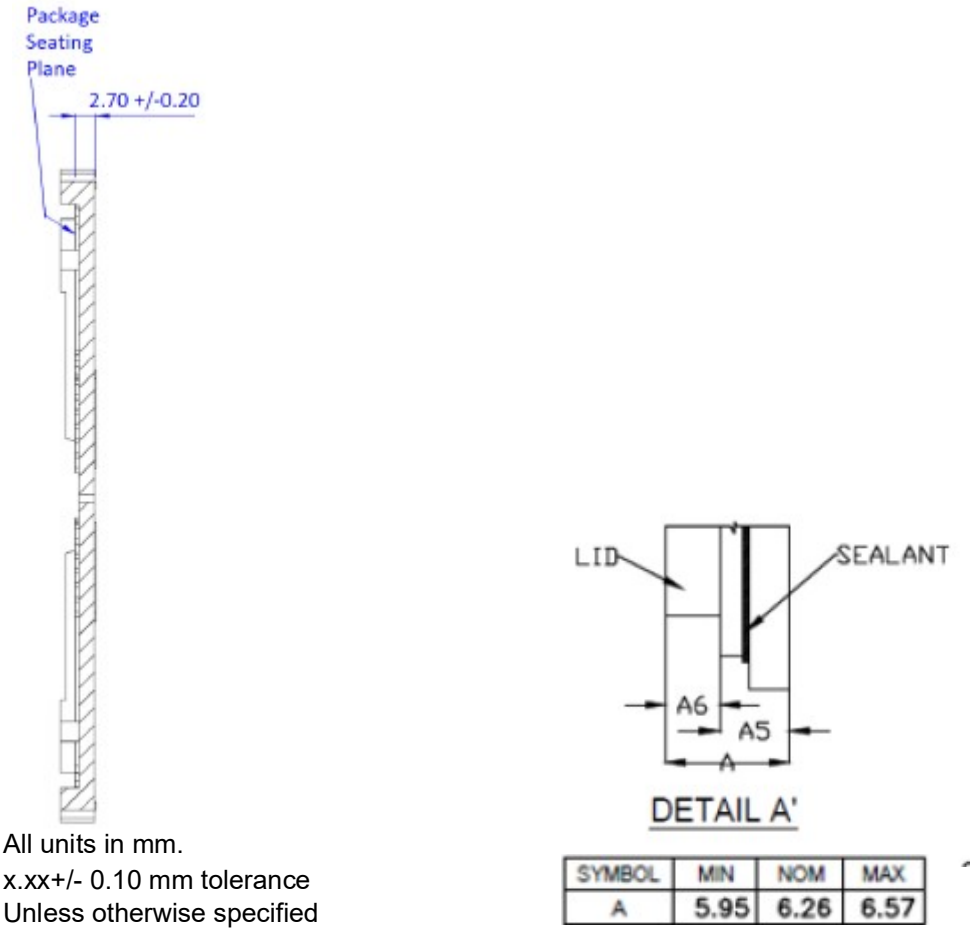


Figure 2.9 CPU and CPU Socket Height and Tolerance

Chapter 3

AMI BIOS

This chapter gives BIOS setup information for the SOM-E78 CPU Computer on Module.

Sections include:

- Introduction
- Entering Setup
- Hot/Operation Keys
- Exiting the BIOS Setup Utility

3.1 Introduction

With the AMI BIOS Setup Utility, users can modify BIOS settings and control various system features. This chapter describes the basic navigation of the BIOS Setup Utility.

Figure 3.1 Setup Program Initial Screen

AMI BIOS ROM has a built-in setup program that allows users to modify the basic system configuration. This information is stored in flash ROM so it retains the setup information when the power is turned off.

3.2 Entering Setup

Turn on the computer and then press <DEL> or <ESC> to enter the Setup menu.

3.2.1 Main Setup

Figure 3.2 Main Setup Screen

- **System Date**
  Set the Date. Use Tab to switch between Date elements.
  Default Ranges:
  Year: 1998-9999
  Months: 1-12
  Days: Dependent on month
  Range of Years may vary.
- **System Time**
  Set the Time. Use Tab to switch between Time elements.

3.2.2 Advanced BIOS Features Setup

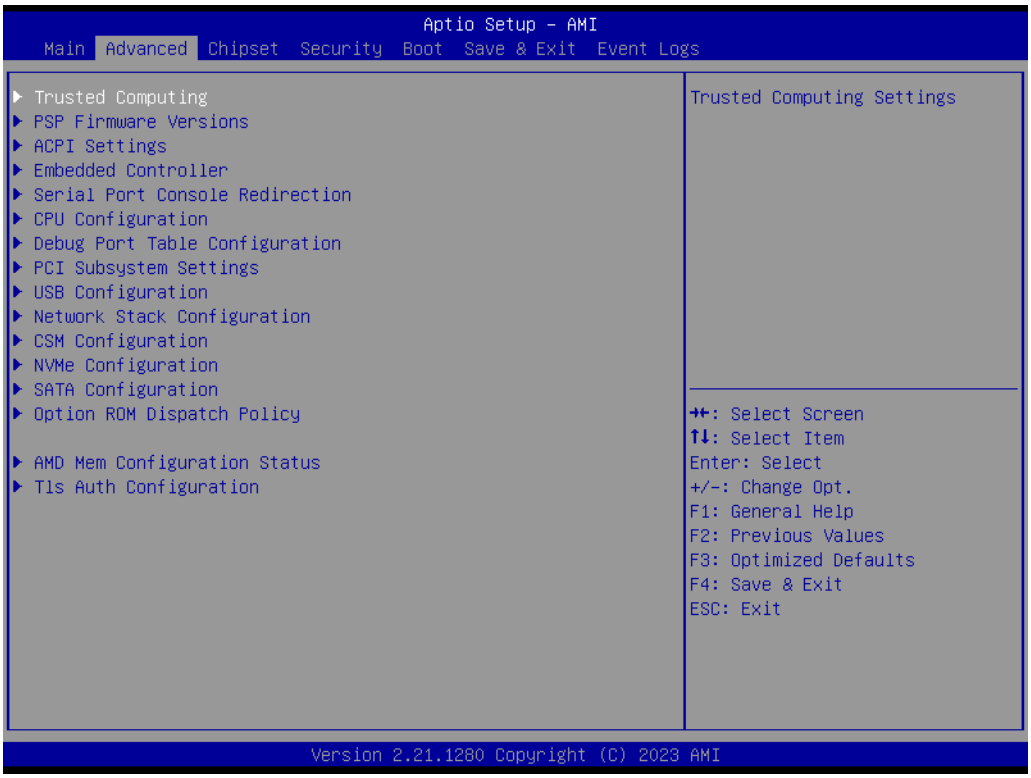


Figure 3.3 Advanced Features Setup Screen

3.2.2.1 Trusted Computing

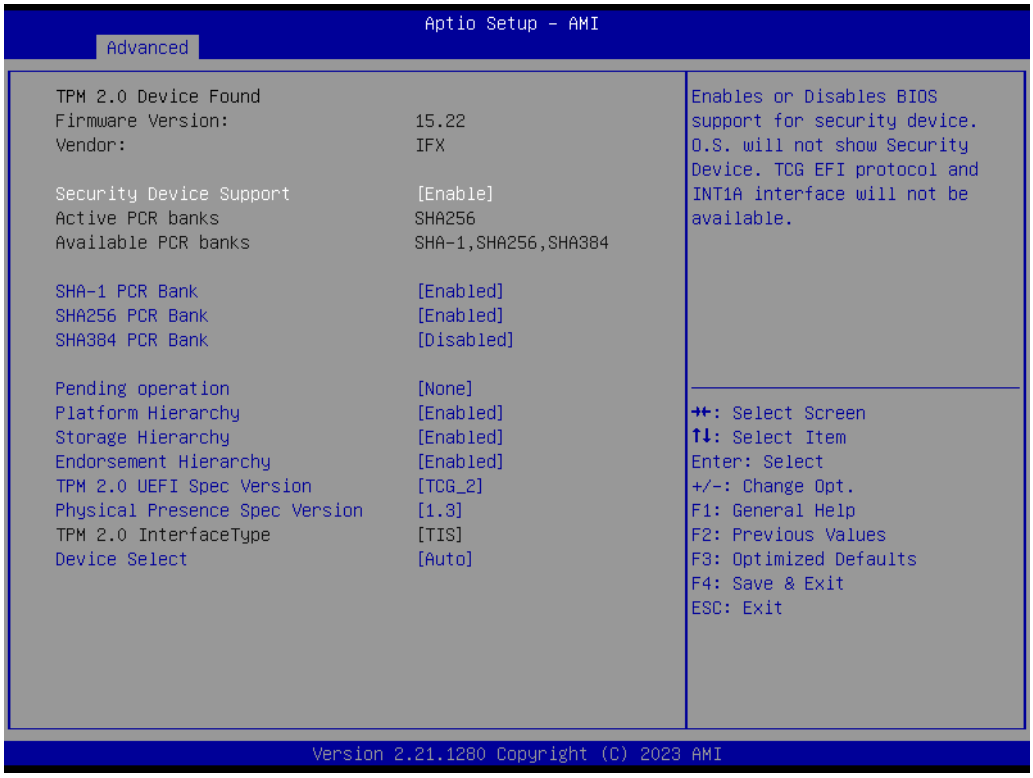


Figure 3.4 Trusted Computing

- **Security Device Support**
  Enables or disables BIOS support for a security device. The OS will not show security devices. TCG EFI protocol and INT1A interface will not be available.
- **SHA-1 PCR Bank**
  Enables or disables SHA-1 PCR bank.
- **SHA256 PCR Bank**
  Enables or disables SHA256 PCR bank
- **SHA384 PCR Bank**
  Enables or disables SHA384 PCR bank
- **Pending operation**
  Schedule an operation for the security device. Note: your computer will reboot during restart in order to change state of security device.
- **Platform Hierarchy**
  Enables or disables Platform Hierarchy.
- **Storage Hierarchy**
  Enables or disables Storage Hierarchy.
- **Endorsement Hierarchy**
  Enables or Disable Endorsement Hierarchy.
- **TPM 2.0 UEFI Spec Version**
  Enables or disables BIOS support for security device. The OS will not show security devices. TCG EFI protocol and INT1A interface will not be available.
- **Physical Presence Spec Version**
  Enables or disables BIOS support for security device. The OS will not show security devices. TCG EFI protocol and INT1A interface will not be available.
- **Device Select**
  Enables or disables BIOS support for security device. The OS will not show security devices. TCG EFI protocol and INT1A interface will not be available.

3.2.2.2 PSP Firmware Versions

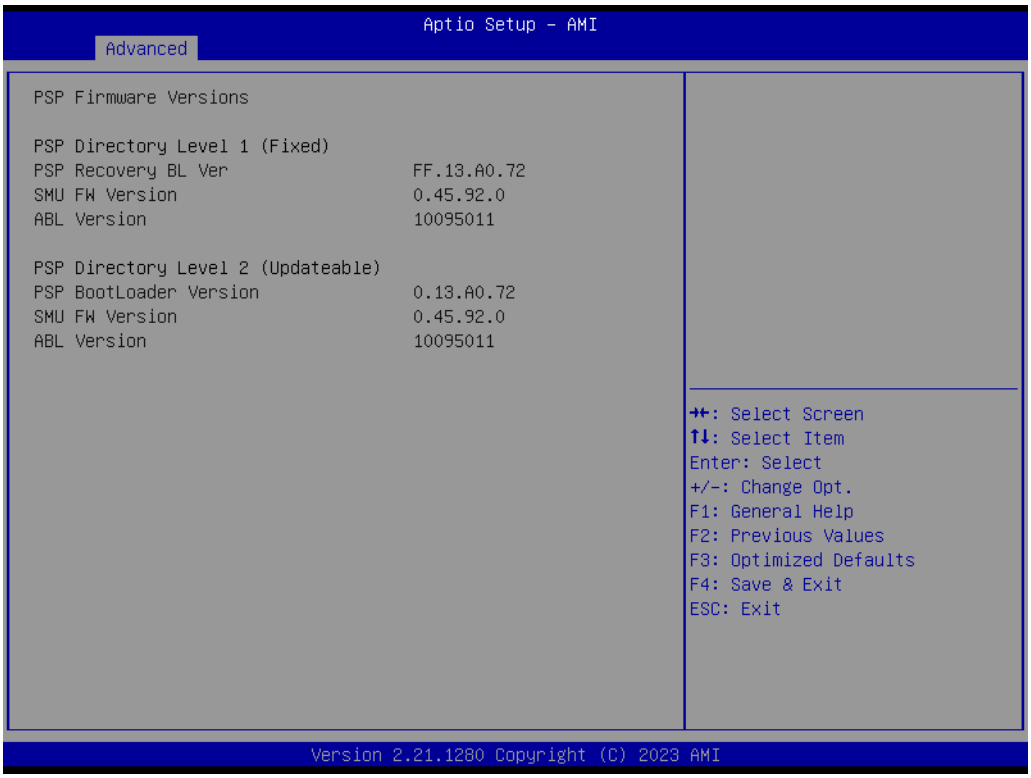


Figure 3.5 PSP Firmware Versions

3.2.2.3 ACPI Settings

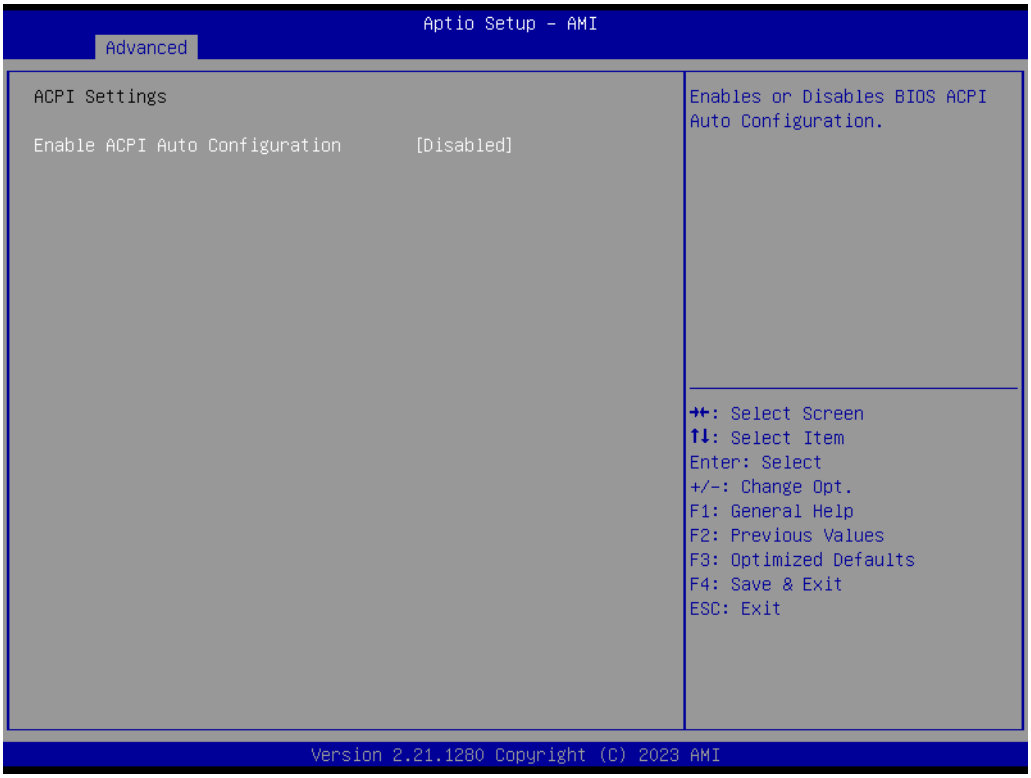


Figure 3.6 ACPI Settings

- **Enable ACPI Auto Configuration**
  Enables or disables BIOS ACPI auto configuration.

3.2.2.4 Embedded Controller

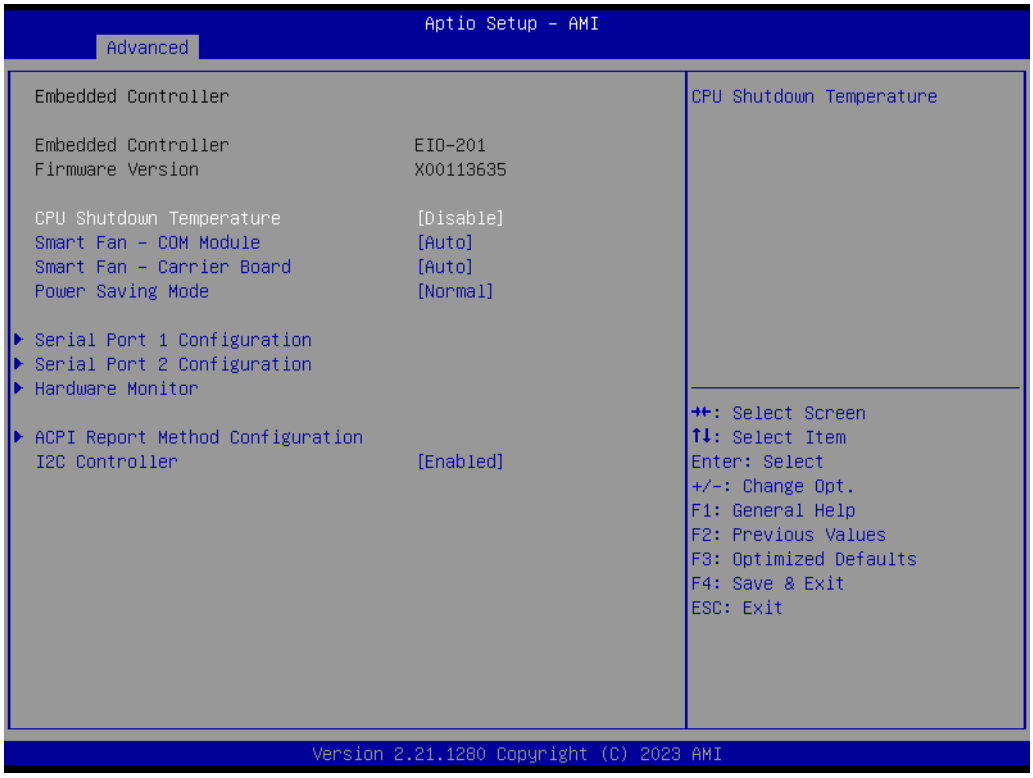


Figure 3.7 Embedded Controller

- **CPU Shutdown Temperature**
  CPU Shutdown Temperature.
- **Smart Fan - COM Module**
  Control COM Module Smart FAN function. Gets a value from EC and only sets a value when it Saves Changes.
- **Smart Fan - Carrier Board**
  Control Carrier Board Smart FAN function. Gets a value from EC and only sets a value when it Saves Changes.
- **Power Saving Mode**
  Select Power Saving Mode.
- **Serial Port 1 Configuration**
  Set parameters of Serial Port 1 (COMA).
- **Serial Port 2 Configuration**
  Set Parameter.
- **Hardware Monitors of Serial Port 2 (COMB)**
  Monitor hardware status.
- **ACPI Report Method Configuration**
  Select ACPI Reporting Method for EC devices.
- **I^2C Control**
  Enable/Disable I2C controller on RDC-IS200.

Serial Port 1 Configuration

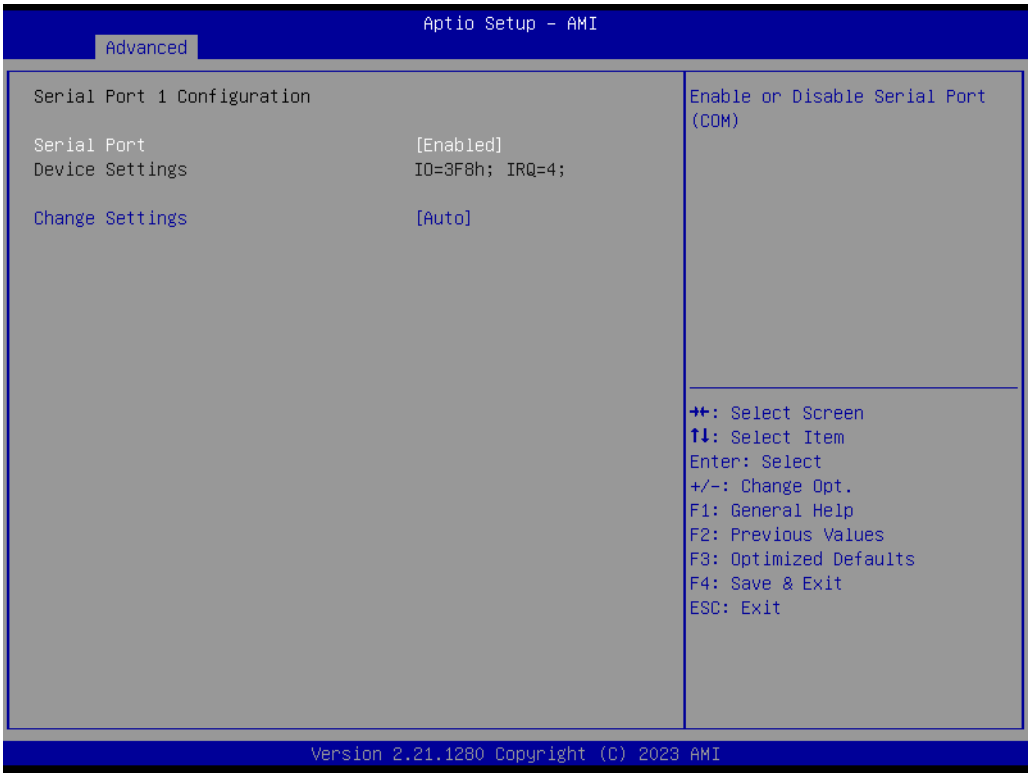


Figure 3.8 Serial Port 1 Configuration

- **Serial Port**
  Enable or disables Serial Port (COM).
- **Change Settings**
  Select an optimal settings for Super IO Device.

Serial Port 2 Configuration

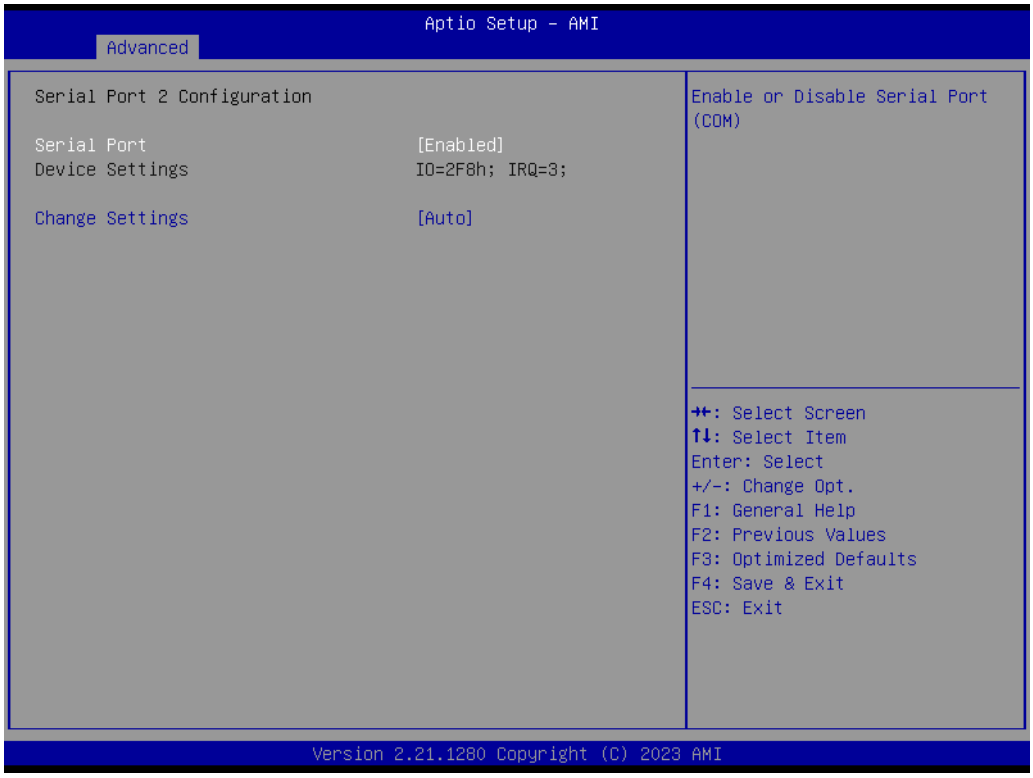


Figure 3.9 Serial Port 2 Configuration

- **Serial Port**
  Enable or disables Serial Port (COM).
- **Change Settings**
  Select an optimal settings for Super IO Device.

Hardware Monitor

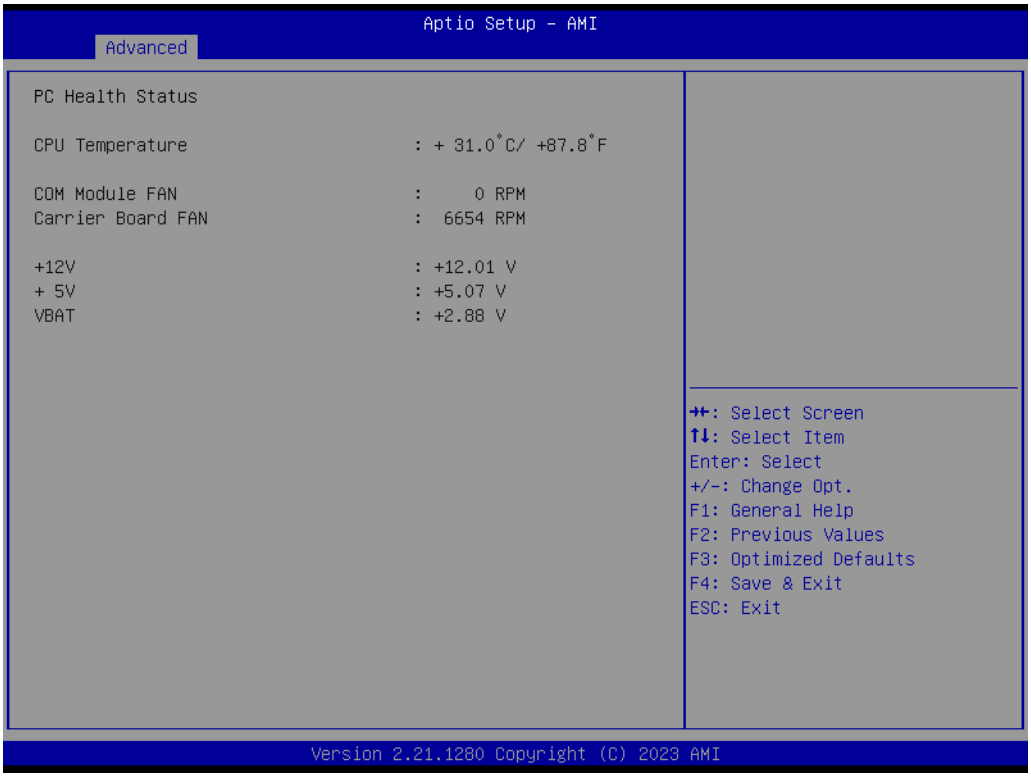


Figure 3.10 Hardware Monitor

ACPI Report Method Configuration

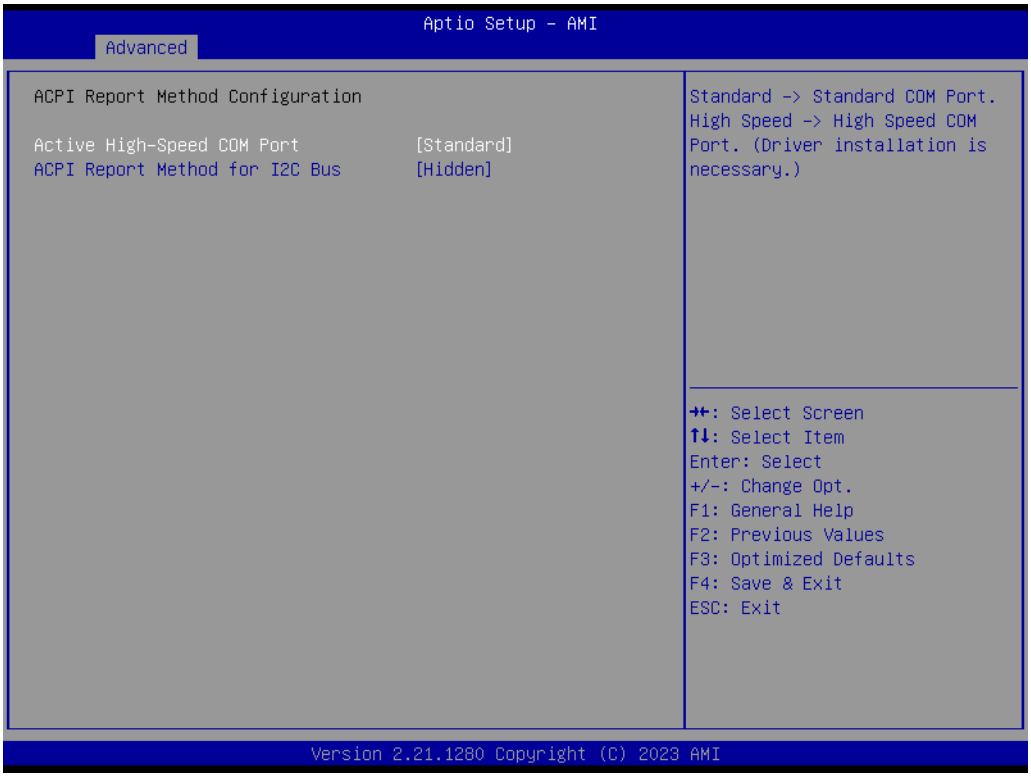


Figure 3.11 ACPI Report Method Configuration

3.2.2.5 Serial Port Console Redirection

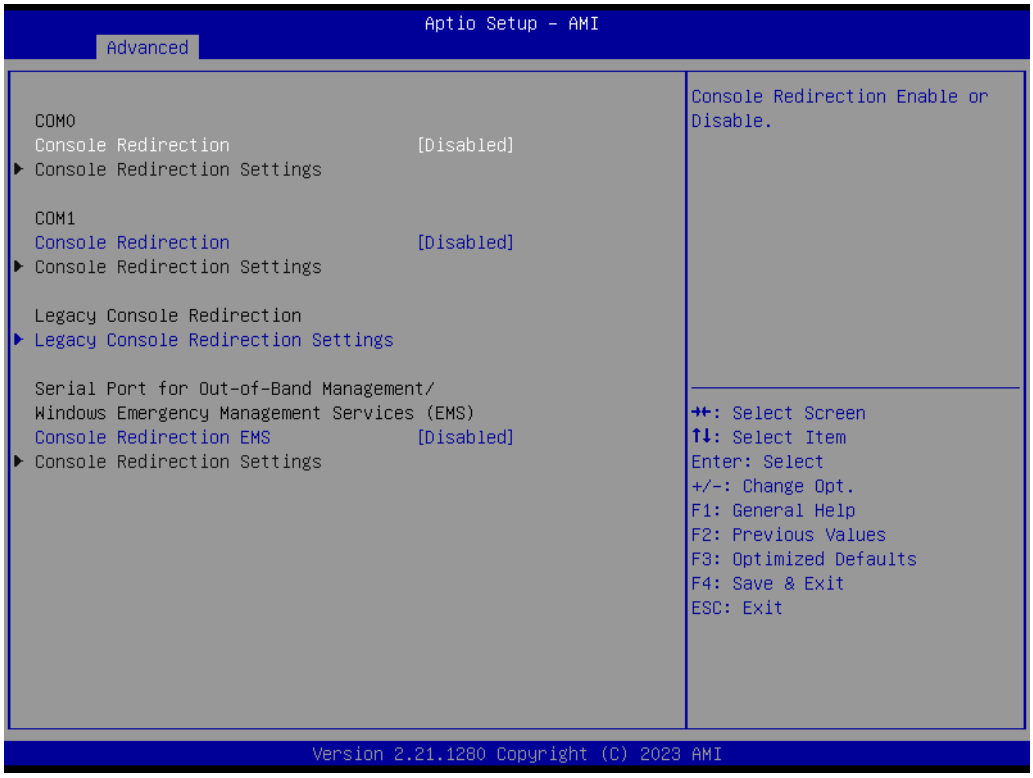


Figure 3.12 Serial Port Console Redirection

- **Console Redirection Settings**
  The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
- **COM1 Console Redirection**
  Console Redirection Enable or Disable.
- **Console Redirection Settings**
  The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
- **Legacy Console Redirection**
  Legacy Console Redirection Settings.
- **Legacy Console Redirection Settings**
  Legacy Console Redirection Settings.
- **Console Redirection EMS**
  Console Redirection enable or disable.
- **Console Redirection Settings**
  The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

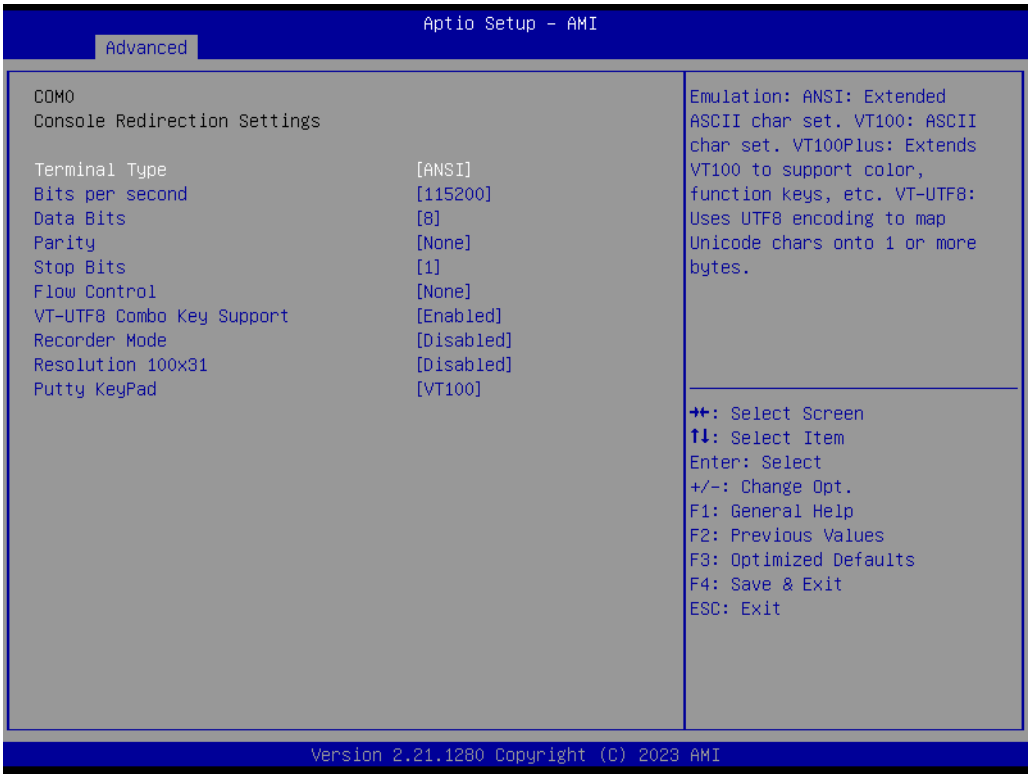


Figure 3.13 Console Redirection Settings

3.2.2.6 CPU Configuration

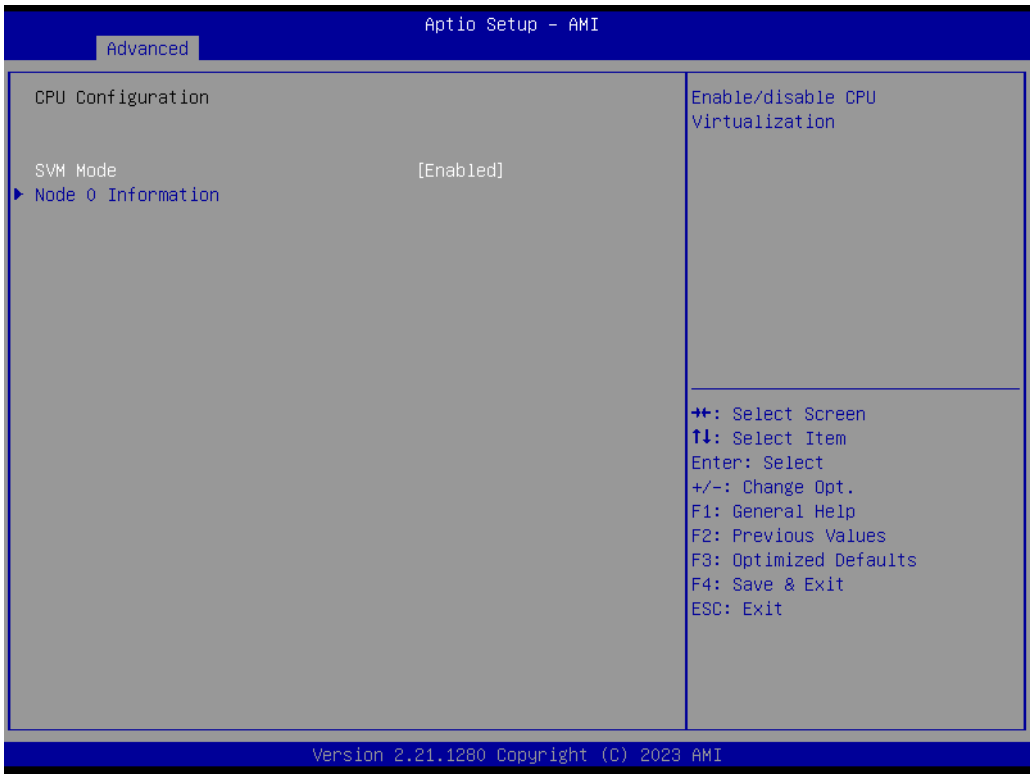


Figure 3.14 CPU Configuration

- **SVM Mode**
  Enable/disable CPU Virtualization.
- **Node 0 Information**
  View Memory Information related to Node 0.

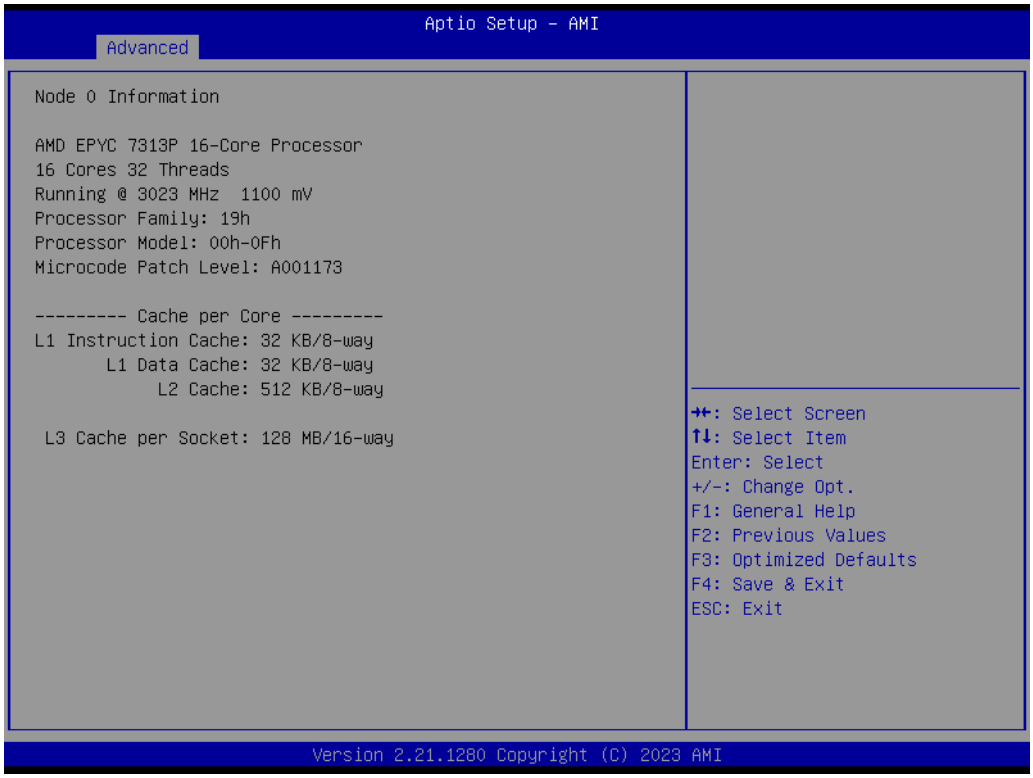


Figure 3.15 Nude 0 Information

3.2.2.7 Debug Port Table Configuration

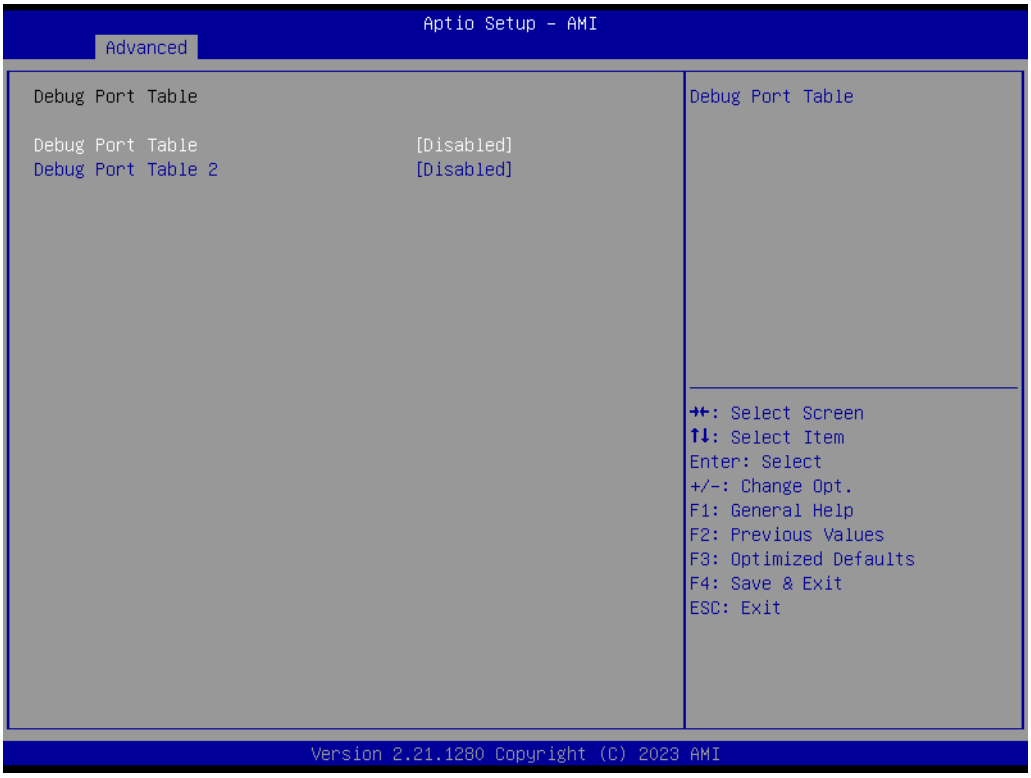


Figure 3.16 Debug Port Table Configuration

- **Debug Port Table**
  Debug Port Table.
- **Debug Port Table 2**
  Debug Port Table 2.

3.2.2.8 PCI Subsystem Settings

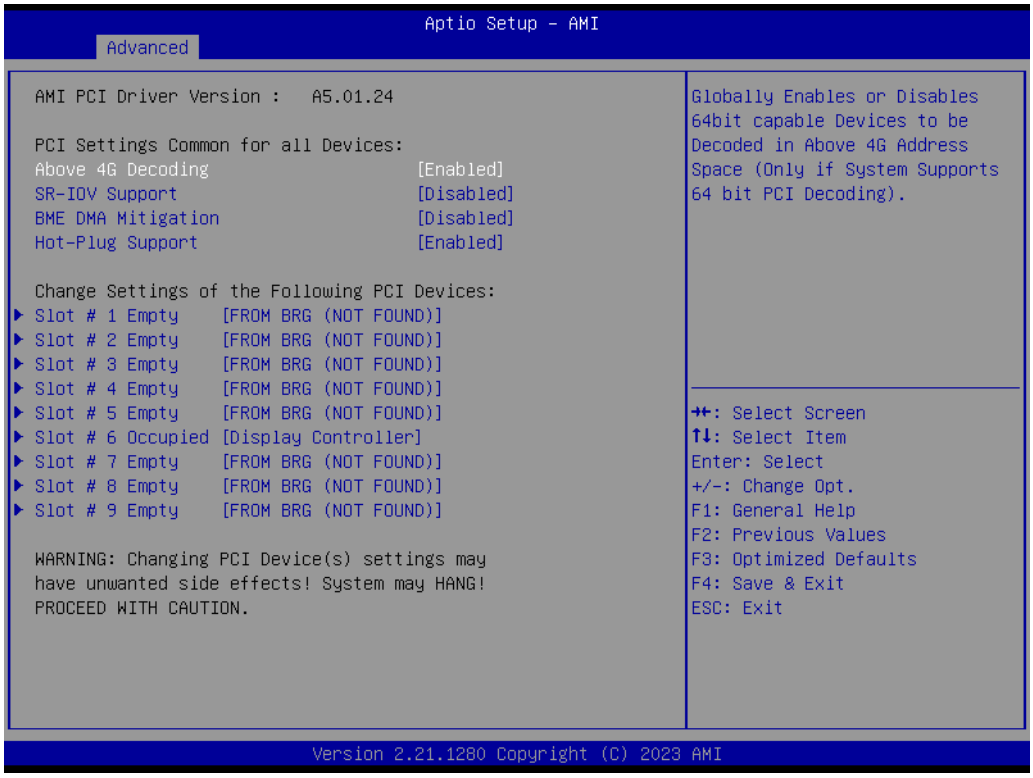


Figure 3.17 PCI Subsystem Settings

- **Above 4G Decoding**
  Globally enables or disables 64-bit-capable devices to be decoded in above 4G. address space (only if system supports 64-bit PCI decoding).
- **SR-IOV Support**
  If system has SR-IOV capable PCIe devices, this option enables or disables Single Root IO Virtualization support.
- **BME DMA Mitigation**
  Re-enable Bus Master Attribute disabled during PCI enumeration for PCI bridges after SMM Locked.
- **Hot-Plug Support**
  Globally enables or disables Hot-Plug for the entire system. If System has Hot-Plug capable slots and this option set to enabled, it provides a setup screen for selecting PCI resource padding for Hot-Plug.
- **Slot # 1 Occupied [Display Controller]**
  Change on Board PCI Device or PCI Slot Settings.
- **Slot # 2 Empty [From BRG (NOT FOUND)]**
  Change On Board PCI Device or PCI Slot Settings.
- **Slot # 3 Empty [From BRG (NOT FOUND)]**
  Change On Board PCI Device or PCI Slot Settings.
- **Slot # 4 Empty [From BRG (NOT FOUND)]**
  Change On Board PCI Device or PCI Slot Settings.
- **Slot # 5 Empty [From BRG (NOT FOUND)]**
  Change On Board PCI Device or PCI Slot Settings.
- **Slot # 6 Empty [From BRG (NOT FOUND)]**
  Change On Board PCI Device or PCI Slot Settings.
- **Slot # 7 Empty [From BRG (NOT FOUND)]**
  Change On Board PCI Device or PCI Slot Settings.

- **Slot # 8 Empty [From BRG (NOT FOUND)]**
  Change On Board PCI Device or PCI Slot Settings.
- **Slot # 9 Empty [From BRG (NOT FOUND)]**
  Change On Board PCI Device or PCI Slot Settings.

3.2.2.9 USB Configuration

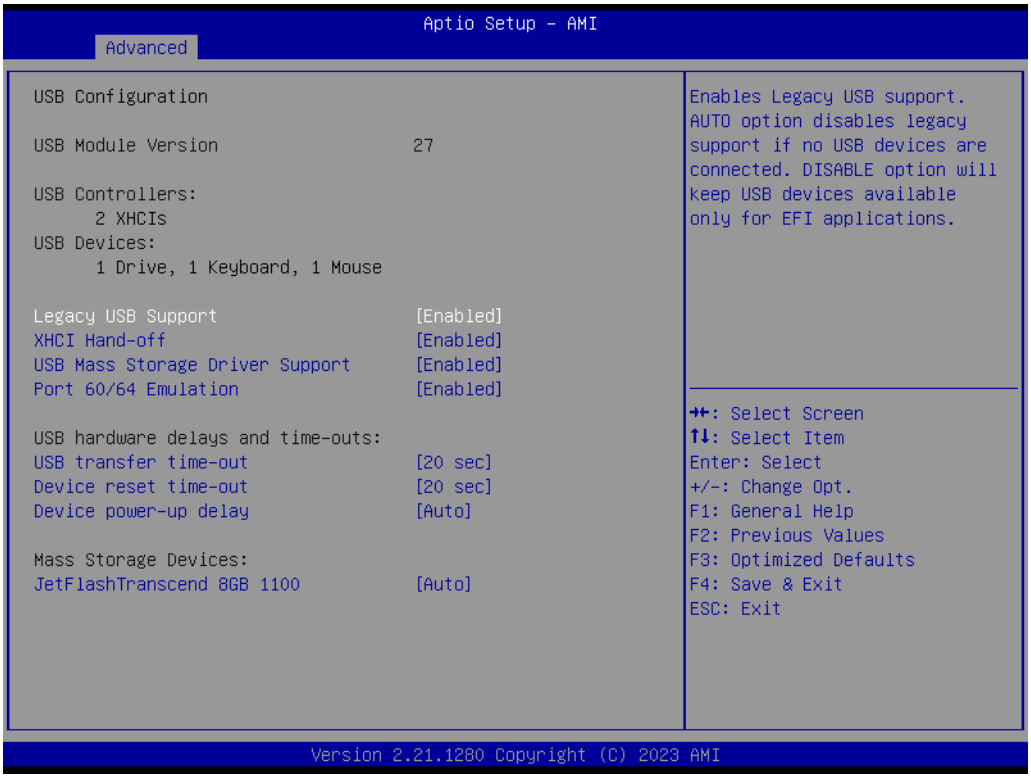


Figure 3.18 USB Configuration

- **Legacy USB Support**
  Enables Legacy USB support. The AUTO option disables legacy support if no USB devices are connected. The Disable option will keep USB devices available only for EFI applications.
- **XHCI Hand-off**
  This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
- **USB Mass Storage Driver Support**
  Enable/Disable USB Mass Storage Driver Support.
- **Port 60/64 Emulation**
  Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OS.
- **USB transfer time-out**
  The time-out value for control, bulk, and interrupt transfers.
- **Device reset time-out**
  USB mass storage device start unit command time-out.
- **Device power-up delay**
  Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses the default value: for a Root port it is 100 ms, for a Hub port the delay is taken from the Hub descriptor.

3.2.2.10 Network Stack Configuration

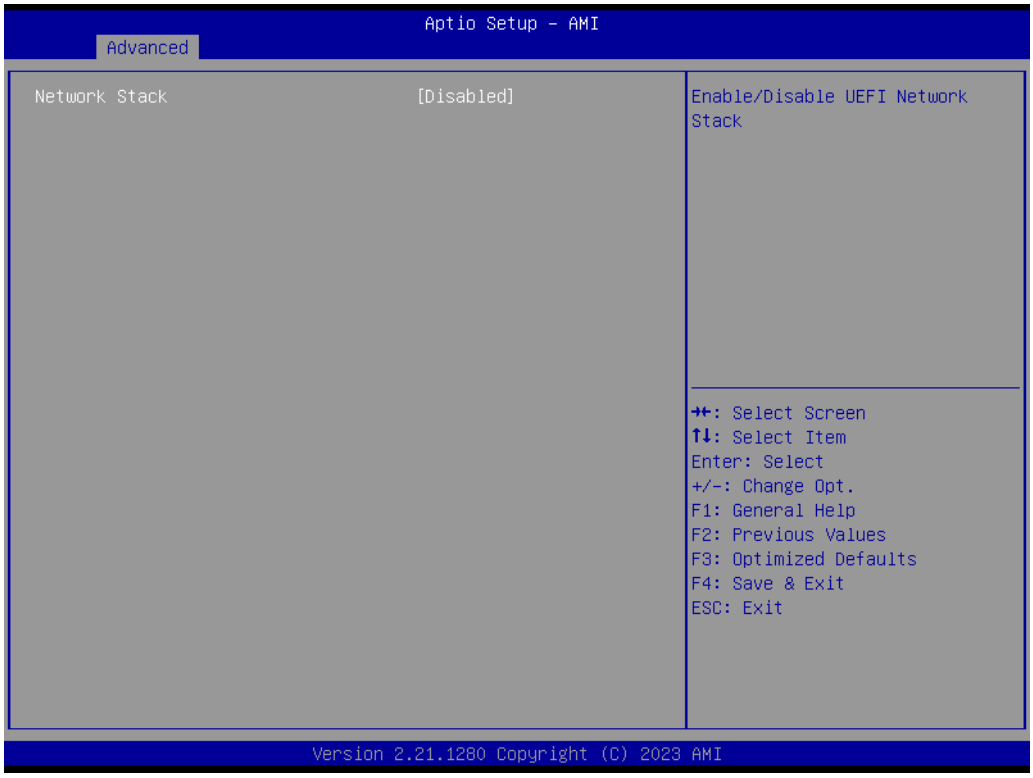


Figure 3.19 Network Stack Configuration

- **Network Stack**
  Enable/disable UEFI Network Stack.

3.2.2.11 CSM Configuration

Figure 3.20 CSM Configuration

- **CSM Support**
  Enable/disable CSM support.
- **GateA20 Active**
  Upon request, GA20 can be disabled using BIOS services. However, it is not advisable to disable GA20, except when executing real-time code above 1MB.
- **INT19 Trap Response**
  When an Option ROM traps INT19, the BIOS can respond in two ways: IMMEDIATE - executing the trap immediately, or POSTPONED - executing the trap during legacy boot.
- **Boot option filter**
  This option controls Legacy/UEFI ROMs priority.

3.2.2.12 NVMe Configuration

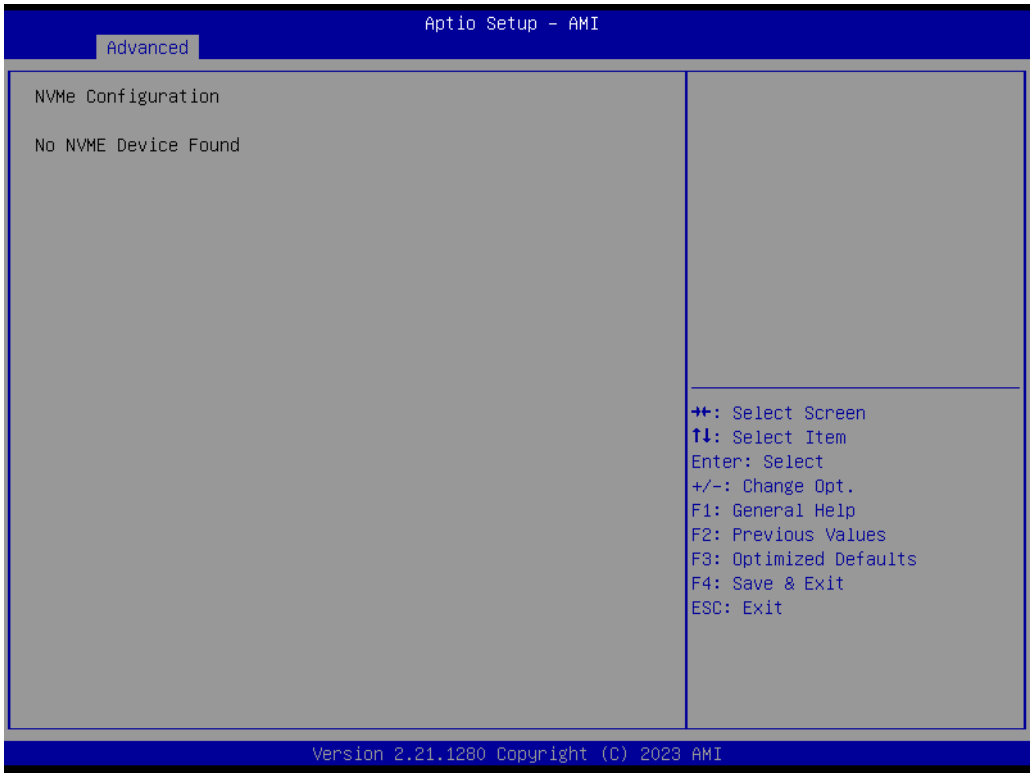


Figure 3.21 NVMe Configuration

3.2.2.13 SATA Configuration

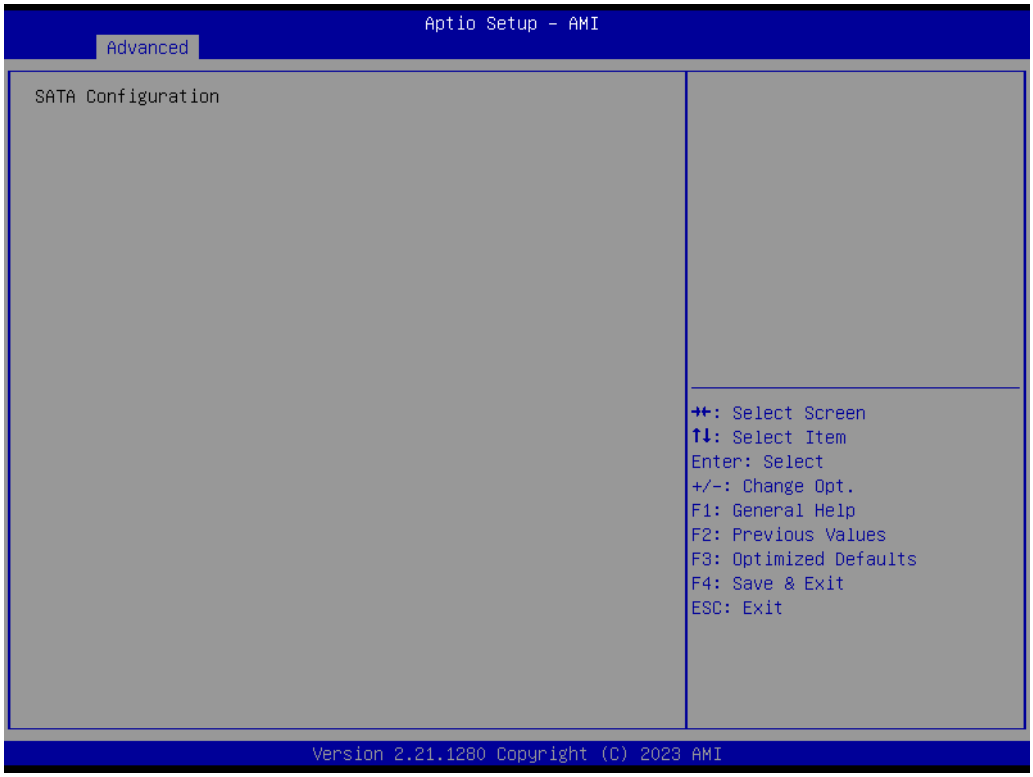


Figure 3.22 NVMe Configuration

3.2.2.14 Option ROM Dispatch Policy

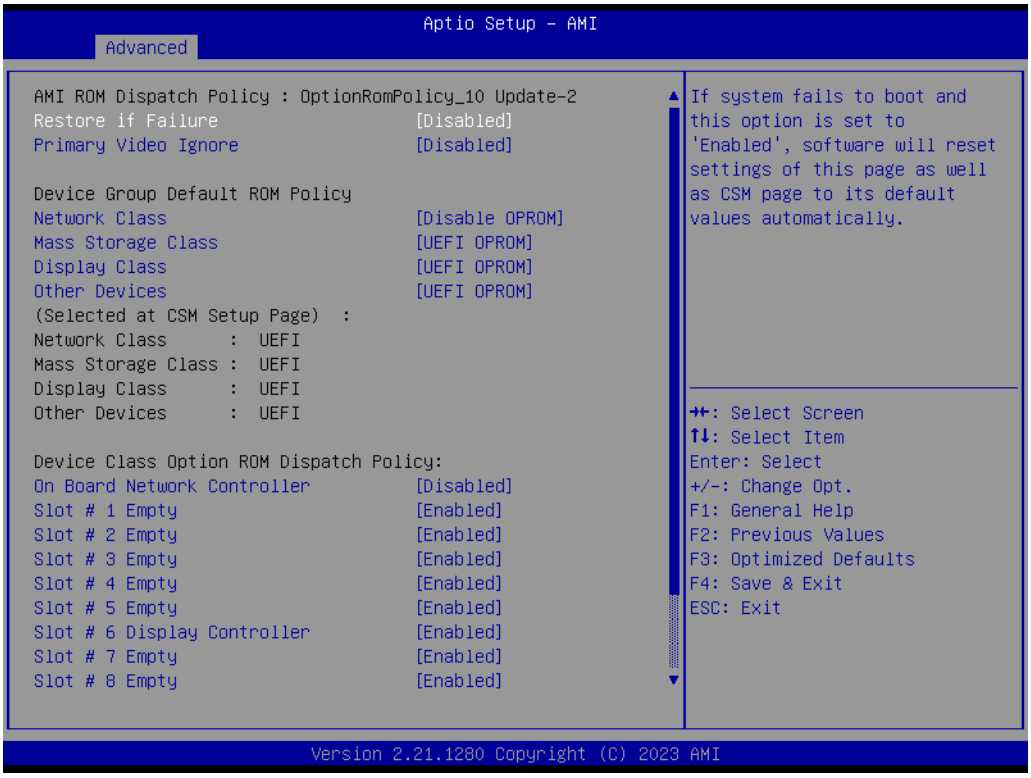


Figure 3.23 Option ROM Dispatch Policy

- **Restore if Failure**
  If system fails to boot and this option is set to ‘Enabled’, the software will reset settings of this page as well as the CSM page to its default values automatically.
- **Primary Video Ignore**
  If the software detects that the Option ROM of the Primary Video Device won't dispatch due to the Policy settings, it will disregard these settings and automatically restore the device to 'Enable'.
- **Network Class**
  Controls the execution of UEFI and Legacy Network OpROM.
- **Mass Storage Class**
  Controls the execution of UEFI and Legacy Storage OpROM.
- **Display Class**
  Controls the execution of UEFI and Legacy Video OpROM.
- **Other Devices**
  Determines OpROM execution policy for devices other than network, storage, or video.
- **On Board Network Controller**
  Onboard Device has:
  UEFI [X]
  Legacy [X]
  Option ROM(s)

  VIDx8086;DIDx15F2?Class: 2/0/0

  @ Sx0|BxC1|Dx0|Fx0
  t: 2Sx0|BxC0|Dx1|Fx1
  t: 1Sx0|BxC0|Dx0|Fx0

AslName:I225
SMBIOS:I225 (G0)

- **Slot # 1 Display Controller**
  Device on Slot has:
  UEFI [X]
  Legacy [X]
  Option ROM(s)

  VIDx10DE?DIDx128B?Class: 3/0/0

  @ Sx0|BxC2|Dx0|Fx0
  t: 2Sx0|BxC0|Dx3|Fx1
  t: 1Sx0|BxC0|Dx0|Fx0
  AslName:
  SMBIOS:PCIEX16_2 (P0)
- **Slot # 2 Empty**
  Enable or Disable Option ROM execution for selected Slot.
- **Slot # 3 Empty**
  Enable or Disable Option ROM execution for selected Slot.
- **Slot # 4 Empty**
  Enable or Disable Option ROM execution for selected Slot.
- **Slot # 5 Empty**
  Enable or Disable Option ROM execution for selected Slot.
- **Slot # 6 Empty**
  Enable or Disable Option ROM execution for selected Slot.
- **Slot # 7 Empty**
  Enable or Disable Option ROM execution for selected Slot.
- **Slot # 8 Empty**
  Enable or Disable Option ROM execution for selected Slot.
- **Slot # 9 Empty**
  Enable or Disable Option ROM execution for selected Slot.

3.2.2.15 AMD Mem Configuration Status

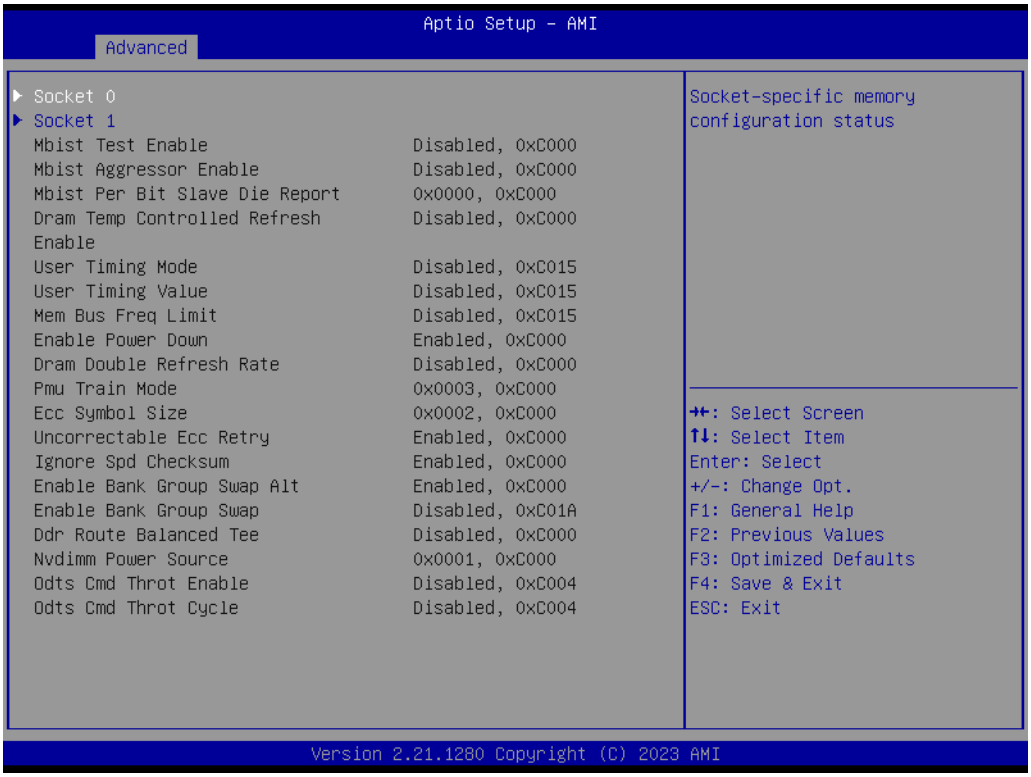


Figure 3.24 AMD Mem Configuration Status

- **Socket 0**
  Socket-specific memory configuration status.
- **Socket 1**
  Socket-specific memory configuration status.

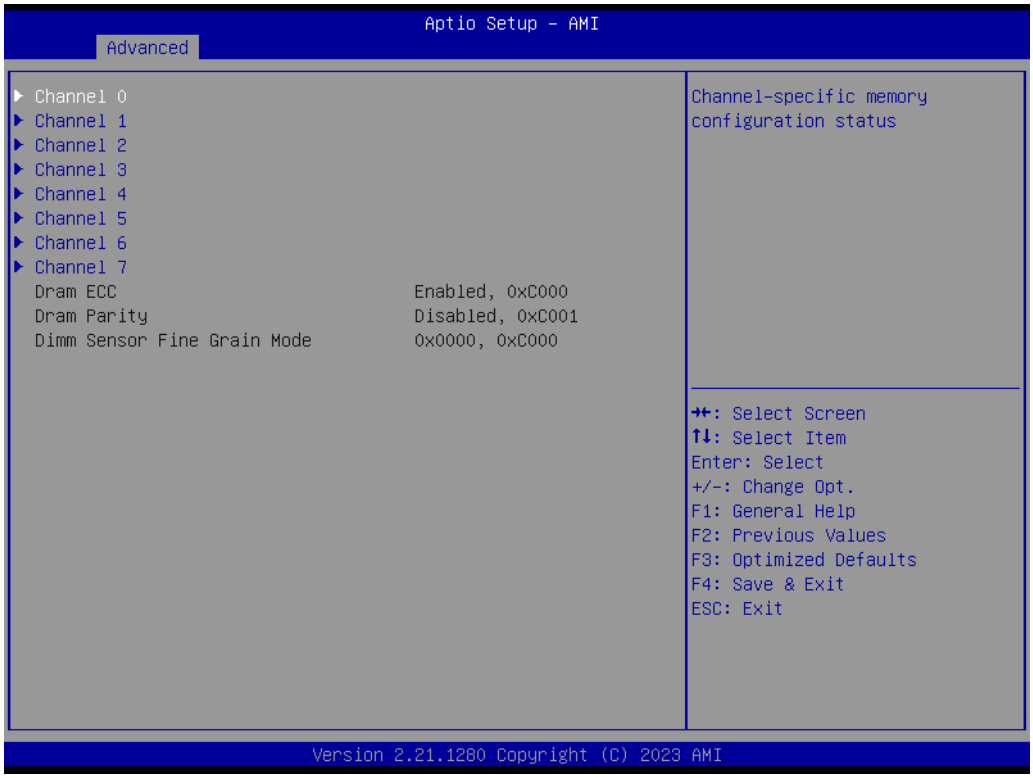


Figure 3.25 Socket 0

- **Channel 0**
  Channel-specific memory configuration status.
- **Channel 1**
  Channel-specific memory configuration status.
- **Channel 2**
  Channel-specific memory configuration status.
- **Channel 3**
  Channel-specific memory configuration status.
- **Channel 4**
  Channel-specific memory configuration status.
- **Channel 5**
  Channel-specific memory configuration status.
- **Channel 6**
  Channel-specific memory configuration status.
- **Channel 7**
  Channel-specific memory configuration status.

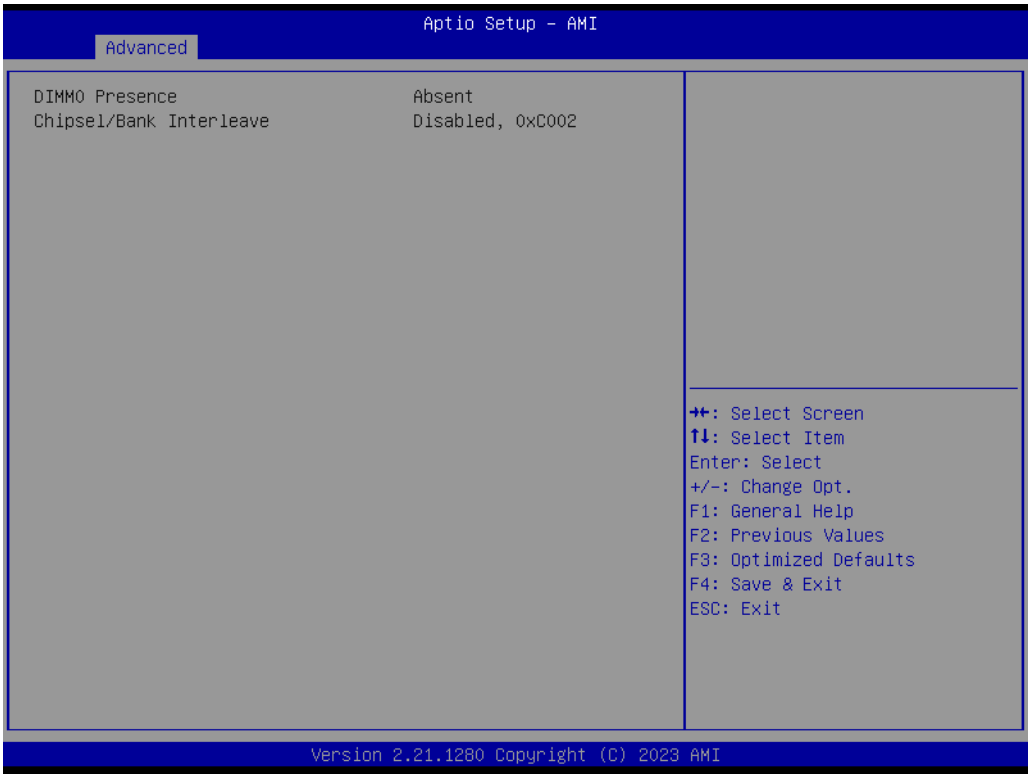


Figure 3.26 Channel 0

3.2.2.16 Tls Auth Configuration

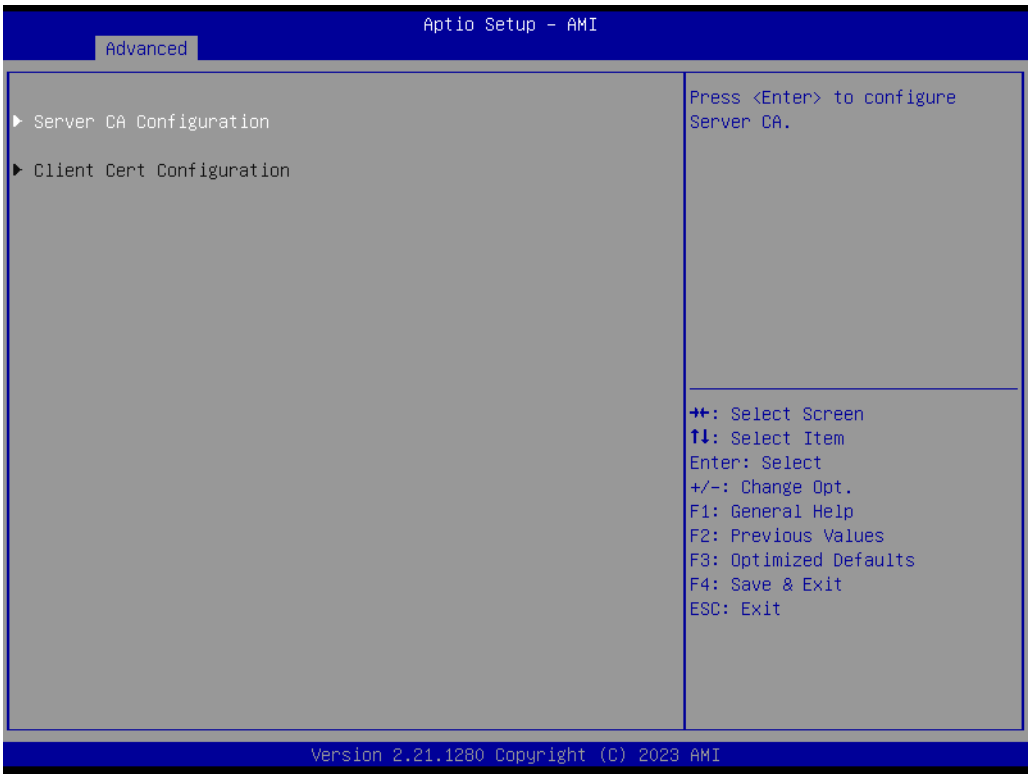


Figure 3.27 Tls Auth Configuration

- **Server CA Configuration**
  Press <Enter> to configure Server CA.

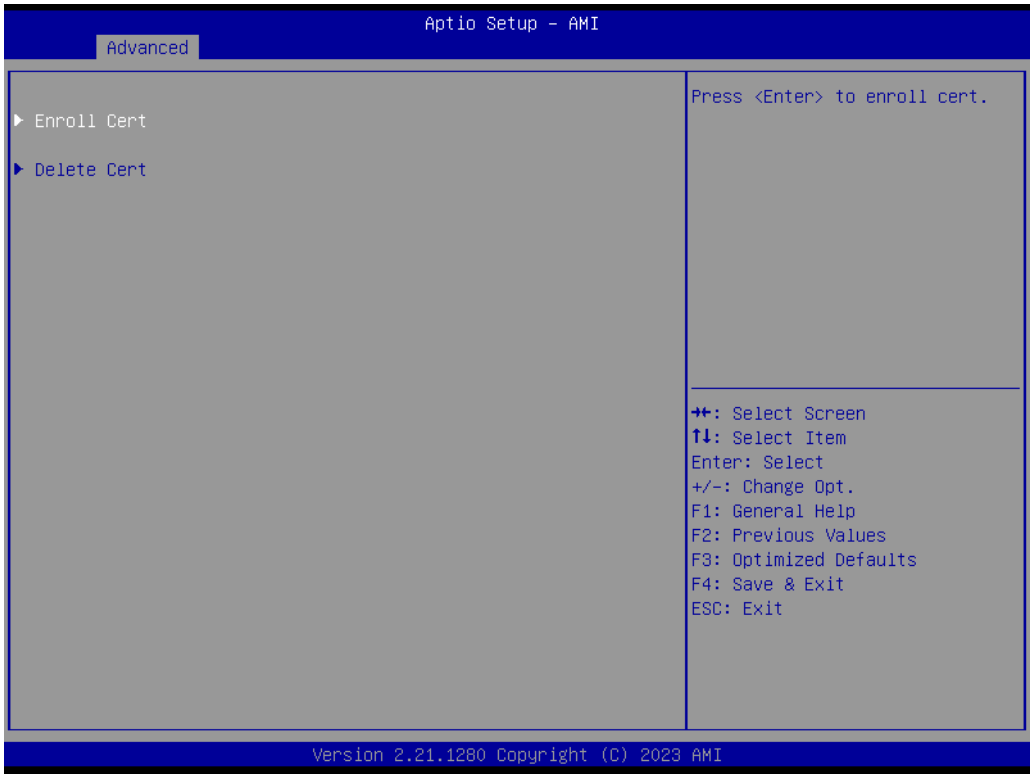


Figure 3.28 Server CA Configuration

- **Enroll Cert**
  Press <Enter> to enroll cert.
- **Delete Cert**
  Press <Enter> to delete cert.

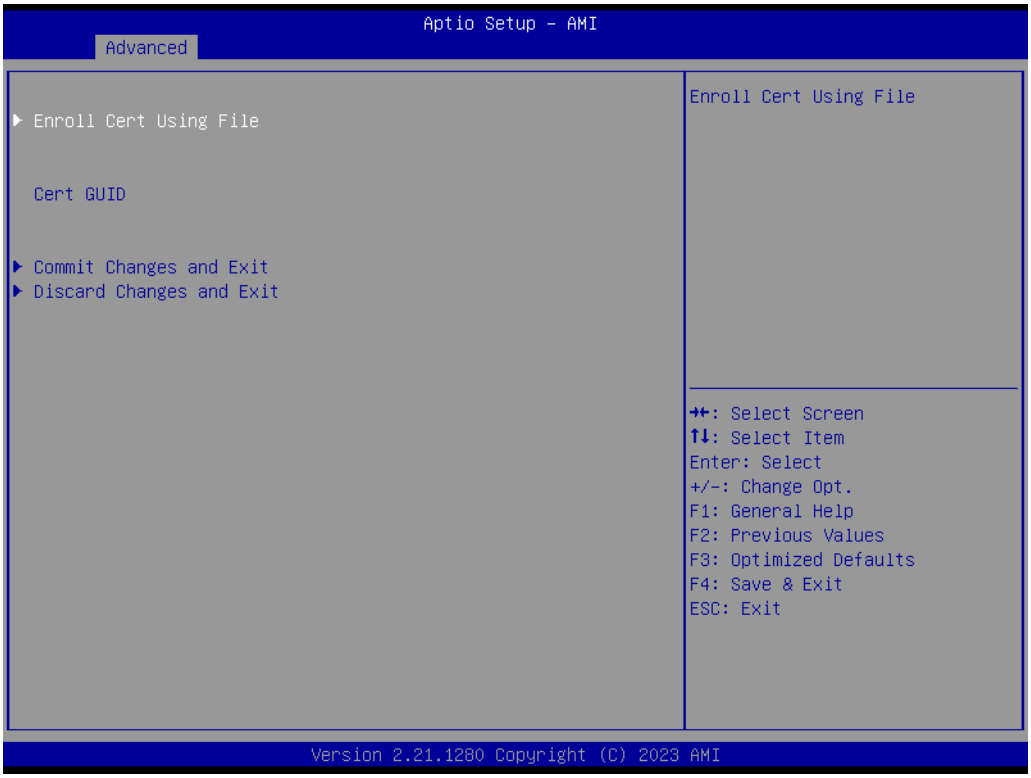


Figure 3.29 Enroll Cert

- **Enroll Cert Using File**
  Enroll Cert Using File.
- **Cert GUID**
  Input digit character in 11111111-2222-3333-4444-1234567890ab format.
- **Commit Changes and Exit**
  Commit Changes and Exit.
- **Discard Changes and Exit**
  Discard Changes and Exit.

3.2.3 Chipset Setup

Figure 3.30 Chipset Setup

- **PCIe Link Training Type**
  PCIe Link training in 1 or 2 steps.
- **PCIe Compliance Mode**
  PCIe Link Compliance Mode.
- **South Bridge**
  South Bridge Parameters.
- **CRB Board**
  CRB Board Parameters.
- **AMD PBS**
  AMD PBS Setup Page.
- **AMD CBS**
  AMD CBS Setup Page.
- **North Bridge**
  North Bridge Parameters.

3.2.3.1 South Bridge

Figure 3.31 South Bridge

- **SB Debug Configuration**
  Options For SB Debug Features.

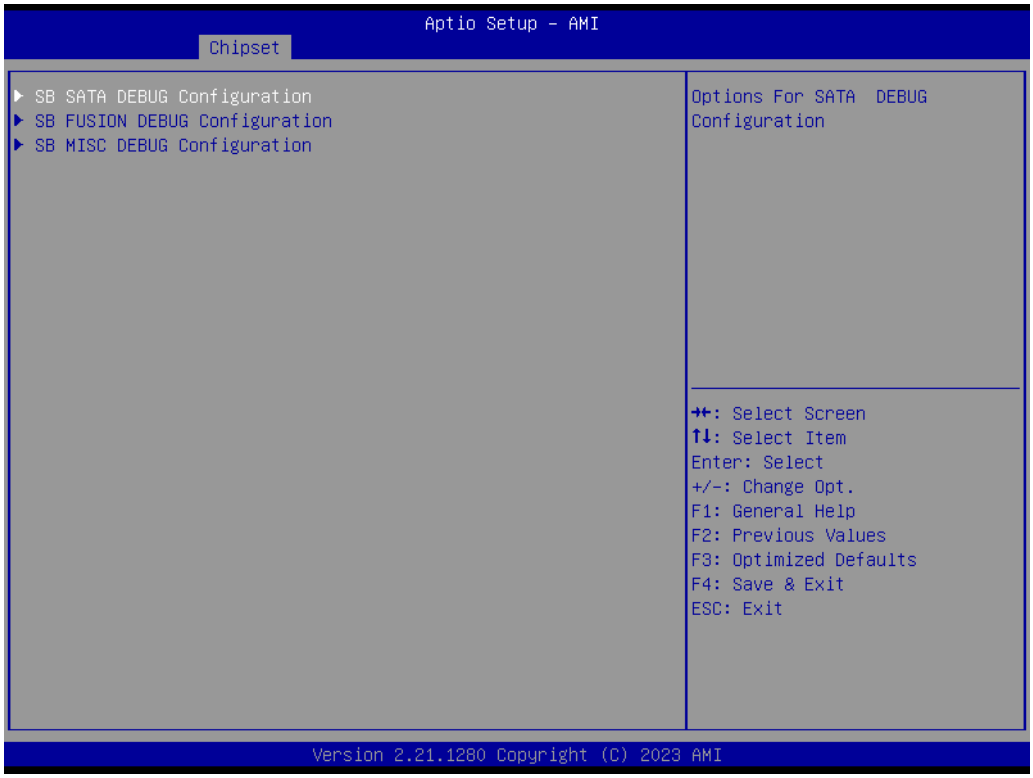


Figure 3.32 SB Debug Configuration

- **SB SATA DEBUG Configuration**
  Options For SATA DEBUG Configuration.
- **SB FUSION DEBUG Configuration**
  Options For SB FUSION DEBUG Configuration.
- **SB MISC DEBUG Configuration**
  Options For SB DEBUG Configuration.

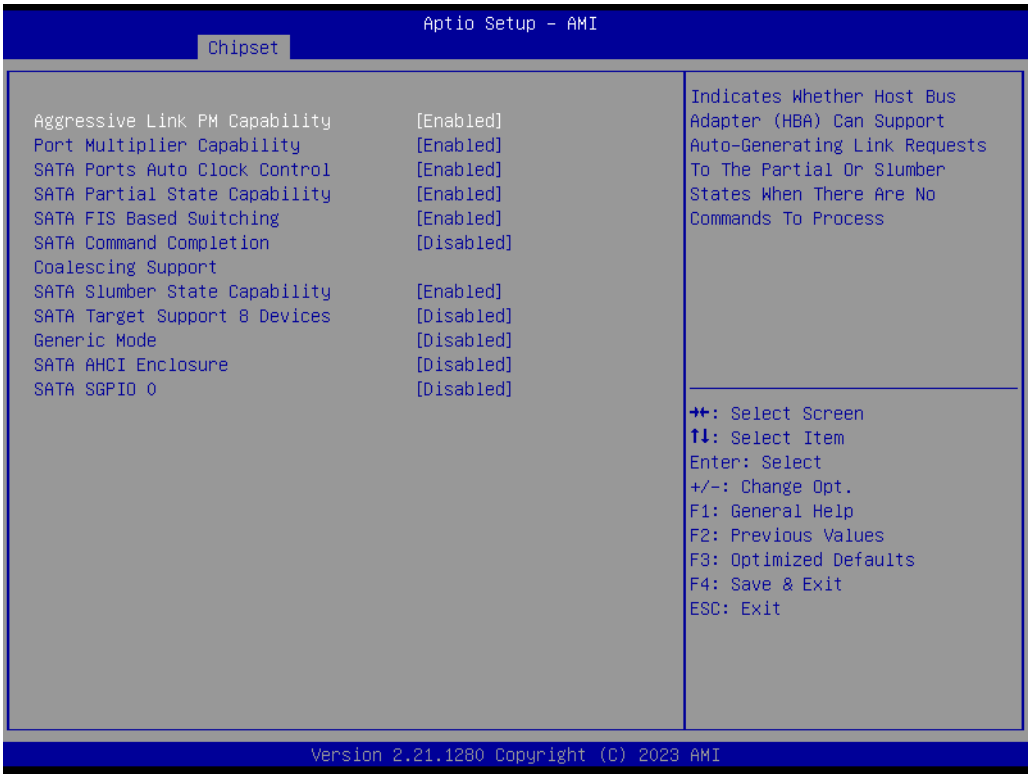


Figure 3.33 SB SATA DEBUG Configuration

- **Aggressive Link PM Capability**
  Indicates whether the Host Bus Adapter (HBA) can support auto-generating link requests to the partial or slumber states when there are no commands to process.
- **Port Multiplier Capability**
  Indicates whether the Host Bus Adapter (HBA) can support an A port multiplier.
- **SATA Ports Auto Clock Control**
  Enable/disable SATA Ports Auto Clock Control.
- **SATA Partial State Capability**
  Indicates whether the SATA Host BUS Adapter (HBA) can support transitions to the partial state.
- **SATA FIS Based Switching**
  Indicates whether the SATA Host BUS Adapter (HBA) can support port multiplier FIS-based switching.
- **SATA Command Completion Coalescing Support**
  Indicates whether the SATA Host BUS Adapter (HBA) can support Command Completion Coalescing.
- **SATA Slumber State Capability**
  Indicates whether the SATA Host BUS Adapter (HBA) can support transitions to the Slumber State.
- **SATA Target Support 8 Devices**
  Indicates whether the SATA Target Supports 8 Devices functions.
- **Generic Mode**
  SATA disables Generic Mode.
- **SATA AHCI Enclosure**
  SATA AHCI Enclosure management.
- **SATA SGPIO 0**
  Enable/disable SATA serial general purpose input/output (SGPIO) 0.

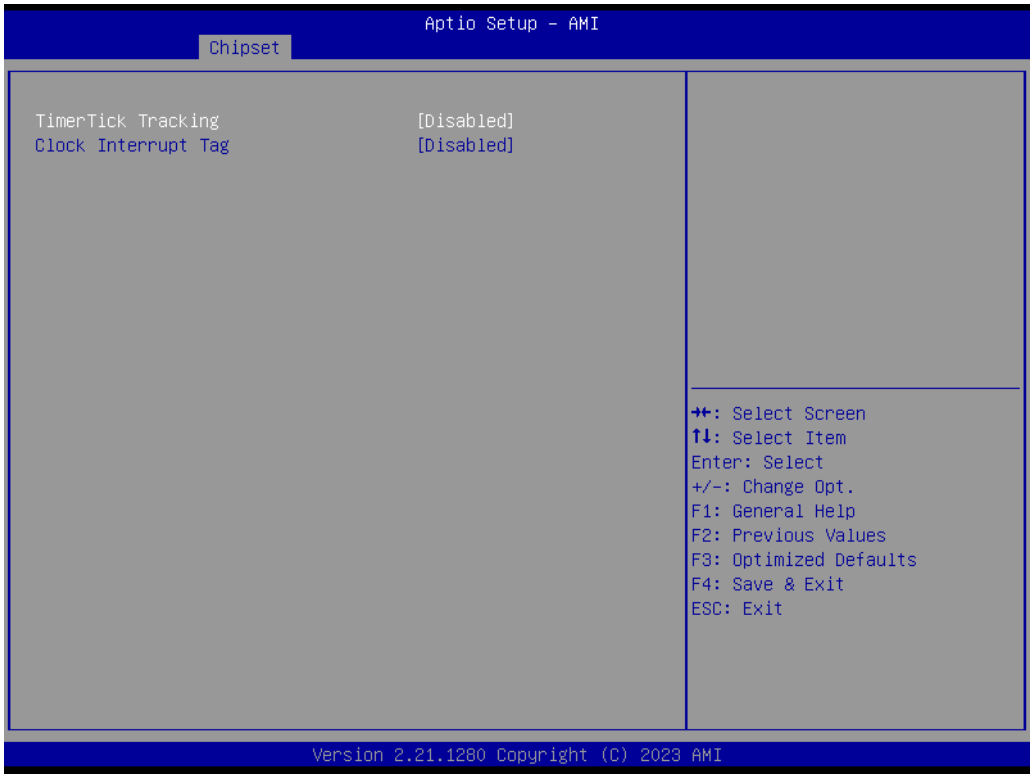


Figure 3.34 SB FUSION DEBUG Configuration

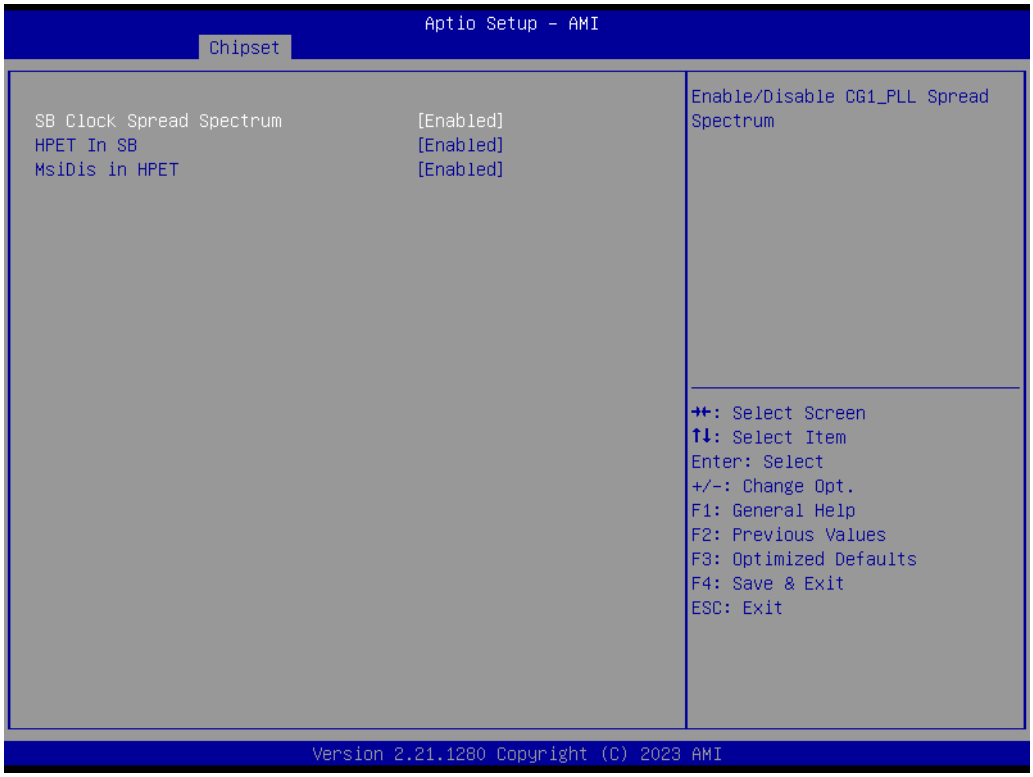


Figure 3.35 SB MISC DEBUG Configuration

- **SB Clock Spread Spectrum**
  Enable/disable CG1_PLL Spread Spectrum.
- **HPET In SB**
  PET function switch.

- **MsiDis in HPET**
  Expose MSI capability in HPET capability register.

3.2.3.2 CRB Board

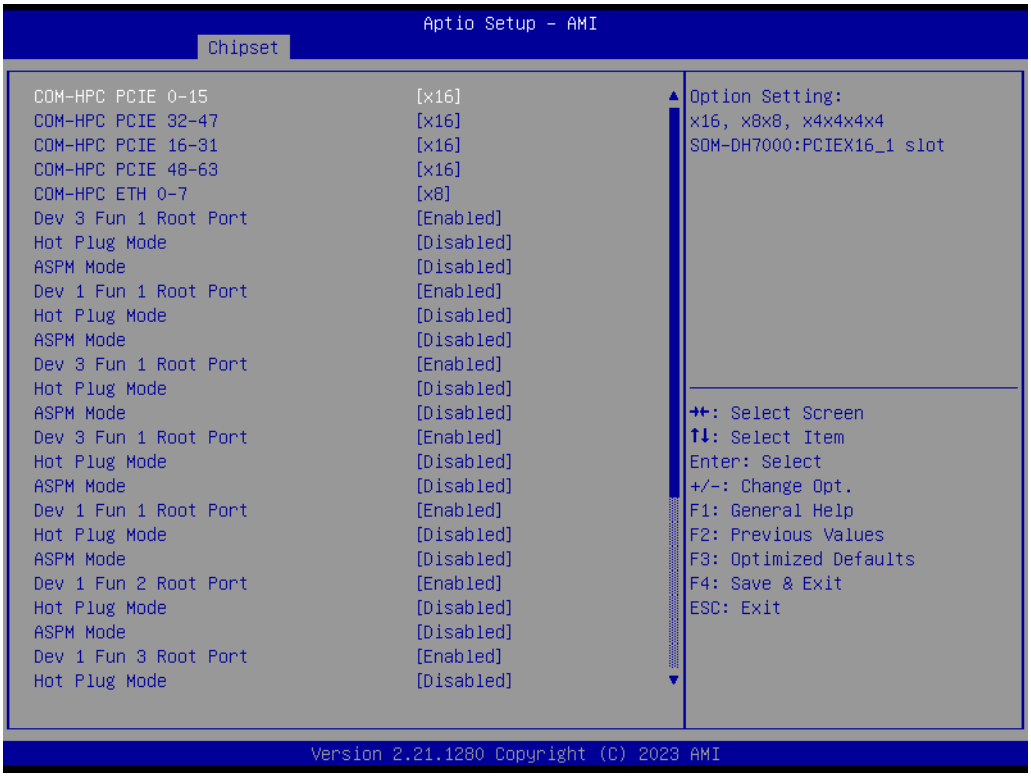


Figure 3.36 CRB Board

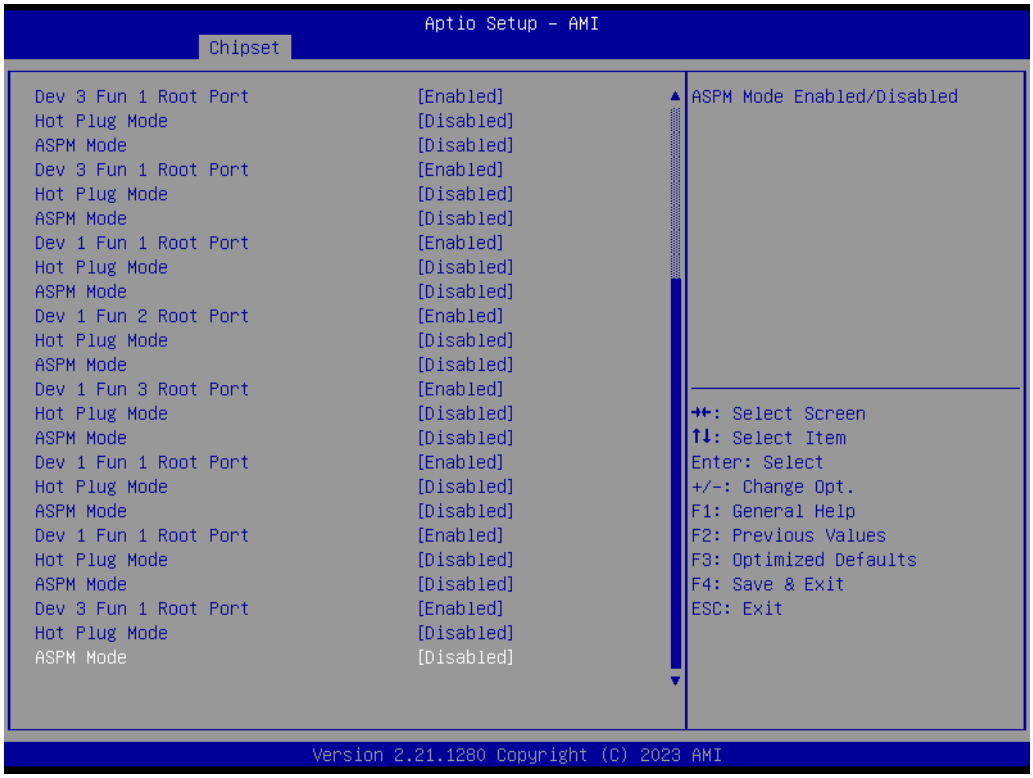


Figure 3.37 CRB Board

- **COM-HPC PCIE 0-15**
  Option Setting:
  X16, x8x8, x4x4x4x4
  SOM-DH7000:PCIEx16_1 slot.
- **COM-HPC PCIE 32-47**
  Option Setting:
  X16, x8x8, x4x4x4x4
  SOM-DH7000:PCIEx16_2 slot.
- **COM-HPC PCIE 16-31**
  Option Setting:
  X16, x8x8, x4x4x4x4
  SOM-DH7000:PCIEx16_3 slot.
- **COM-HPC PCIE 48-63**
  Option Setting:
  X16, x8x8, x4x4x4x4
  SOM-DH7000:PCIEx16_4 slot.
- **COM-HPC ETH 0-7**
  Option Setting:
  x8, x4x4
  SOM-DH7000:PCIEx8_1 slot.
- **Dev 3 Fun 1 Root Port**
  PCIe Lane: 0-15.
- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.
- **Dev 1 Fun 1 Root Port**
  PCIe Lane: 16-16.

- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.
- **Dev 3 Fun 1 Root Port**
  PCIe Lane: 55-48.
- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.
- **Dev 3 Fun 1 Root Port**
  PCIe Lane: 79-64.
- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.
- **Dev 1 Fun 1 Root Port**
  PCIe Lane: 32-35.
- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.
- **Dev 1 Fun 2 Root Port**
  PCIe Lane: 36-36.
- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.
- **Dev 1 Fun 3 Root Port**
  PCIe Lane: 37-37.
- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.
- **Dev 1 Fun 1 Root Port**
  PCIe Lane: 80-95.
- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.
- **Dev 1 Fun 1 Root Port**
  PCIe Lane: 100-100.
- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.
- **Dev 3 Fun 1 Root Port**
  PCIe Lane: 112-127.
- **Hot Plug Mode**
  Hot Plug Mode enable/disable.
- **ASPM Mode**
  ASPM Mode enable/disable.

3.2.3.3 AMD PBS

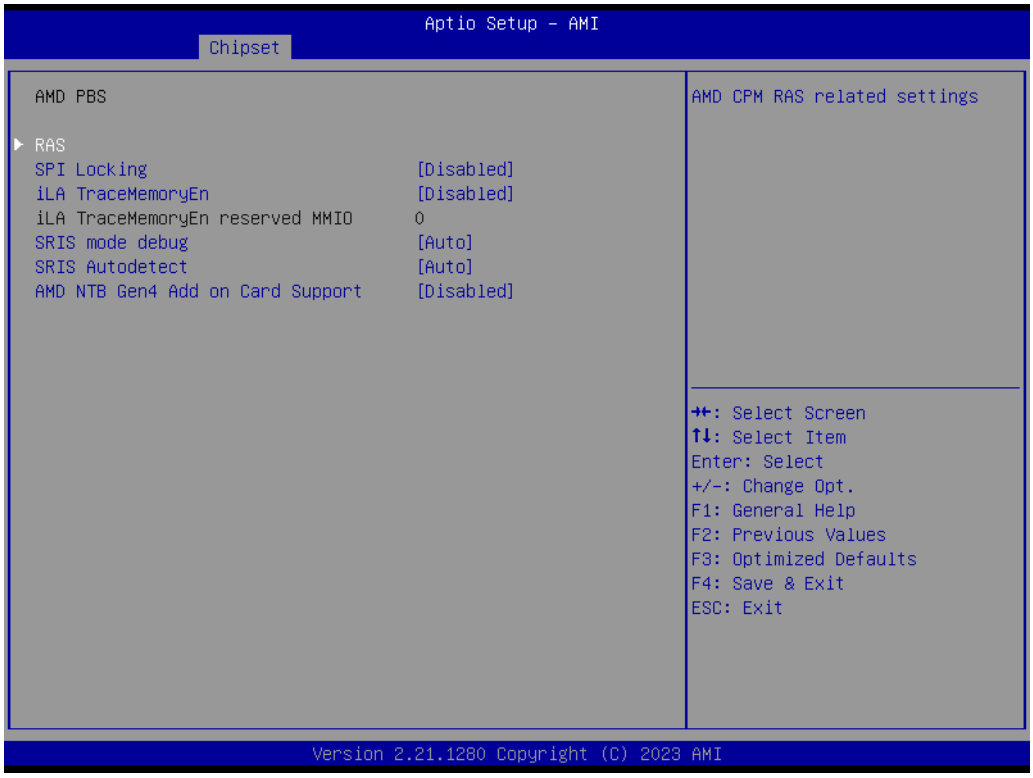


Figure 3.38 AMD PBS

- **RAS**
  AMD CPM RAS related settings.
- **SPI Locking**
  Enable/disable SPI Locking for protecting ROM part.
- **iLA TraceMemoryEn**
  Reserved 1M bytes MMIO space on 1M boundary when iLA TraceMemoryEn enabled.
- **SRIS mode debug**
  Control SRIS mode debug.
- **SRIS Autodetect**
  Control SRIS Autodetect.
- **AMD NTB Gen4 Add on Card Support**
  Enables support for AMD NTB Gen4 PCIe add-on card.

Figure 3.39 RAS

- **RAS Periodic SMI Control**
  Enable/disable Periodic SMI for polling [MCA Threshold] error.
- **SMI Threshold**
  The [SMI Threshold] limits the number of [MCA Threshold and Deferred Error SMI source] per a Unit time (Defined by [SMI Scale]). (Default: 5 dec interrupts)
- **SMI Scale**
  The [SMI Scale] defines the time scale. (Default: 1000 dec)
- **SMI Scale Unit**
  The [SMI Scale Unit] defines the unit of time scale. (Default: ms)
- **SMI Period**
  The [SMI Period] defines the polling interval (Default: 1000 dec, Maximum: 32767 dec, 0: Disable, Unit: ms)
- **GHES Notify Type**
  Notification type for deferred/corrected errors.
- **GHES UnCorr Notify Type**
  Notification type for uncorrected errors.
- **PCIe GHES Notify Type**
  Notification type for PCIe corrected errors.
- **PCIe UnCorr GHES Notify Type**
  Notification type for PCIe uncorrected errors.
- **PCIe Root Port Corr Err Mask Reg**
  Initialize the PCIe AER Corrected Error Mask register of the root port.
- **PCIe Root Port UnCorr Err Mask Reg**
  Initialize the PCIe AER Uncorrected Error Mask register of the root port.
- **Pcie Root Port UnCorr Error Sev Reg**
  Initialize the PCIe AER Uncorrected Error Severity registers of the root port.

- **PCIe Device Corr Err Mask Reg**
  Initialize the PCIe AER corrected error mask register of PCIe Device.
- **PCIe Device UnCorr Err Mask Reg**
  Initialize the PCIe AER uncorrected error mask register of PCIe Device.
- **Pcie Device UnCorr Error Sev Reg**
  Initialize the PCIe AER uncorrected error severity registers of PCIe Device.
- **CCIX GHES Deferred Err Notify Type**
  Notification type for CCIX deferred error.
- **CCIX GHES Corrected Err Notify Type**
  Notification type for CCIX corrected error.
- **DDR4 DRAM Hard Post Package Repair**
  This feature allows spare DRAM rows to replace malfunctioning rows via an in-field repair mechanism.
- **HEST DMC Structure Support**
  HEST DMC (deferred machine check) structure support.
- **RAS EINJ Mode**
  BIOS: Send APEI EINJ actions to PSP via CPM EINJ SMI callback; PSP; Send APEI EINJ actions to PSP via PSP Mailbox.

3.2.3.4 AMD CBS

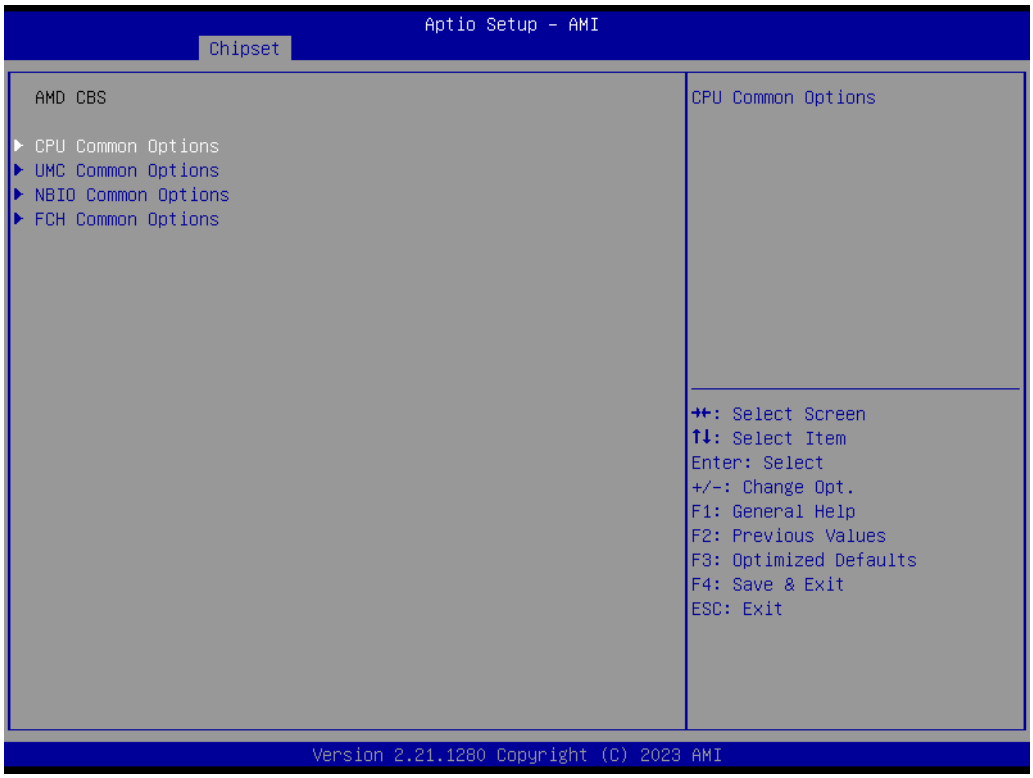


Figure 3.40 AMD CBS

- **CPU Common Options**
  CPU common options.
- **UMC Common Options**
  UMC common options.
- **NBIO Common Options**
  NBIO common options.
- **FCH Common Options**
  FCH common options.

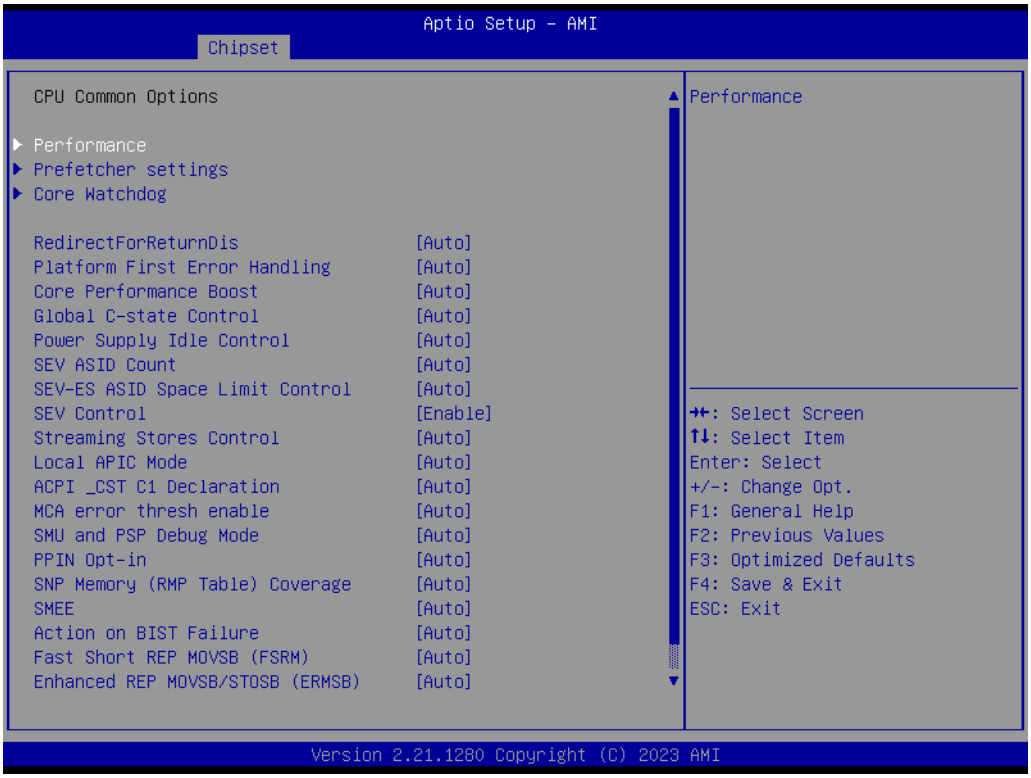


Figure 3.41 CPU Common Options

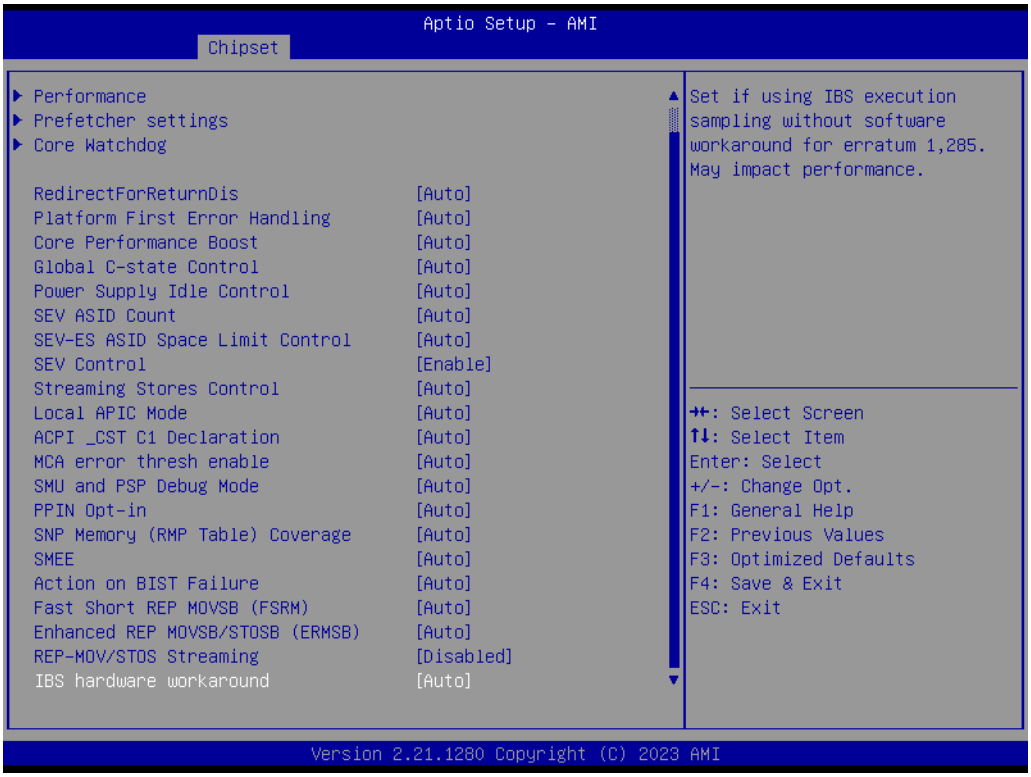


Figure 3.42 CPU Common Options

- **Performance**
  Performance.
- **Prefetcher settings**
  Prefetcher settings.

- **Core Watchdog**
  Core Watchdog.
- **RedirectForReturnDis**
  A workaround for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrctForReturns] to 1.
- **Platform First Error Handling**
  Enable/disable PFEH, cloak individual banks, and mask deferred error interrupts from each bank.
- **Core Performance Boost**
  Disable CPB.
- **Global C-state Control**
  Controls IO based C-state generation and DF C-states.
- **Power Supply Idle Control**
  Power Supply Idle Control.
- **SEV ASID Count**
  This field specifies the maximum valid ASID, which affects the maximum system physical address space. 16TB of physical address space is available for systems that support 253 ASIDs, while 8TB of physical address space is available for systems that support 509 ASIDs.
- **SEV-ES ASID Space Limit Control**
  Customize SEV-ES ASID space limit.
- **SEV Control**
  Can be used to disable SEV. To re-enable SEV, a Power Cycle is needed after selecting the 'Enable' option.
- **Streaming Stores Control**
  Enables or disables the streaming stores functionality.
- **Local APIC Mode**
  Select local APIC mode: Compatability, xAPIC or x2APIC.
- **ACPI_CST C1 Declaration**
  Determines whether or not to declare the C1 state to the OS.
- **MCA error thresh enable**
  Enable MCA error thresholding.
- **SMU and PSP Debug Mode**
  When this option is enabled, specific uncorrected errors detected by the PSP FW or SMU FW will hang and not reset the system.
- **PPIN Opt-in**
  Turn on PPIN feature.
- **SNP Memory (RMP Table) Coverage**
  Enabled = Entire system memory is covered.
- **SMEE**
  Control secure memory encryption enable.
- **Action on BIST Failure**
  Action to take when a CCD BIST failure is detected.
- **Fast Short REP MOVSB (FSRM)**
  Can be disabled for analysis purposes as long as the OS supports it.
- **Fast Short REP MOVSB (FSRM)**
  Can be disabled for analysis purposes as long as the OS supports it.
- **Enhanced REP MOVSB/STOSB (ERMSB)**
  Can be disabled for analysis purposes as long as the OS supports it.
- **REP-MOV/STOS Streaming**
  Allow REP-MOVS/STOS to use non-caching streaming stores for large sizes.

- **IBS hardware workaround**
  Set if using IBS execution sampling without software workaround for erratum 1,285. It may impact performance.

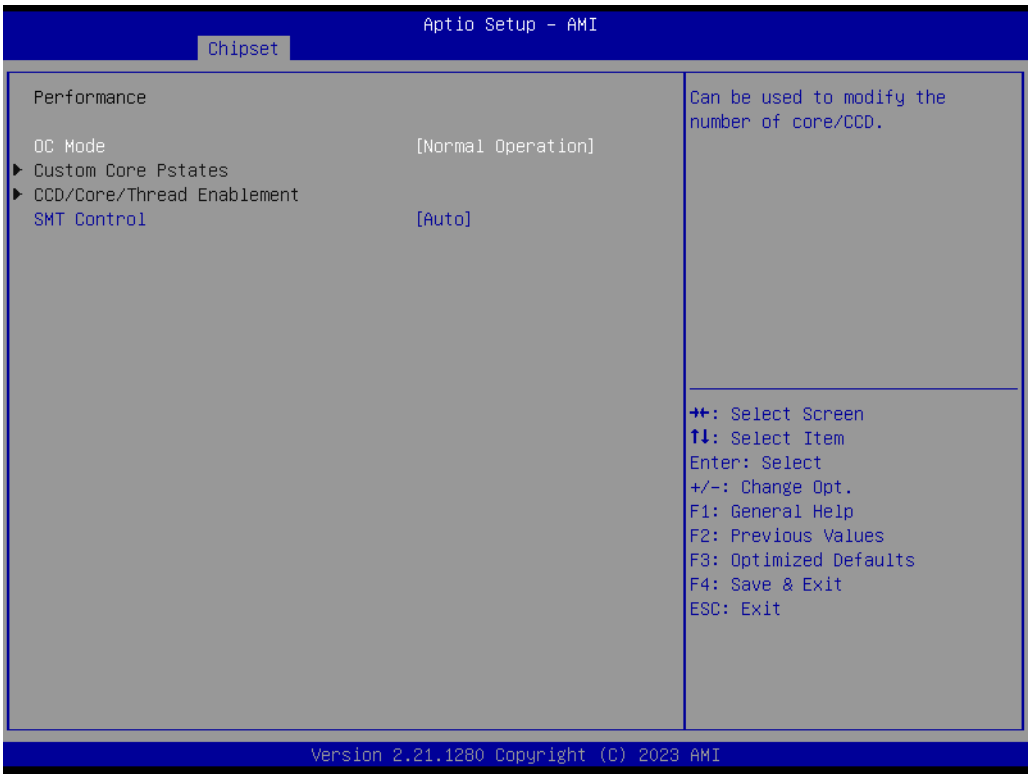


Figure 3.43 Performance

- **OC Mode**
  Can be used to modify the number of core/CCD.
- **SMT Control**
  Can be used to disable symmetric multi-threading. To re-enable SMT, a Power Cycle is needed after selecting the ‘Enable’ option. Select ‘Auto’ based on BIOS PCD (PcdAmdSmtMode) default setting. WARNING – S3 is Not Supported on systems where SMT is disabled.

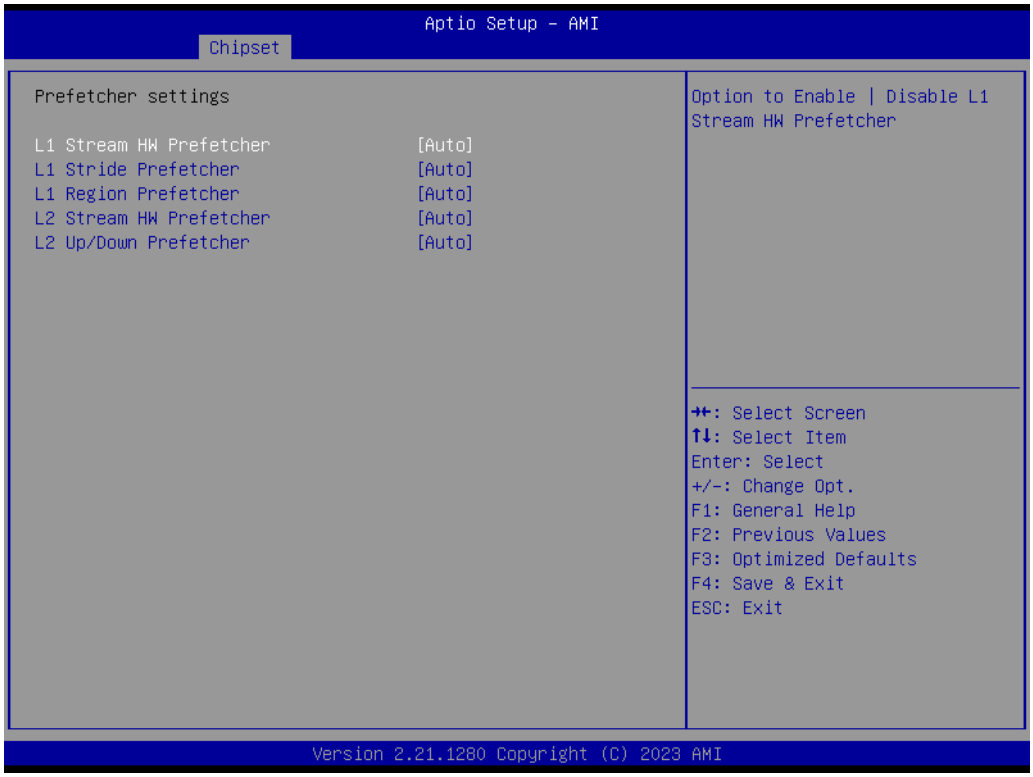


Figure 3.44 Prefetcher settings

- **L1 Stream HW Prefetcher**
  Options to Enable | Disable L1 Stream HW Prefetcher.
- **L1 Stride Prefetcher**
  Uses memory access history of individual instructions to fetch additional lines when each access is a constant distance from the previous.
- **L1 Region Prefetcher**
  Uses memory access history to fetch additional lines when the data access for a given instruction tends to be followed by other data accesses.
- **L2 Stream HW Prefetcher**
  Option to Enable | Disable L2 Stream HW Prefetcher.
- **L2 Up/Down Prefetcher**
  Uses memory access history to determine whether to fetch the next or previous line for all memory accesses.

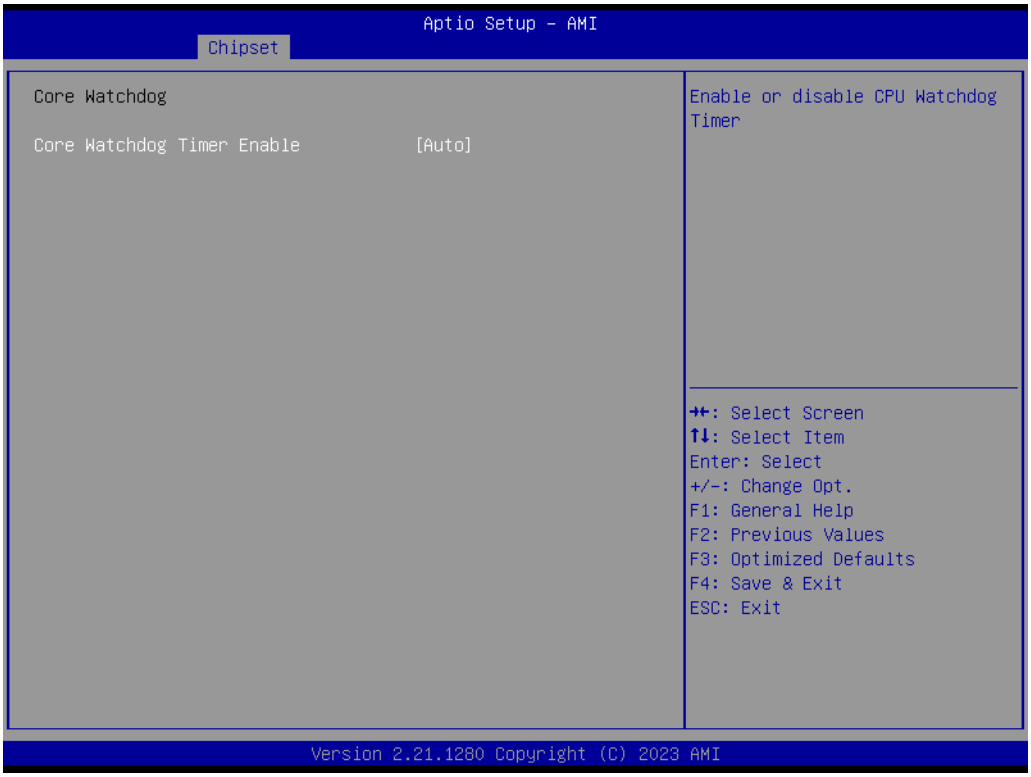


Figure 3.45 Core Watchdog

Figure 3.46 UMC Common Options

- **DDR4 Common Options**
  DDR4 Common Options.
- **DRAM Memory Mapping**
  DRAM Memory Mapping.

- **NVDIMM**
  NVDIMM.
- **Memory MBIST**
  Memory MBIST.

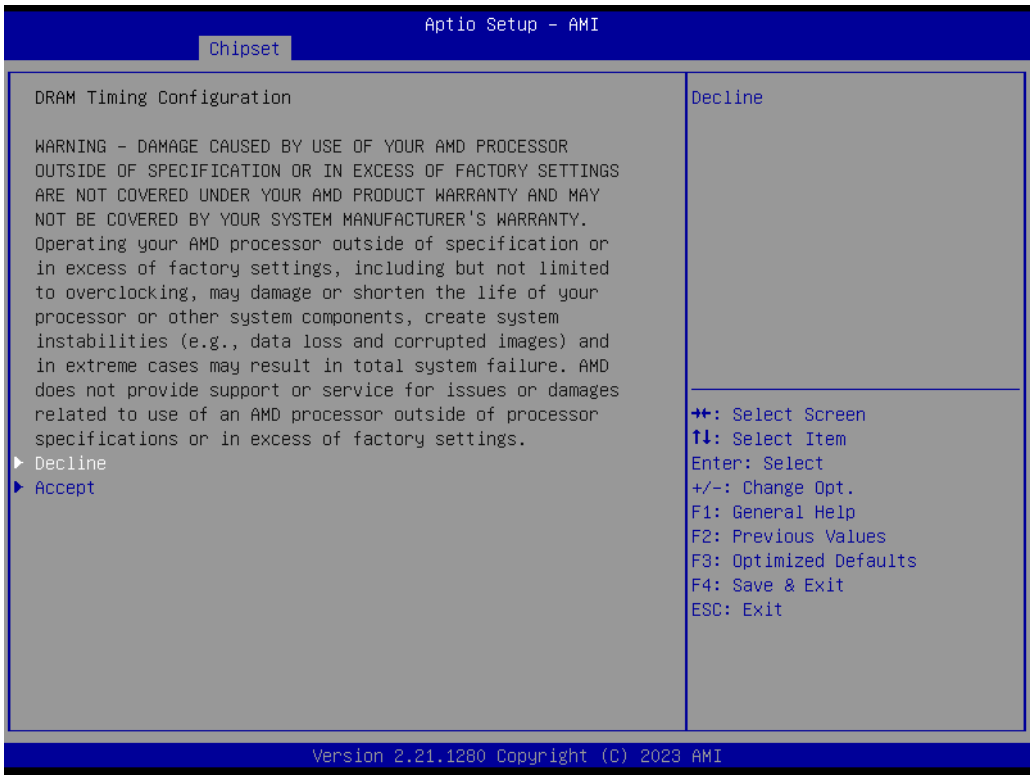


Figure 3.47 DRAM Timing Configuration

- **Decline**
  Decline.
- **Accept**
  Accept.

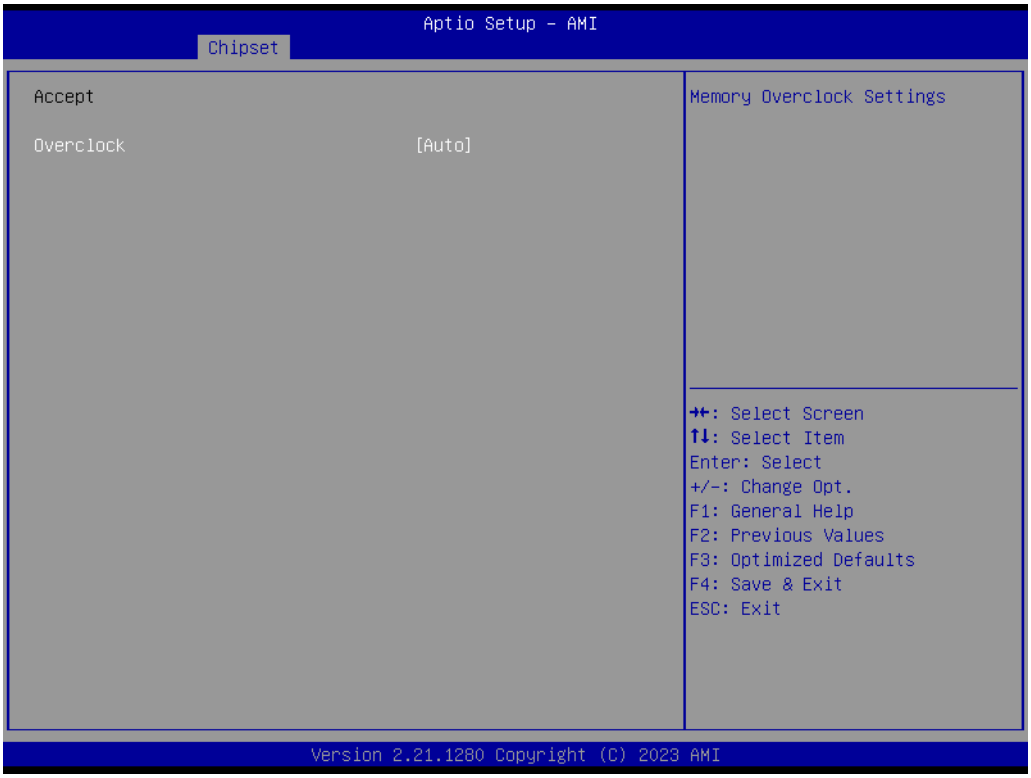


Figure 3.48 Accept

- **Overclock**
  Memory Overclock Settings.

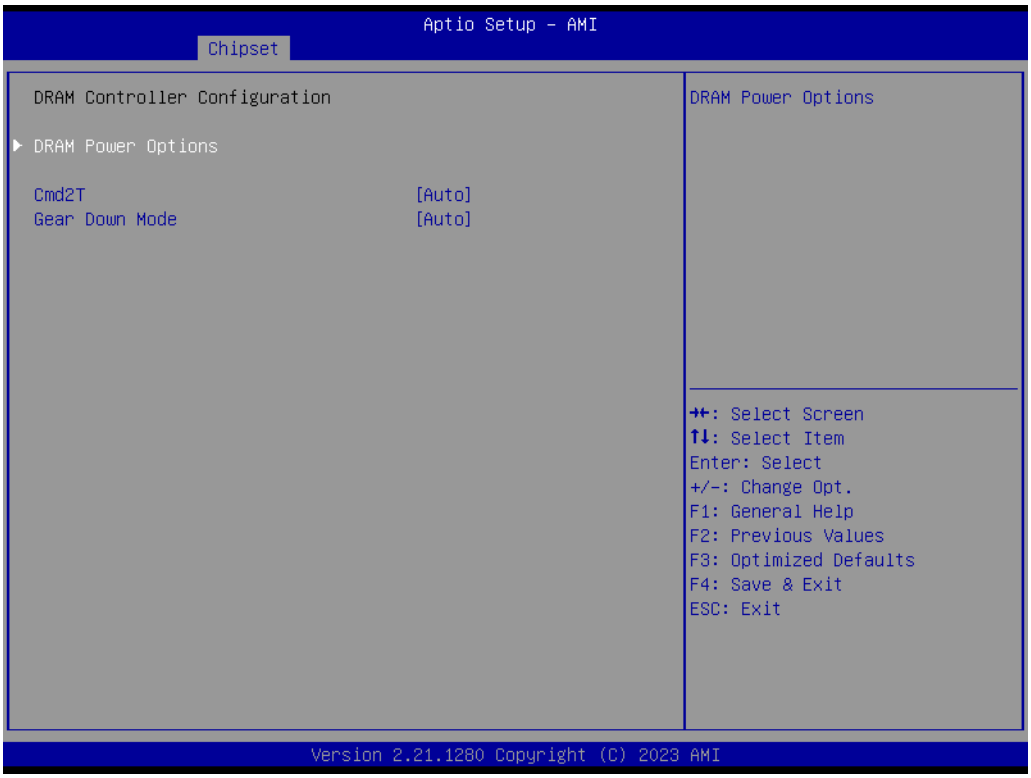


Figure 3.49 DRAM Controller Configuration

- **DRAM Power Options**
  DRAM Power Options.
- **Cmd2T**
  Select between 1T and 2T mode on ADDR/CMD.
- **Gear Down Mode**
  Enable or disable Gear Down Mode.

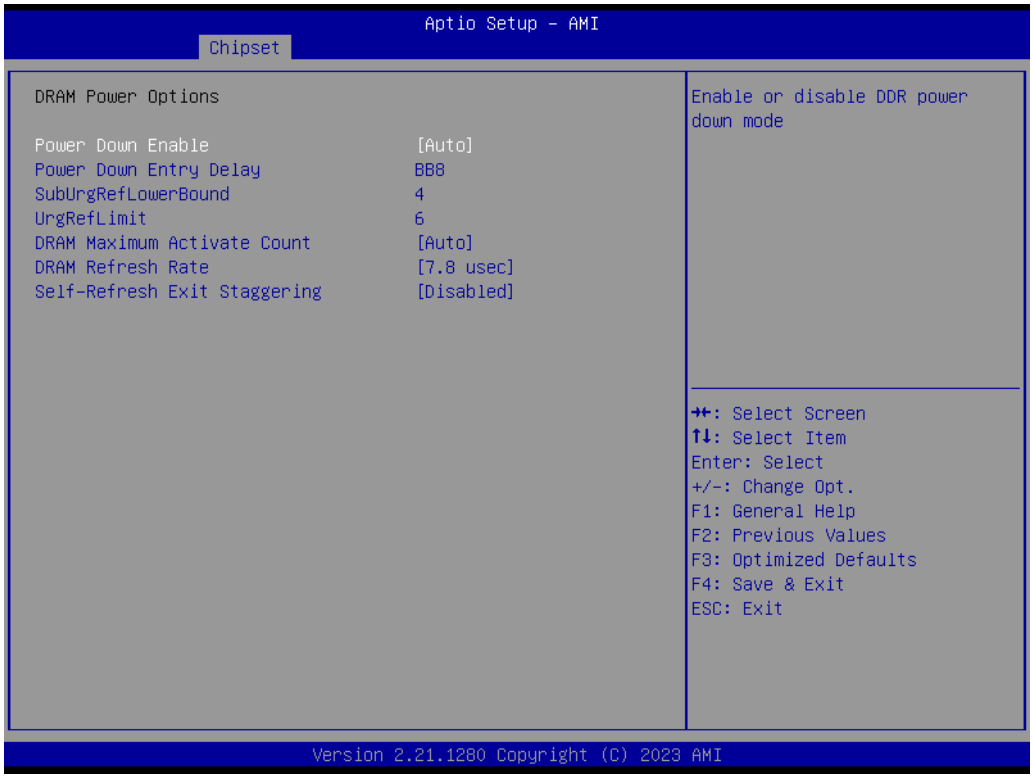


Figure 3.50 DRAM Power Options

- **Power Down Enable**
  Enable or disable DDR power down mode.
- **Power Down Entry Delay**
  Specify value at UMC: : CH : : DramTiming17 [19:8].
  PwrDownDly.
- **SubUrgRefLowerBound.**
  Specifies the stored refresh limit to required enter sub-urgent refresh mode
  Constraint: SubUrgRefLowerBound <= UrgRefLimit.
  Valid value: 6 ~ 1
- **UrgRefLimit**
  Specifies the stored refresh limit to required enter urgent refresh mode
  Constraint: SubUrgRefLowerBound <= UrgRefLimit.
  Valid value: 6 ~ 1
- **DRAM Maximum Activate Count**
  Override DIMM SPD Byte 7 [3:0] Maximum Activate Count (MAC) Auto: based on SPD setting.
- **DRAM Refresh Rate**
  DRAM Refresh Rate.
- **Self-Refresh Exit Staggering**
  Tcksrx += (Trfc/n * (UMC_Number % 4)), here n = 3 or 4
  Disabled: does not apply the extra addition.

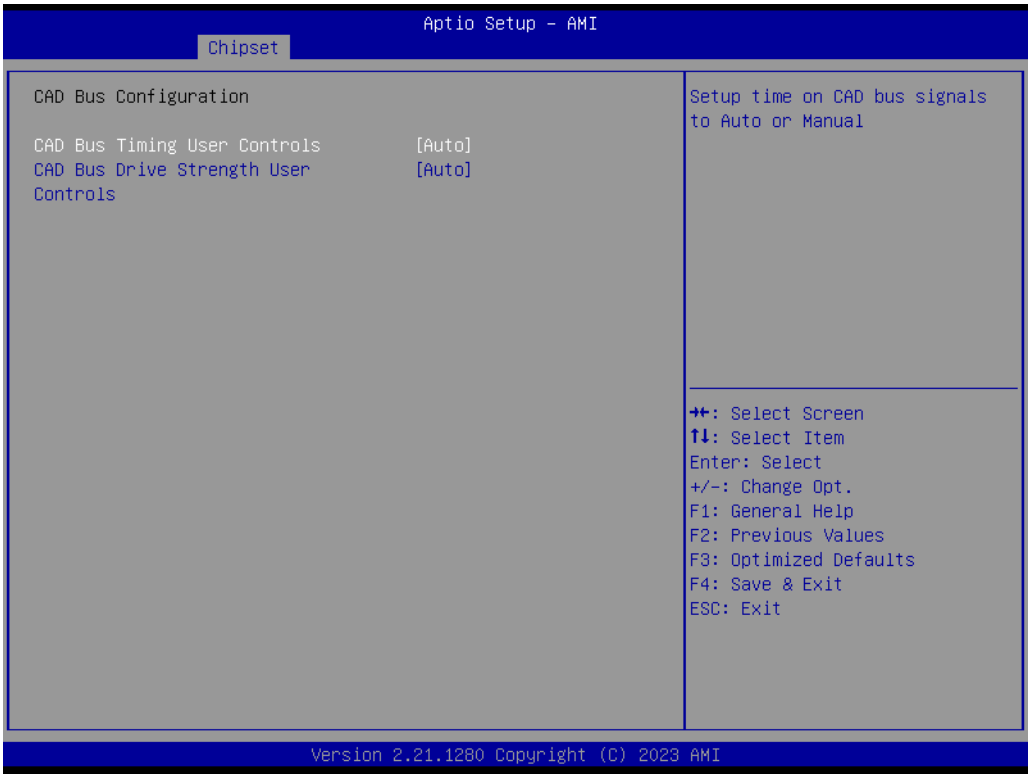


Figure 3.51 CAD Bus Configuration

- **CAD Bus Timing User Controls**
  Setup time on CAD bus signals to Auto or Manual.
- **CAD Bus Drive Strength User Controls**
  Drive Strength on CAD bus signals to Auto or Manual.

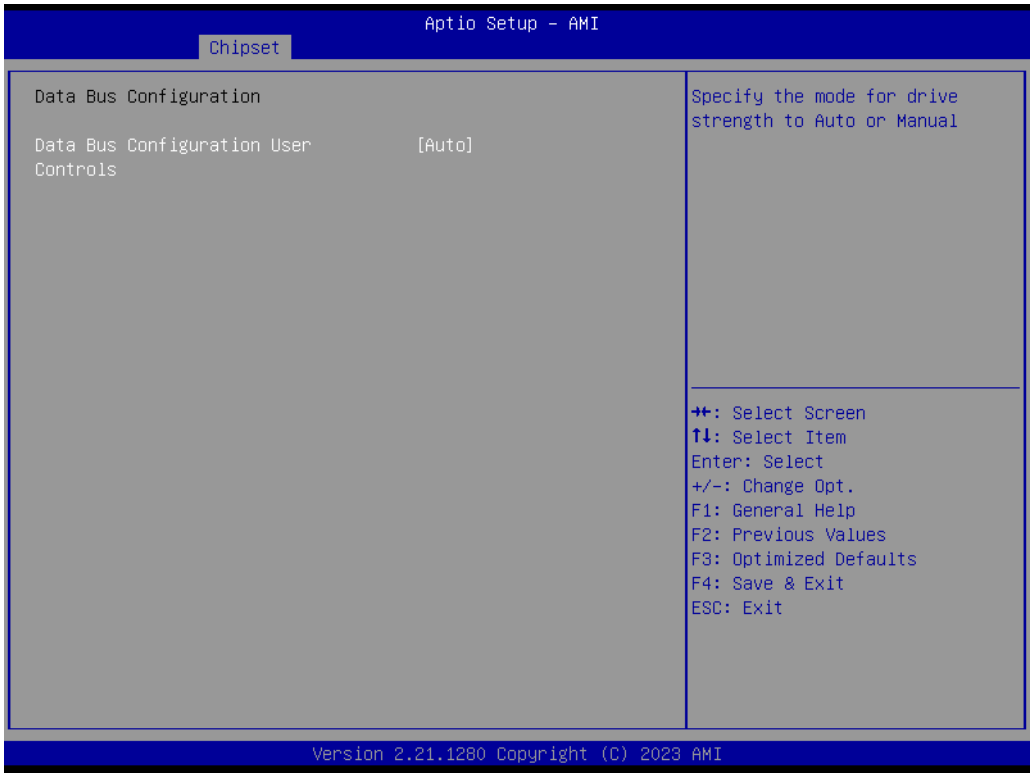


Figure 3.52 Data Bus Configuration

- **Data Bus Configuration User Controls**
  Specify the mode for drive strength to Auto or Manual.

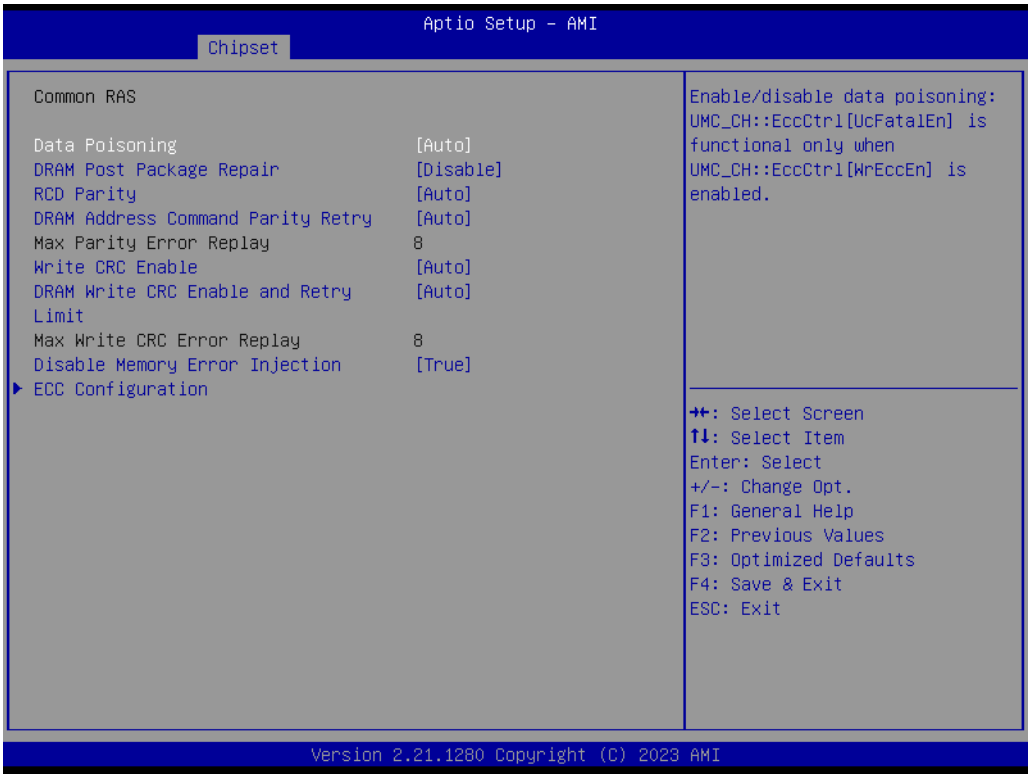


Figure 3.53 Common RAS

- **Data Poisoning**
  Enable/disable data poisoning: UMC_CH::EccCtrl[UcFatalEn] is functional only when UMC_CH::EccCtrl[WrEccEn] is enabled.
- **DRAM Post Package Repair**
  Enable or disable DRAM Post Package Repair.
- **RCD Parity**
  Enable or disable RCD parity.
- **DRAM Address Command Parity Retry**
  UMC_CH::RecCtrl[RecEn][0] and UMC_CH::RecCtrl[MaxParRply].
- **Write CRC Enable**
  Enable write CRC generation. UMC::CH::BeqCtrl1[WrCrcEn].
- **DRAM Write CRC Enable and Retry Limit**
  UMC_CH::RecCtrl[RecEn][1] and UMC_CH::RecCtrl[MaxCrcRply]
- **Disable Memory Error Injection**
  True: UMC::CH::MiscCfg[DisErrInj]=1
- **ECC Configuration**
  ECC Configuration.

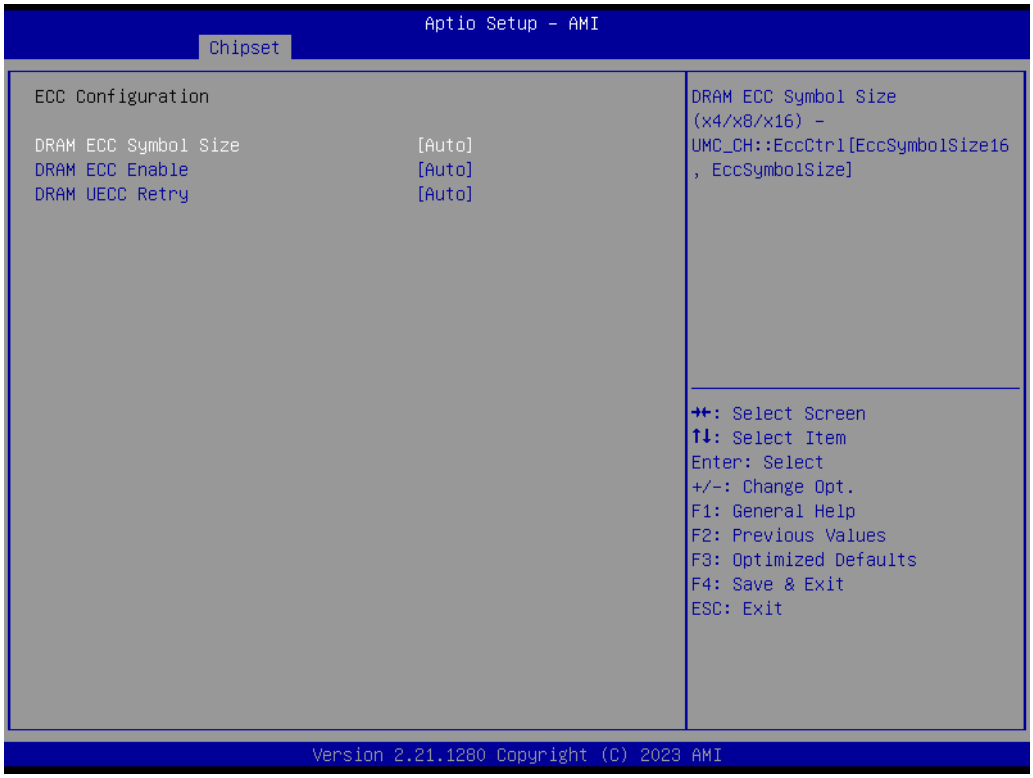


Figure 3.54 ECC Configuration

- **DRAM ECC Symbol Size**
  DRAM ECC Symbol Size (x4/x8/x16) - UMC_CH::EccCtrl[EccSymbolSize16, EccSymbolSize].
- **DRAM ECC Enable**
  Use this option to enable/disable DRAM ECC. Auto will set ECC to enable.
- **DRAM UECC Retry**
  Use this option to enable/disable DRAM UECC Retry.

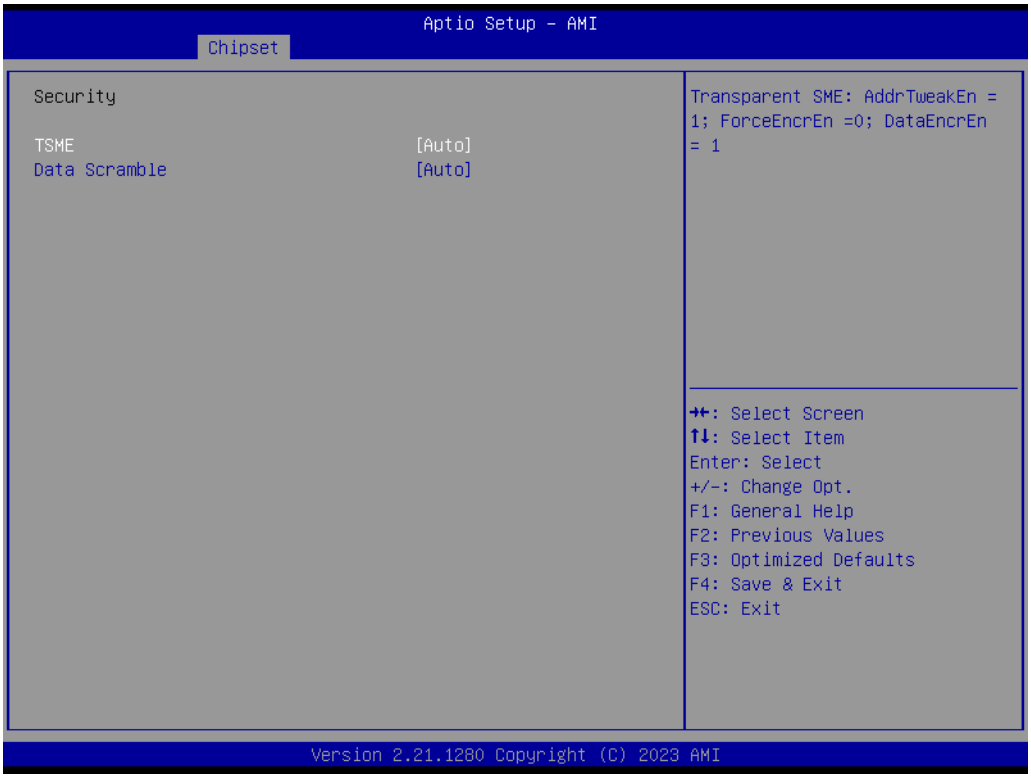


Figure 3.55 Security

- **TSME**
  Transparent SME: AddrTweakEn = 1; ForceEncrEn =0; DataEncrEn = 1.
- **Data Scramble**
  Data scrambling: DataScrambleEn.

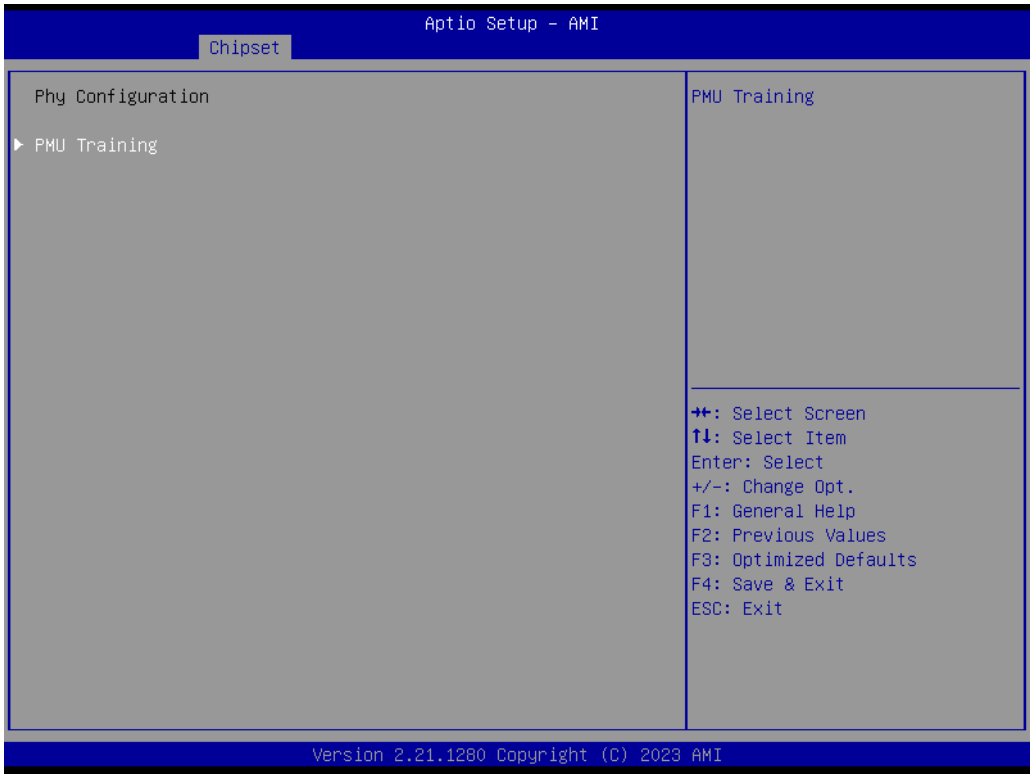


Figure 3.56 Phy Configuration

- **PMU Training**
  PMU Training.

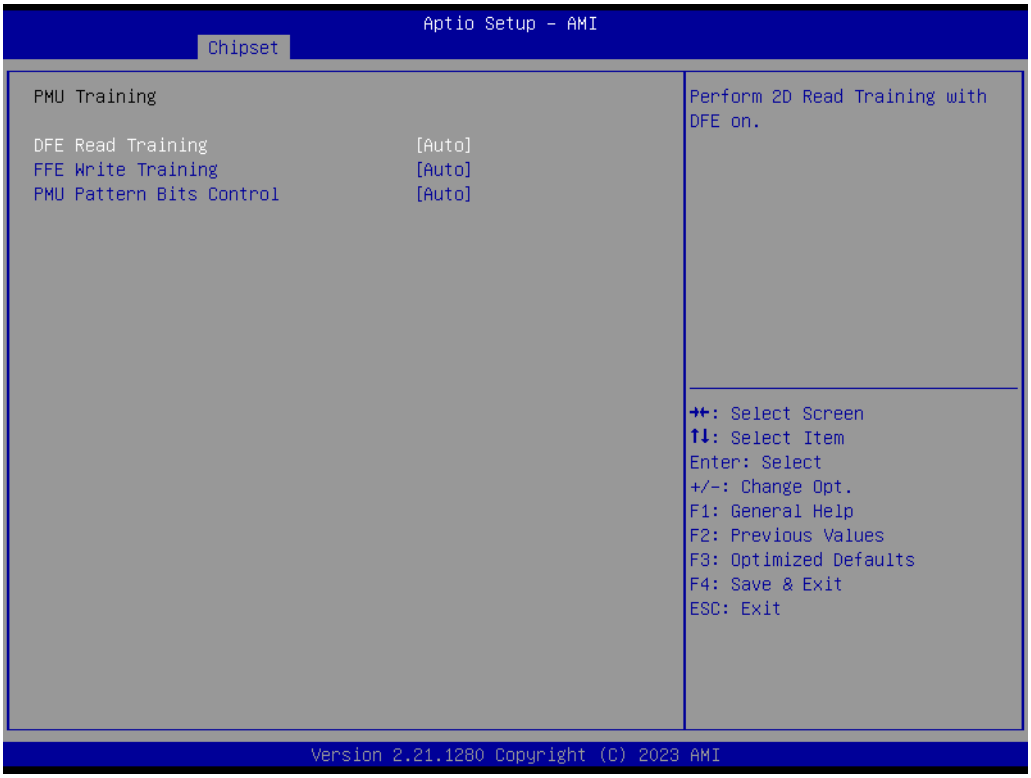


Figure 3.57 PMU Training

- **DFE Read Training**
  Perform 2D Read Training with DFE on.
- **FFE Write Training**
  Perform 2D Write Training with FFE on.
- **PMU Pattern Bits Control**
  Customize PMU pattern bits.

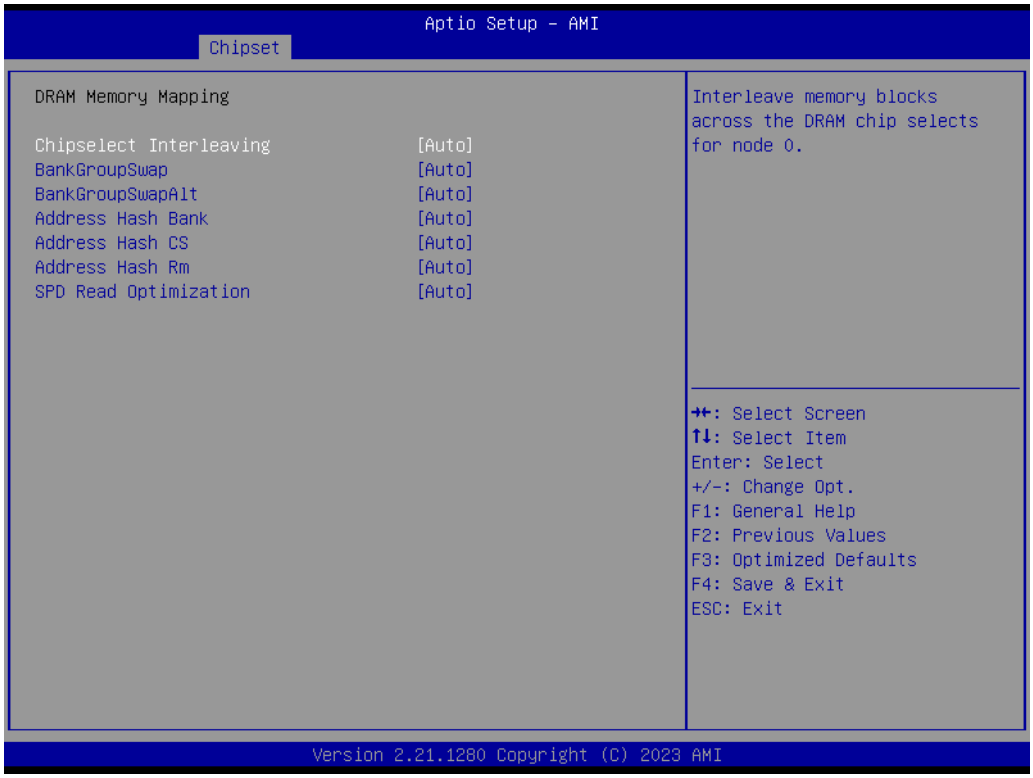


Figure 3.58 DRAM Memory Mapping

- **Chipselect Interleaving**
  Interleave memory blocks across the DRAM chip selects for node 0.
- **BankGroupSwap**
  BankGroupSwapAlt default = Enabled in BIOS, which has priority than Bank-GroupSwap. BIOS equation: If BankGroupSwapAlt == Enabled Then Bank-GroupSwap = Disabled Endif Please set BankGroupSwapAlt to Disabled while set BankGroupSwap to Enabled.
- **BankGroupSwapAlt**
  BankGroupSwapAlt default = Enabled in BIOS, which has priority than Bank-GroupSwap. BIOS equation: If BankGroupSwapAlt == Enabled Then Bank-GroupSwap = Disabled Endif Please set BankGroupSwapAlt to Disabled while set BankGroupSwap to Enabled.
- **Address Hash Bank**
  Enable or disable bank address hashing.
- **Address Hash CS**
  Enable or disable CS address hashing.
- **Address Hash Rm**
  Enable or disable RM address hashing.
- **SPD Read Optimization**
  Enable or disable SPD Read Optimization, enabled - SPD reads are skipped for reserved fields and most of upper 256 Bytes, disabled - read all 512 SPD Bytes.

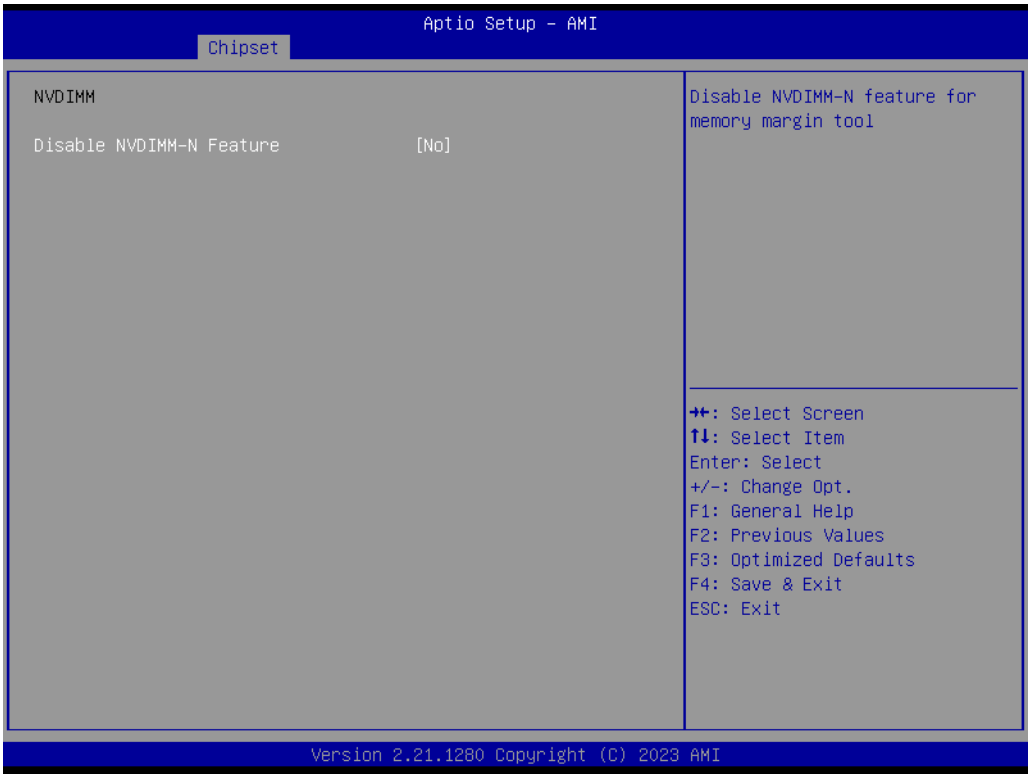


Figure 3.59 NVDIMM

- **Disable NVDIMM-N Feature**
  Disable NVDIMM-N feature for memory margin tool.

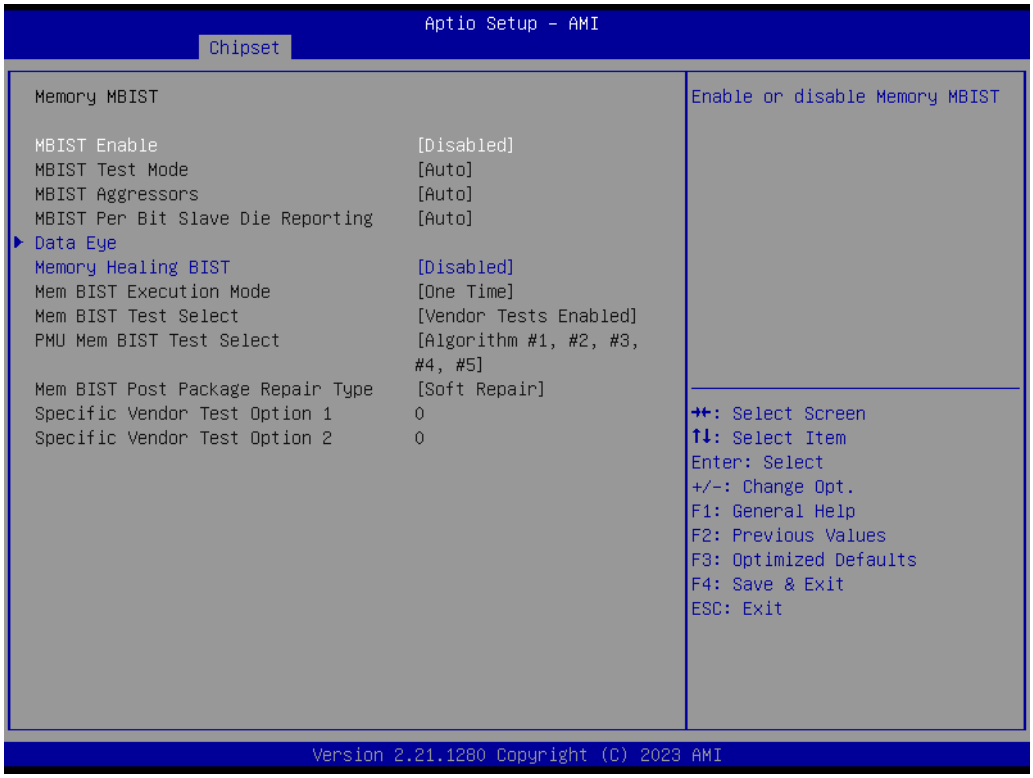


Figure 3.60 Memory MBIST

- **MBIST Enable**
  Enable or disable memory MBIST.
- **Data Eye**
  Data Eye.
- **Memory Healing BIST**
  Enabling a full memory test will extend the startup time.
  - The BIOS Memory Built-In Self-Test (Mem BIST) assesses the entire memory after initialization. If any memory components are found to be defective, they will be repaired through either a soft or hard Post-Production Repair (PPR) process, depending on the system's configuration. This test will take approximately 3 minutes for every 16GB of installed memory.
  - In cases where Self-Healing Built-In Self-Test (BIST) is supported by the device and the DIMM, it will execute JEDEC DRAM self-healing procedures for any detected issues with the DRAM. If necessary, a hard repair will be performed on any failing memory. This test will take about 10 seconds for each memory rank per channel.

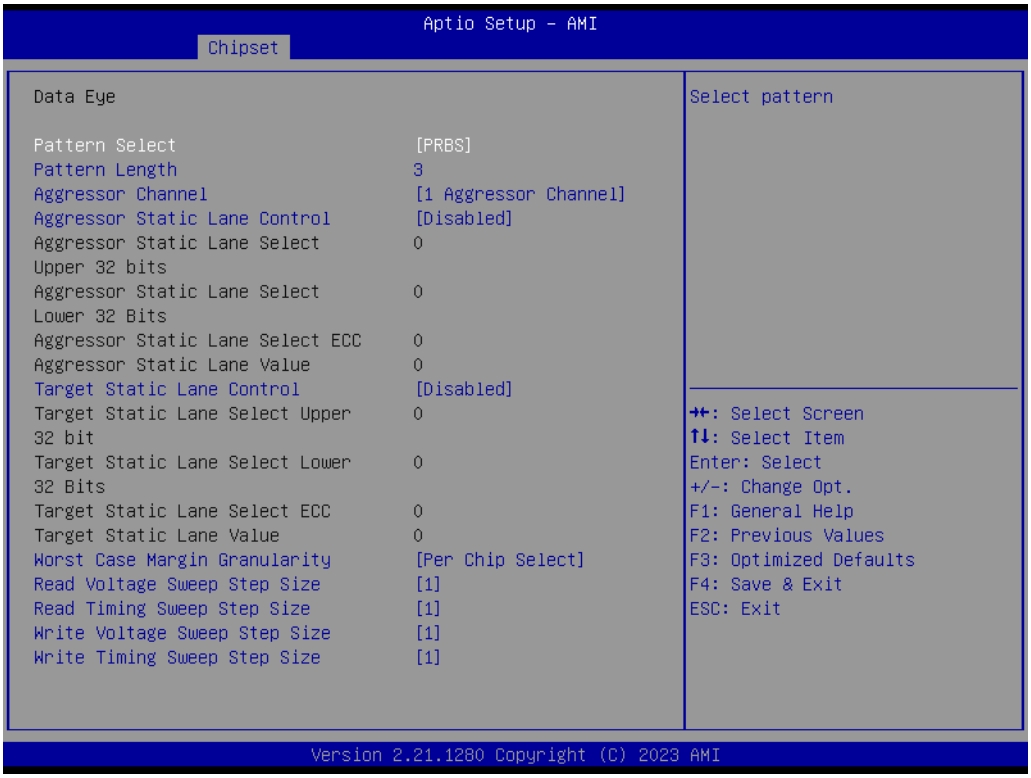


Figure 3.61 Data Eye

- **Pattern Select**
  Pattern Select.
- **Pattern Length**
  This token helps to determine the pattern length. The possible options are N=3...12.
- **Aggressor Channel**
  This helps read the aggressors channels. If it is enabled, you can read from one or more than one aggressor channel. The default is set to disabled.
- **Aggressor Static Lane Control**
  This option, if enabled, will control the Aggressor Static Lane Controls.
- **Target Static Lane Control**
  Enable or disable target static lane.
- **Worst Case Margin Granularity**
  Select per Chip or per Nibble.
- **Read Voltage Sweep Step Size**
  This option determines the step size for Read Data Eye voltage sweep. Supported options are 1,2 and 4.
- **Read Timing Sweep Step Size**
  This options supports step size for Read Data Eye. Supported options are 1, 2 and 4.
- **Write Voltage Sweep Step Size**
  This option determines the step size for write Data Eye voltage sweep. Supported options are 1,2 and 4.
- **Write Timing Sweep Step Size**
  This options supports step size for write Data Eye. Supported options are 1, 2 and 4.

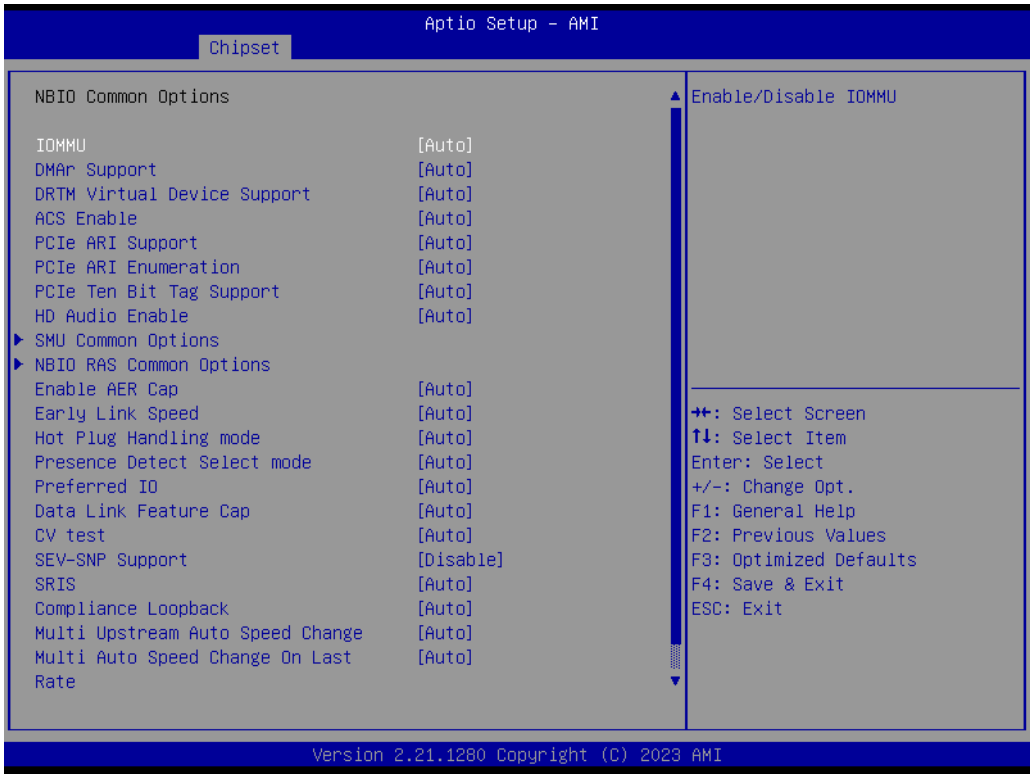


Figure 3.62 NBIO Common Options

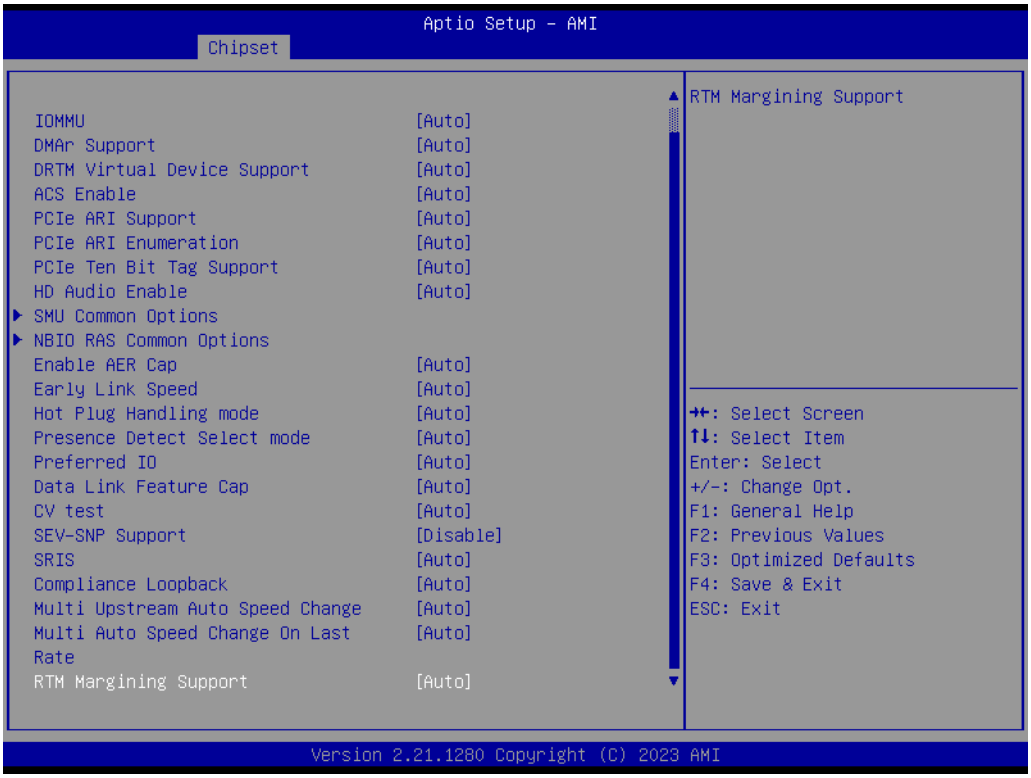


Figure 3.63 NBIO Common Options

- **IOMMU**
  Enable/disable IOMMU.
- **DMAr Support**
  Enable DMAr system protection during POST.
- **DRTM Virtual Device Support**
  Enable DRTM ACPI virtual device.
- **ACS Enable**
  AER must be enabled for ACS enable to work.
- **PCIe ARI Support**
  Enables Alternative Routing-ID Interpretation.
- **PCIe ARI Enumeration**
  Activates ARI Forwarding for each downstream port.
- **PCIe Ten Bit Tag Support**
  Enables PCIe ten bit tags for supported devices. Auto = Enabled.
- **HD Audio Enable**
  Controls HD audio enable or disable.
- **SMU Common Options**
  SMU common options.
- **NBIO RAS Common Options**
  NBIO RAS common options.
- **Enable AER Cap**
  Enables advanced error reporting capability.
- **Early Link Speed**
  Early link speed.
- **Hot Plug Handling mode**
  Controls the hot plug handling mode.

- **Control the Hot Plug Handling mode**
  Controls the presence detect select mode.
- **Preferred IO**
  Preferred IO Select Type Auto: Default.
- **Data Link Feature Cap**
  Data link feature capability.
- **CV test**
  Set this to enabled to support running PCIECV tool. Auto - preserve h/w defaults.
- **SEV-SNP Support**
  Enable or Disable SEV-SNP support.
- **SRIS**
  SRIS.
- **Compliance Loopback**
  Compliance Loopback Test.
- **Multi Upstream Auto Speed Change**
  Defines the setting of this feature for all PCIe devices. 'Auto' uses the DXIO default setting of 0 for Gen1 and 1 for Gen2/3.
- **Multi Auto Speed Change On Last Rate**
  Determines how PCIe link training speed should behave with respect to the last advertised speed for all ports. Disabled=Use highest data rate ever advertised. Enabled=Use last data rate advertised.
- **RTM Margining Support**
  RTM margining support.

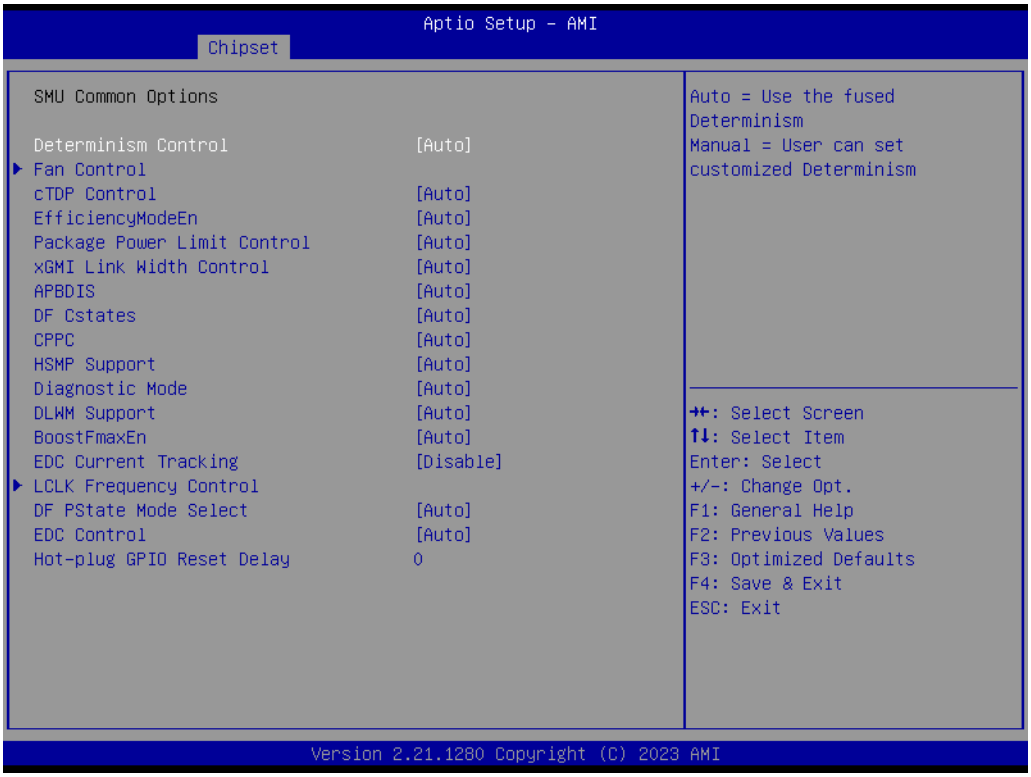


Figure 3.64 SMU Common Options

- **Determinism Control**
  Auto = Uses the fused Determinism
  Manual = Users can set customized Determinism.
- **Fan Control**
  Fan control.
- **cTDP Control**
  Auto = Use the fused TDP
  Manual = Users can set customized TDP
  TDP is used to define the RC thermal model only
- **EfficiencyModeEn**
  0 = use performance optimized CCLK DPM settings
  1 = use power efficiency optimized CCLK DPM settings.
- **Package Power Limit Control**
  Auto = Use the fused PPT
  Manual = User can set customized PPT
  PPT will be used as the ASIC power limit
- **xGMI Link Width Control**
  Auto = Use default xGMI link width controller settings
  Manual = User can set custom xGMI link width controller settings.
- **APBDIS**
  0 = not APBDIS (mission mode)
  1 = APBDIS
- **DF Cstates**
  Enable = Enables DF C-states
  Disable = Disables DF C-states
- **CPPC**
  FEATURE_CPPC_MASK

- **HSMP Support**
  Enable or disable HSMP support.
- **Diagnostic Mode**
  Enable or disable Diag mode.
- **DLWM Support**
  Enable or disable DLWM support.
- **BoostFmaxEn**
  Auto = Use the default Fmax
  Manual = User can set the boost Fmax
  (043B) BoostFmax.
- **EDC Current Tracking**
  The generation a correctable MCE when the telemetry current value is over the set threshold defined by EDC Current Tracking threshold.
- **LCLK Frequency Control**
  LCLK Frequency Control.
- **DF PState Mode Select**
  Selects the DF PState Mode.
  - Normal
  - Limit Highest (FCLK is limited to DF Pstate FCLK Limit, only the highest DF Pstate is used)
  - Limit All (FCLK is limited to DF Pstate FCLK limit, all DF Pstates are used).
- **EDC Control**
  Auto = Use the fused VDDCR_CPU EDC limit
  Manual = User can set customized VDDCR_CPU EDC limit.
- **Hot-plug GPIO Reset Delay**
  GPIO reset delay in milliseconds.

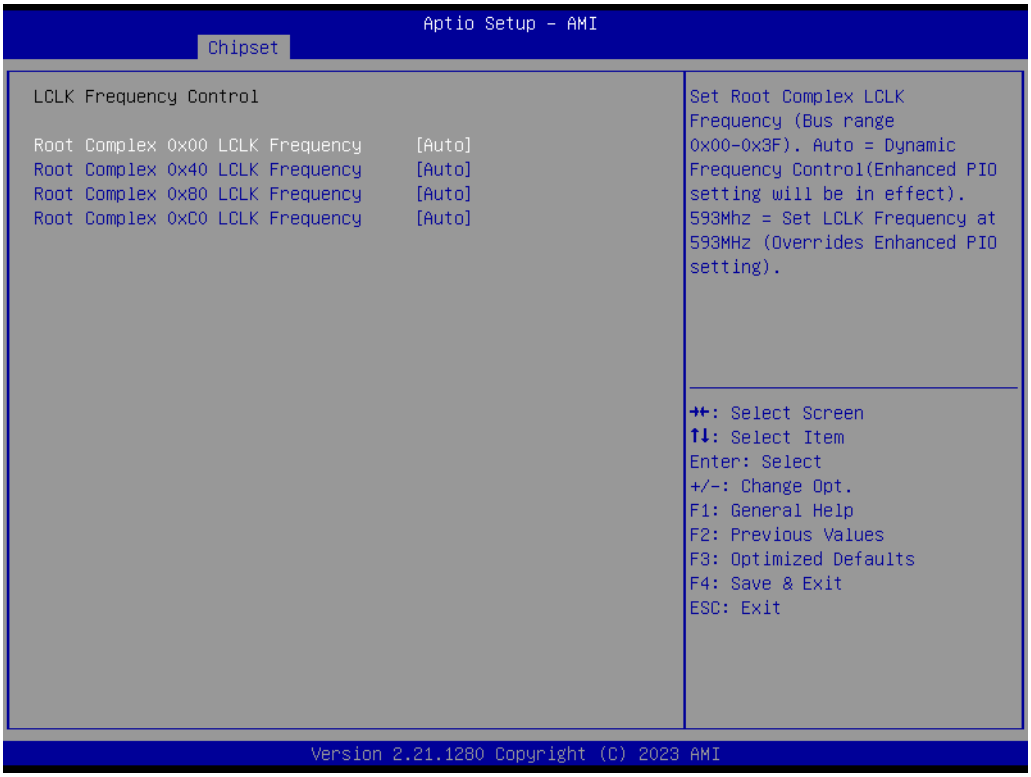


Figure 3.65 LCLK Frequency Control

- **Root Complex 0x00 LCLK Frequency**
  Set Root Complex LCLK Frequency (Bus range 0x00-0x1F). Auto = Dynamic Frequency Control (Enhanced PIO setting will be in effect). 593Mhz = Set LCLK Frequency at 593MHz (Overrides Enhanced PIO setting).
- **Root Complex 0x40 LCLK Frequency**
  Set Root Complex LCLK Frequency (Bus range 0x40-0x5F). Auto = Dynamic Frequency Control (Enhanced PIO setting will be in effect). 593Mhz = Set LCLK Frequency at 593MHz (Overrides Enhanced PIO setting).
- **Root Complex 0x80 LCLK Frequency**
  Set Root Complex LCLK Frequency (Bus range 0x80-0x9F). Auto = Dynamic Frequency Control (Enhanced PIO setting will be in effect). 593Mhz = Set LCLK Frequency at 593MHz (Overrides Enhanced PIO setting).
- **Root Complex 0xC0 LCLK Frequency**
  Set Root Complex LCLK Frequency (Bus range 0xC0-0xDF). Auto = Dynamic Frequency Control (Enhanced PIO setting will be in effect). 593Mhz = Set LCLK Frequency at 593MHz (Overrides Enhanced PIO setting).

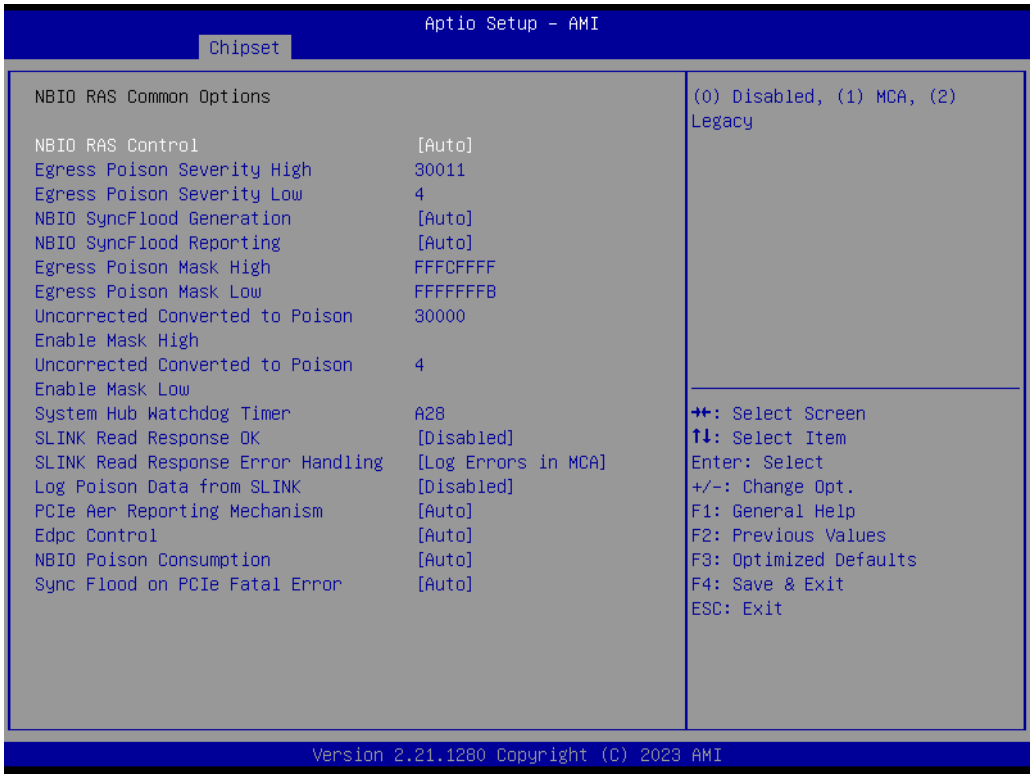


Figure 3.66 NBIO RAS Common Options

- **NBIO RAS Control**
  (0) Disabled, (1) MCA, (2) Legacy.
- **Egress Poison Severity High**
  Each bit set to 1 enables HIGH severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.
- **Egress Poison Severity Low**
  Each bit set to 1 enables HIGH severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.
- **NBIO SyncFlood Generation**
  This value may be used to mask SyncFlood caused by NBIO RAS options. When set to TRUE SyncFlood from NBIO is masked. When set to FALSE, NBIO is capable of generating SyncFlood.
- **NBIO SyncFlood Reporting**
  This value may be used to enable SyncFlood reporting to APML. When set to TRUE SyncFlood will be reported to APML. When set to FALSE, that reporting will be disabled.
- **Egress Poison Mask High**
  These set the enable mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.
- **Egress Poison Mask Low**
  These set the enable mask for masking of errors logged in EGRESS_POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.
- **Uncorrected Converted to Poison Enable Mask High**
  These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP.

errors on arrays associated with that egress port. For each bit set to 0, errors are masked.

- **Uncorrected Converted to Poison Enable Mask Low**
  These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP errors on arrays associated with that egress port. For each bit set to 0, errors are masked.
- **System Hub Watchdog Timer**
  This value specifies the timer interval of the SYSHUB Watchdog timer in milli-seconds.
- **SLINK Read Response OK**
  This value specifies whether SLINK read response errors are converted to an Okay response. When this value is set to TRUE, read response errors are converted to Okay responses with data of all FFs. When set to FALSE, read response errors are not converted.
- **SLINK Read Response Error Handling**
  This value specifies whether SLINK write response errors are converted to an Okay response. When this value is set to 0, write response errors will be logged in the MCA. When set to 1, write response errors will trigger an MCOMMIT error. When this value is set to 2, write response errors are converted to Okay responses.
- **Log Poison Data from SLINK**
  This value specifies whether poison data propagated from SLINK will generate a deferred error. When set to TRUE, deferred errors are enabled. When set to FALSE, errors are not generated.
- **PCIe Aer Reporting Mechanism**
  This value selects the method of reporting AER errors from PCI Express. ..A value of 1 allows OS First handling of the errors through generation of a system control interrupt (SCI). A value of 2 provides for Firmware First handling of errors through generation of a system management interrupt (SMI).
- **Edpc Control**
  (0) Disabled; (1) Enabled; (3) Auto.
- **NBIO Poison Consumption**
  NBIO Poison Consumption.
- **Sync Flood on PCIe Fatal Error**
  When 'Sync Flood on PCIe Fatal Error' is True, PcdAmdPcieSyncFloodOnFatal should be set to True.
  When 'Sync Flood on PCIe Fatal Error' is False, PcdAmdPcieSyncFloodOnFatal should be set to False.
  When 'Sync Flood on PCIe Fatal Error' is Auto, PcdAmdPcieSyncFloodOnFatal should retain its AGESA default.

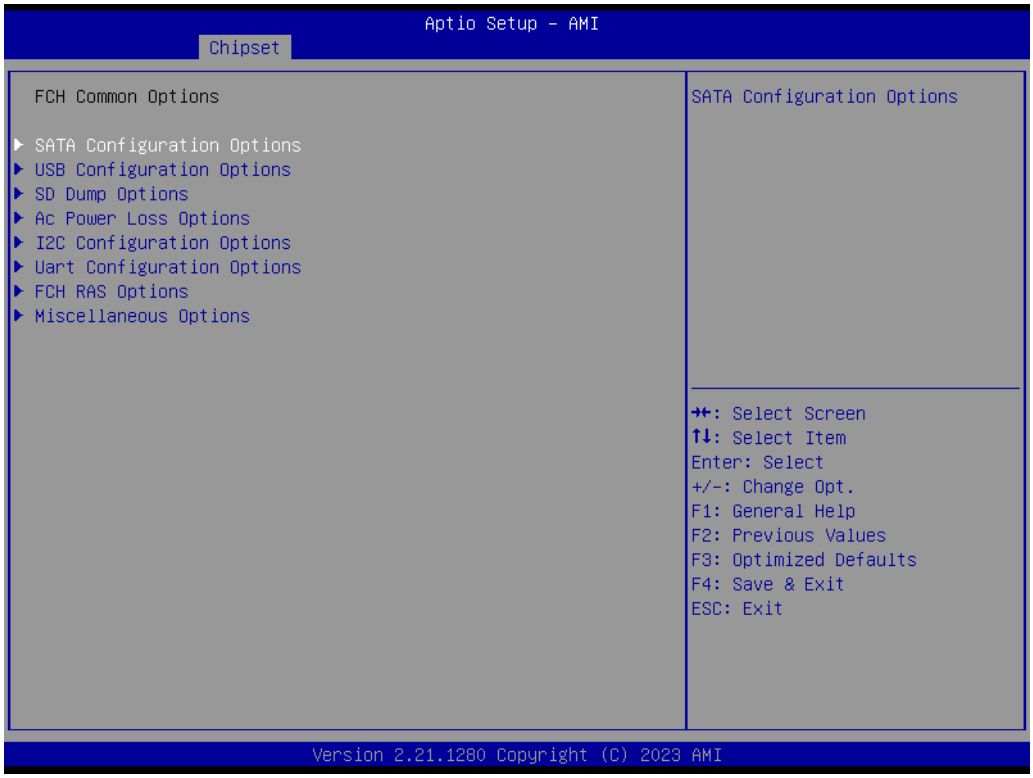


Figure 3.67 FCH Common Options

- **SATA Configuration Options**
  SATA configuration options.
- **USB Configuration Options**
  USB configuration options.
- **SD Dump Options**
  SD dump options.
- **Ac Power Loss Options**
  Ac power loss options.
- **I2C Configuration Options**
  I2C configuration options.
- **Uart Configuration Options**
  Uart configuration options.
- **FCH RAS Options**
  FCH RAS options.
- **Miscellaneous Options**
  Miscellaneous options.

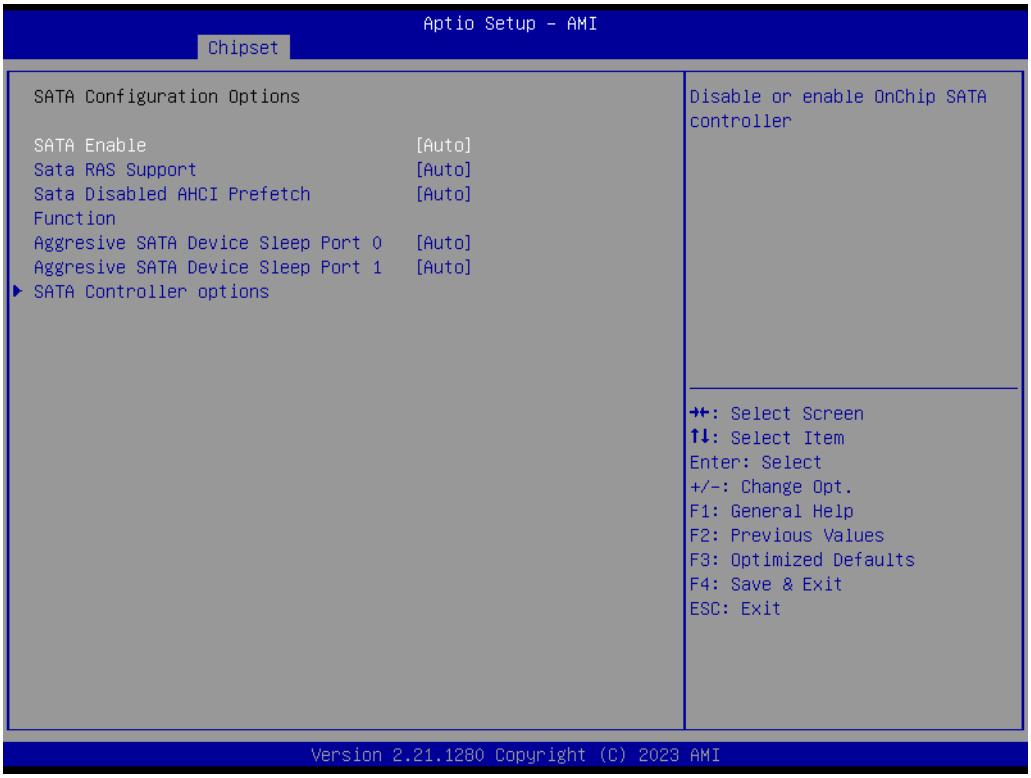


Figure 3.68 SATA Configuration Options

- **SATA Enable**
  Enable or disable OnChip SATA controller.
- **Sata RAS Support**
  Enable or disable Sata RAS support.
- **Sata Disabled AHCI Prefetch Function**
  Enable or disable Sata disabled AHCI prefetch function.
- **Aggresive SATA Device Sleep Port 0**
  Enable or disable aggressive SATA device sleep on port 0.
- **Aggresive SATA Device Sleep Port 1**
  Enable or disable aggressive SATA device sleep on port 1.
- **SATA Controller options**
  SATA Controller options.

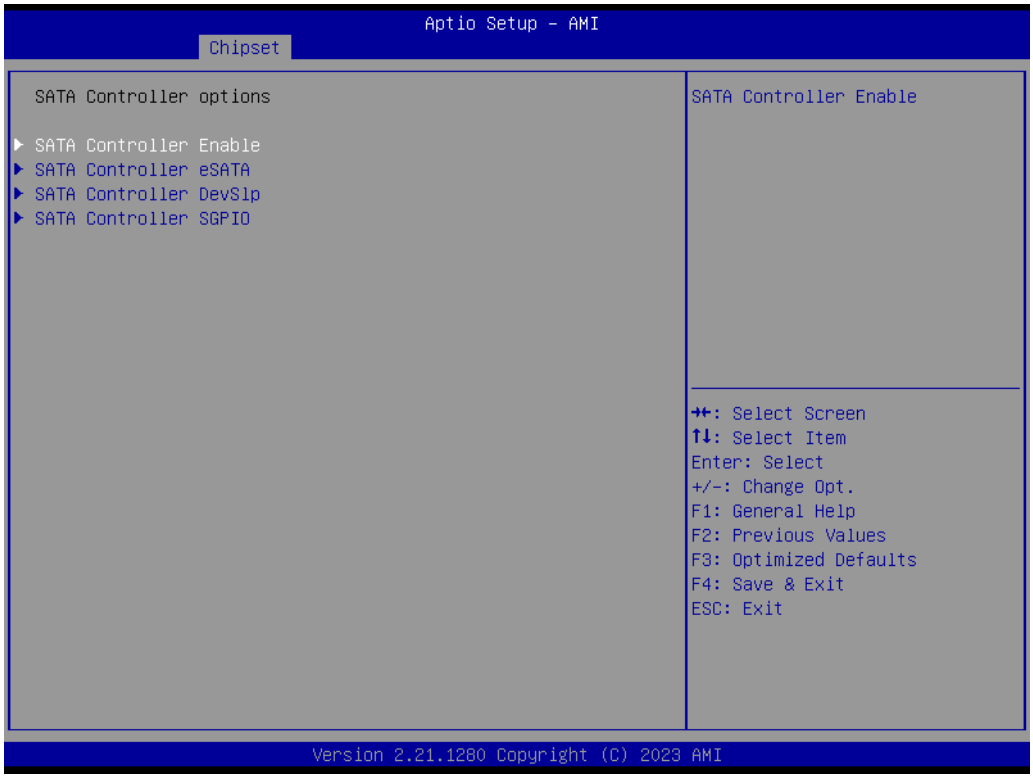


Figure 3.69 SATA Controller options

- **SATA Controller Enable**
  SATA controller enable.
- **SATA Controller eSATA**
  SATA controller eSATA.
- **SATA Controller DevSlp**
  SATA controller DevSlp.
- **SATA Controller SGPIO**
  SATA controller SGPIO.

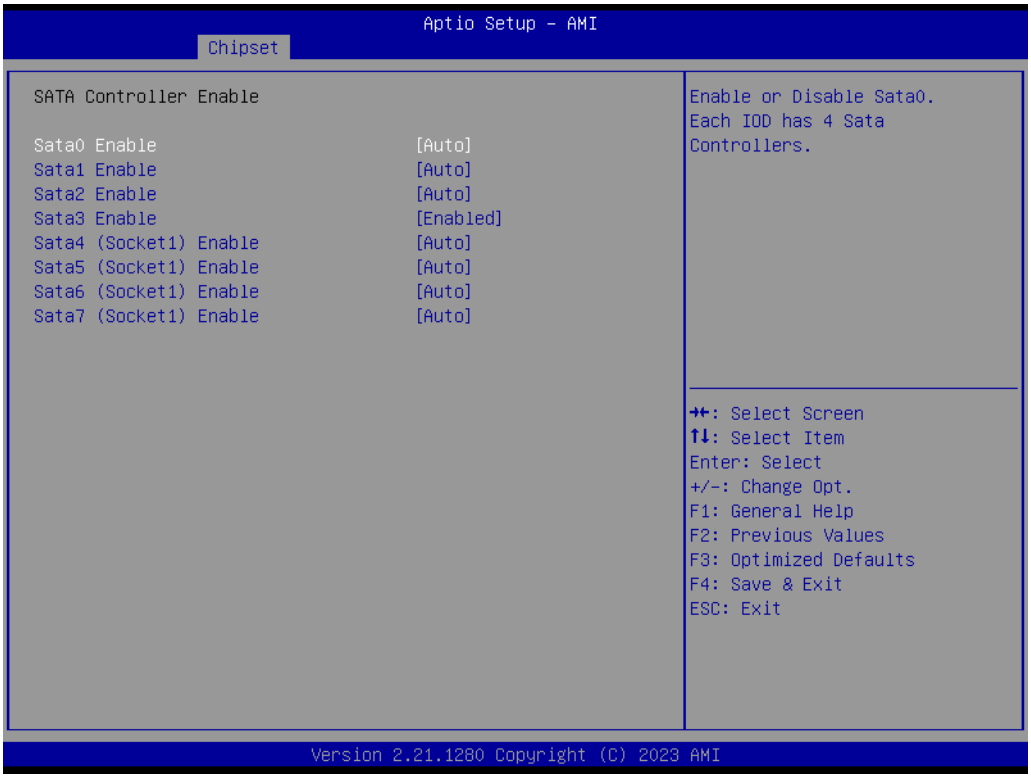


Figure 3.70 SATA Controller Enable

- **Sata0 Enable**
  Enable or disable Sata0. Each IOD has 4 Sata Controllers.
- **Sata1 Enable**
  Enable or disableSata1. Each IOD has 4 Sata Controllers.
- **Sata2 Enable**
  Enable or disable Sata2. Each IOD has 4 Sata Controllers.
- **Sata3 Enable**
  Enable or disable Sata3. Each IOD has 4 Sata Controllers.
- **Sata4 (Socket1) Enable**
  Enable or disable Sata4 on Socket 1 (IOD1).. Each IOD has 4 Sata Controllers.
- **Sata5 (Socket1) Enable**
  Enable or disable Sata5 on Socket 1 (IOD1).. Each IOD has 4 Sata Controllers.
- **Sata6 (Socket1) Enable**
  Enable or disable Sata6 on Socket 1 (IOD1).. Each IOD has 4 Sata Controllers.
- **Sata7 (Socket1) Enable**
  Enable or disable Sata7 on Socket 1 (IOD1).. Each IOD has 4 Sata Controllers.

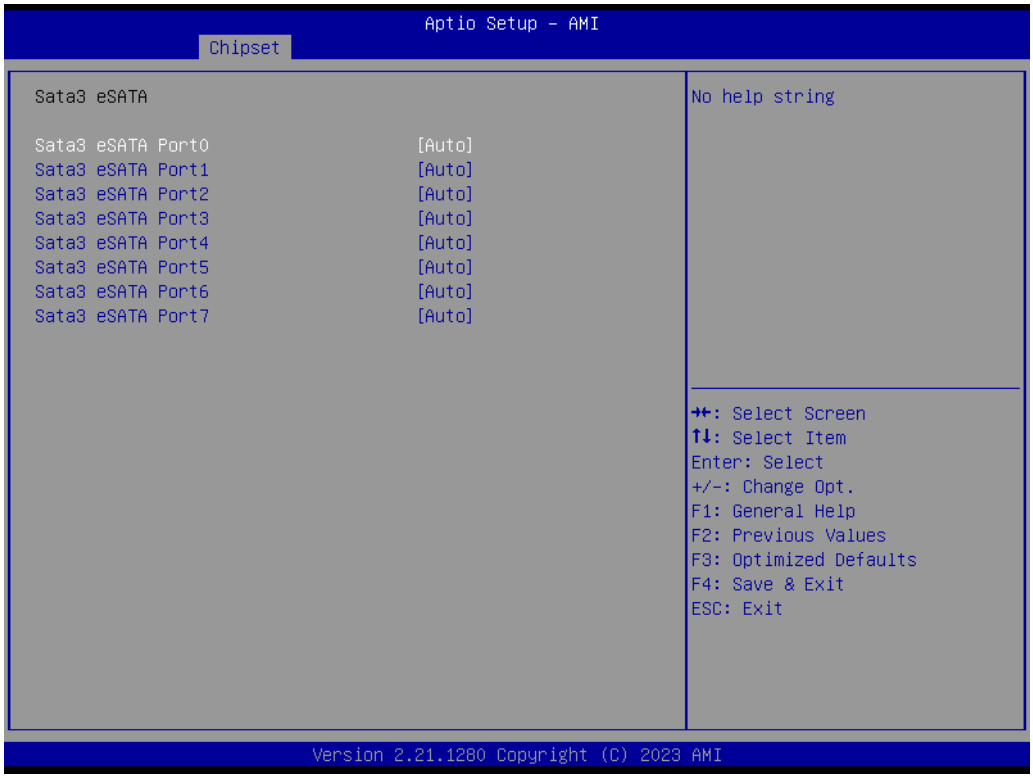


Figure 3.71 Sata3 eSATA

- **Sata3 eSATA Port0**
  No help string.
- **Sata3 eSATA Port1**
  No help string.
- **Sata3 eSATA Port2**
  No help string.
- **Sata3 eSATA Port3**
  No help string.
- **Sata3 eSATA Port4**
  No help string.
- **Sata3 eSATA Port5**
  No help string.
- **Sata3 eSATA Port6**
  No help string.
- **Sata3 eSATA Port7**
  No help string.

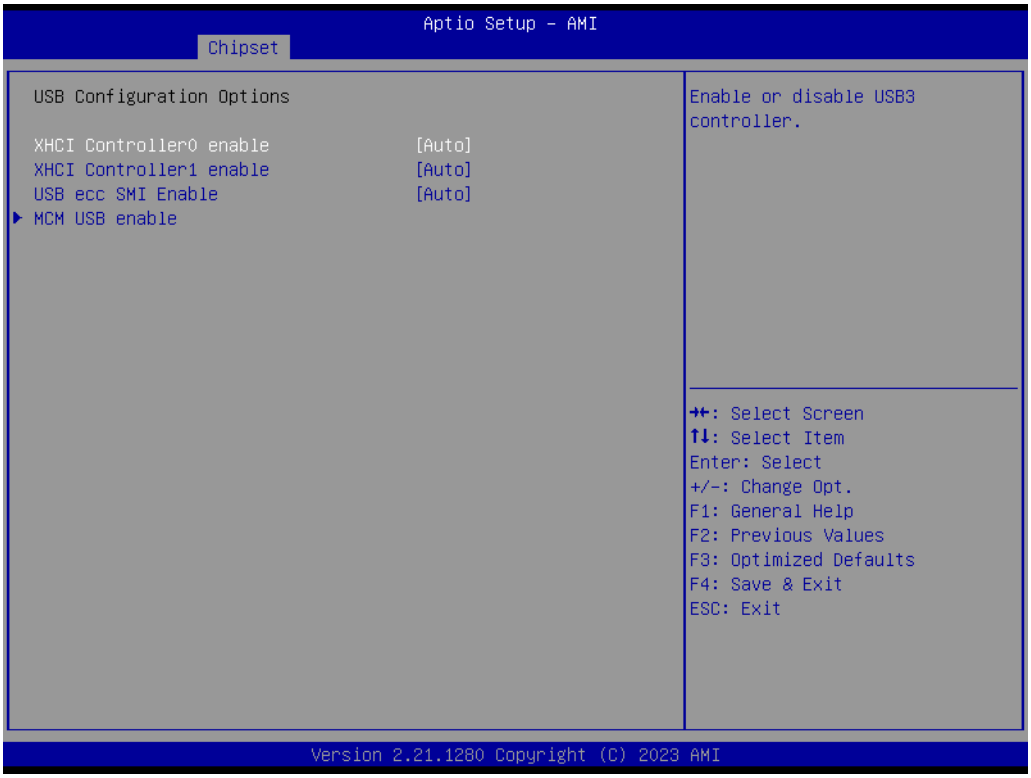


Figure 3.72 USB Configuration Options

- **XHCI Controller0 enable**
  Enable or disable USB3 controller.
- **XHCI Controller1 enable**
  Enable or disable USB3 controller.
- **USB ecc SMI Enable**
  Enable or disable USB ecc SMI.
- **MCM USB enable**
  MCM USB enable.

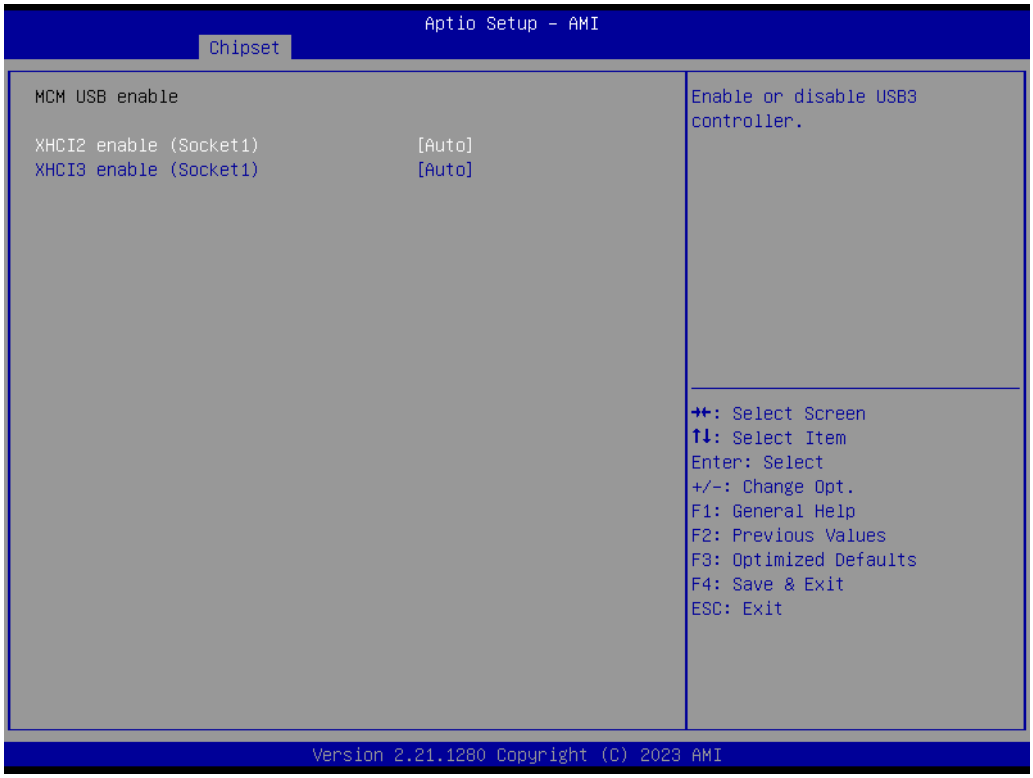


Figure 3.73 MCM USB enable

- **XHCI2 enable (Socket1)**
  Enable or disable USB3 controller.
- **XHCI3 enable (Socket1)**
  Enable or disable USB3 controller.

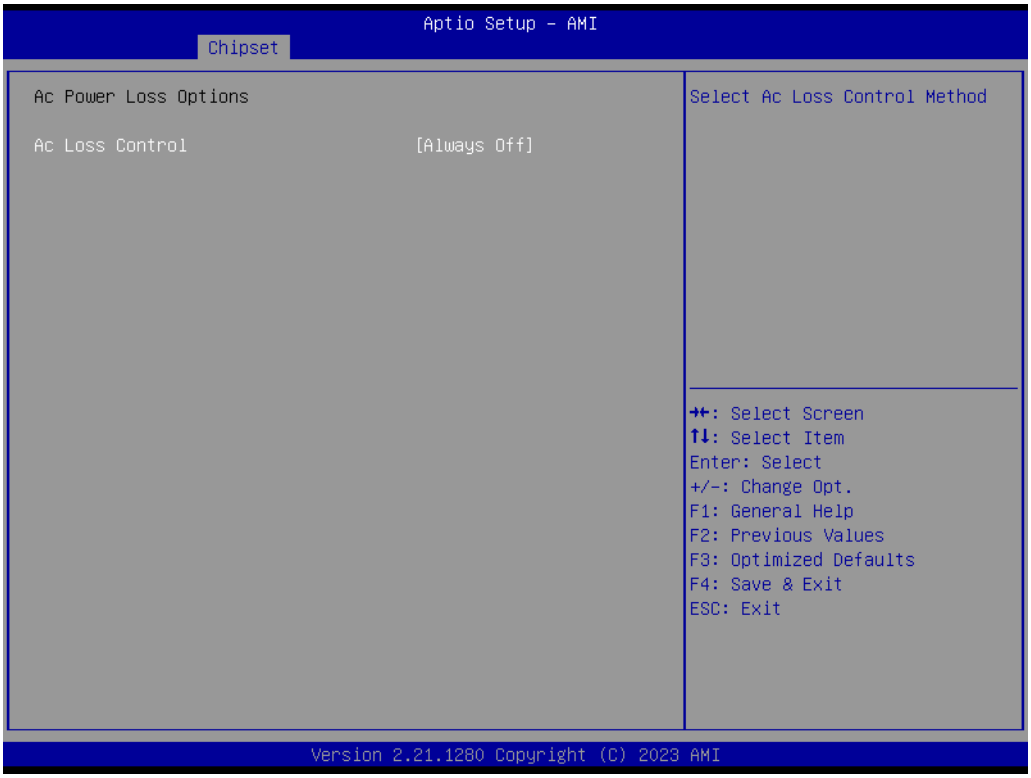


Figure 3.74 Ac Power Loss Options

- **Ac Loss Control**
  Select Ac Loss Control method.

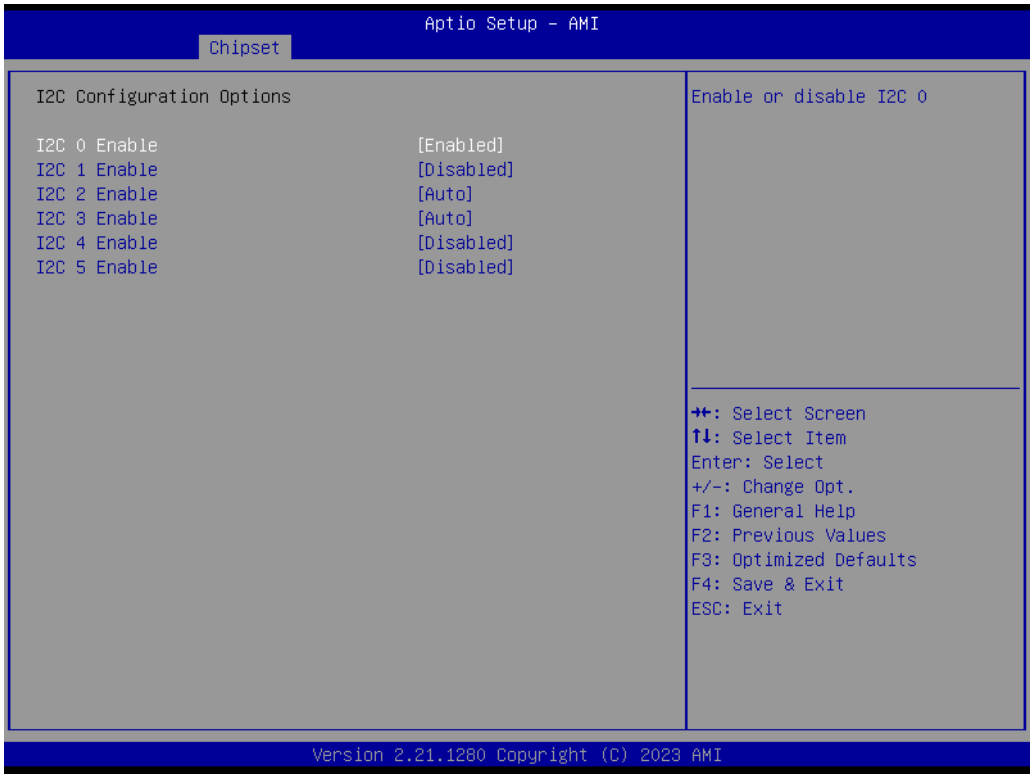


Figure 3.75 I2C Configuration Options

- **I2C 0 Enable**
  Enable or disable I2C 0.
- **I2C 1 Enable**
  Enable or disable I2C 1.
- **I2C 2 Enable**
  Enable or disable I2C 2.
- **I2C 3 Enable**
  Enable or disable I2C 3.
- **I2C 4 Enable**
  Enable or disable I2C 4.
- **I2C 5 Enable**
  Enable or disable I2C 5.

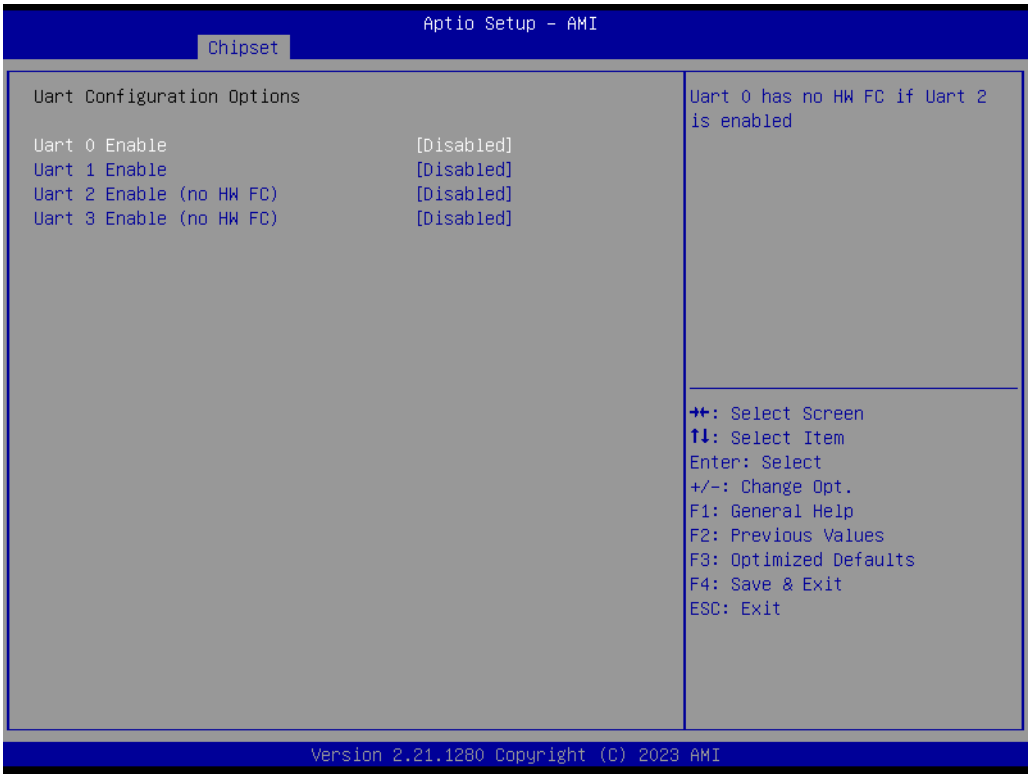


Figure 3.76 Uart Configuration Options

- **Uart 0 Enable**
  Uart 0 has no HW FC if Uart 2 is enabled.
- **Uart 1 Enable**
  Uart 1 has no HW FC if Uart 3 is enabled.
- **Uart 2 Enable (no HW FC)**
  Uart 2 has no HW FC if Uart 0 is enabled.
- **Uart 3 Enable (no HW FC)**
  Uart 3 has no HW FC if Uart 1 is enabled.

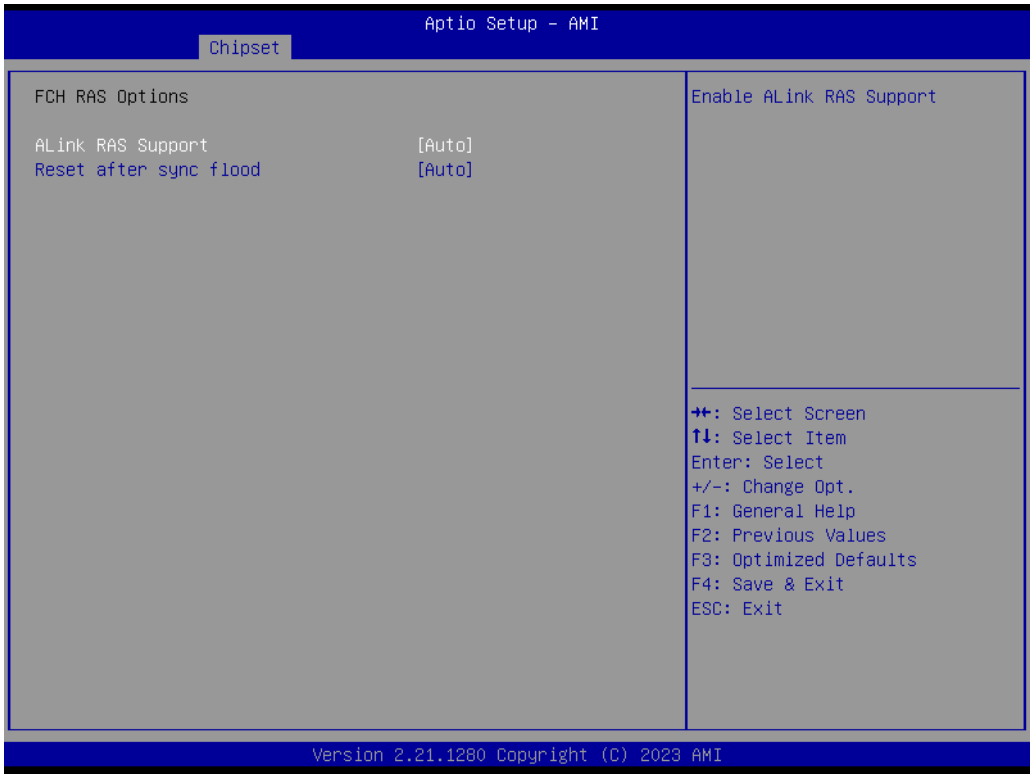


Figure 3.77 FCH RAS Options

- **ALink RAS Support**
  Enable ALink RAS support.
- **Reset after sync flood**
  Enable AB to forward downstream sync-flood message to system controller.

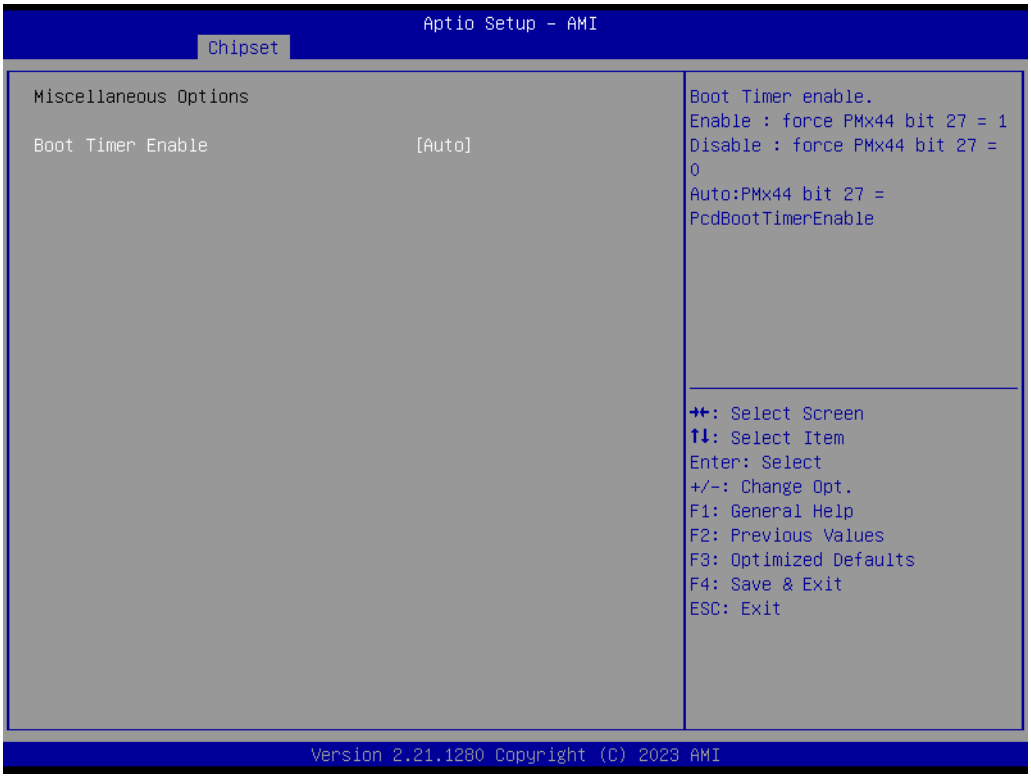


Figure 3.78 Miscellaneous Options

- **Boot Timer Enable**
  Boot Timer enable.
  Enable: force PMx44 bit 27 = 1
  Disable: force PMx44 bit 27 = 0.
  Auto:PMx44 bit 27 = PcdBootTimerEnable.

3.2.3.5 North Bridge

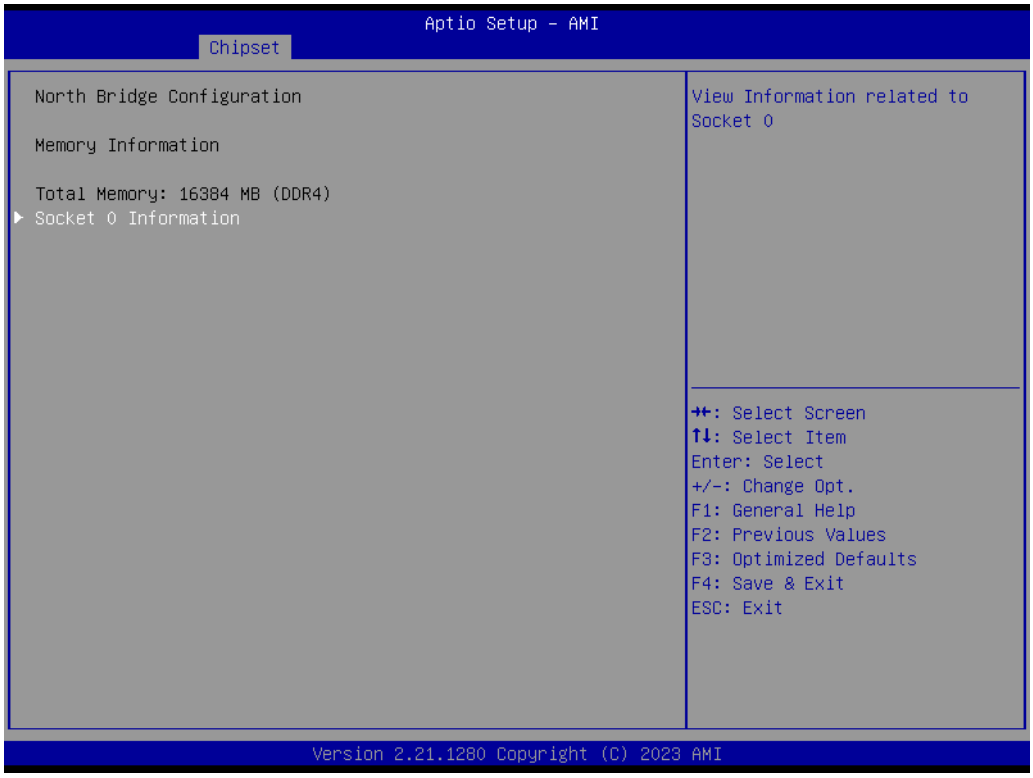


Figure 3.79 North Bridge

- **Socket 0 Information**
  View Information related to Socket 0.

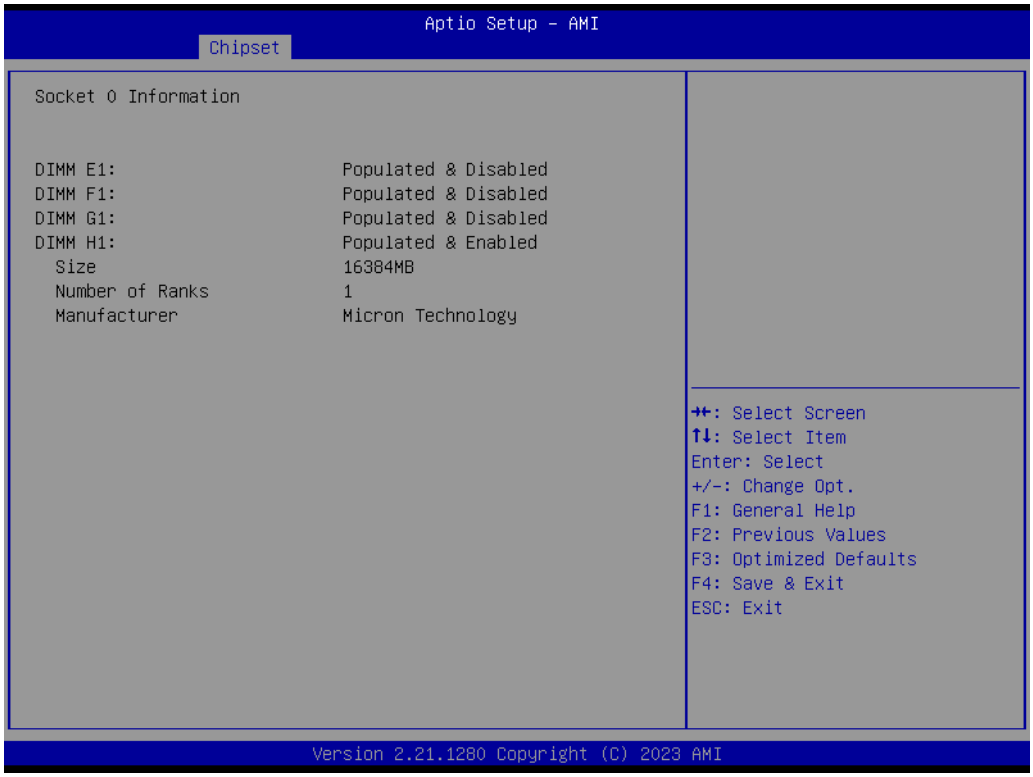


Figure 3.80 Socket 0 Information

3.2.4 Security Chipset

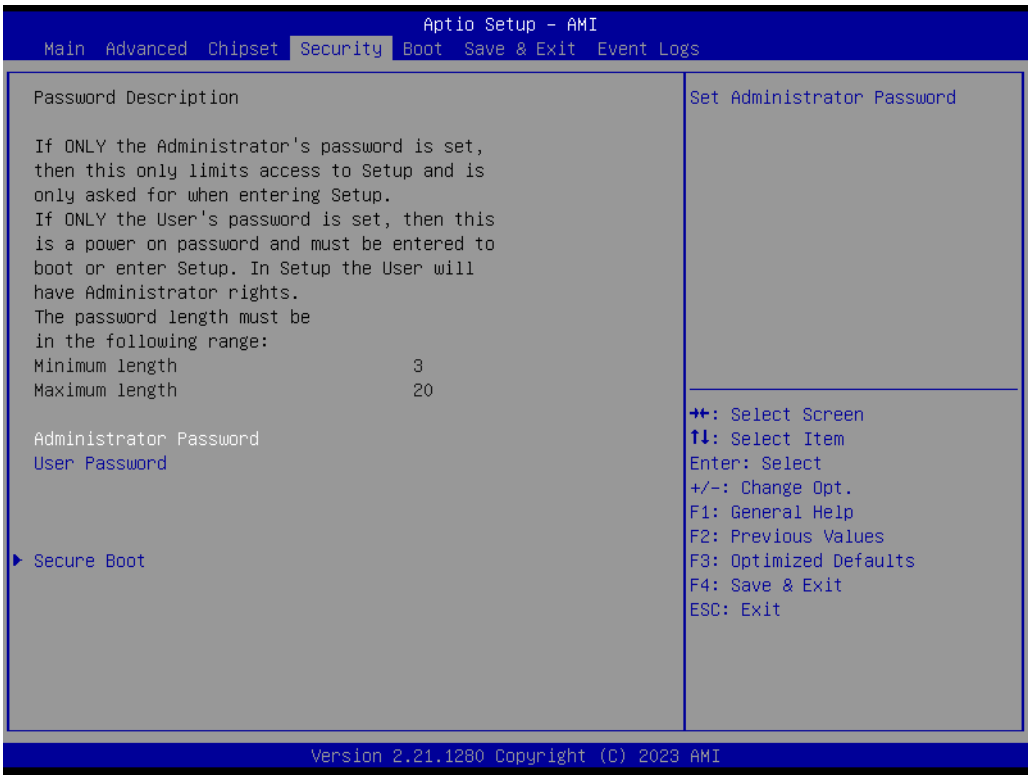


Figure 3.81 Security

- **Administrator Password**
  Set administrator password.
- **User Password**
  Set user password.
- **Secure Boot**
  Secure boot configuration.

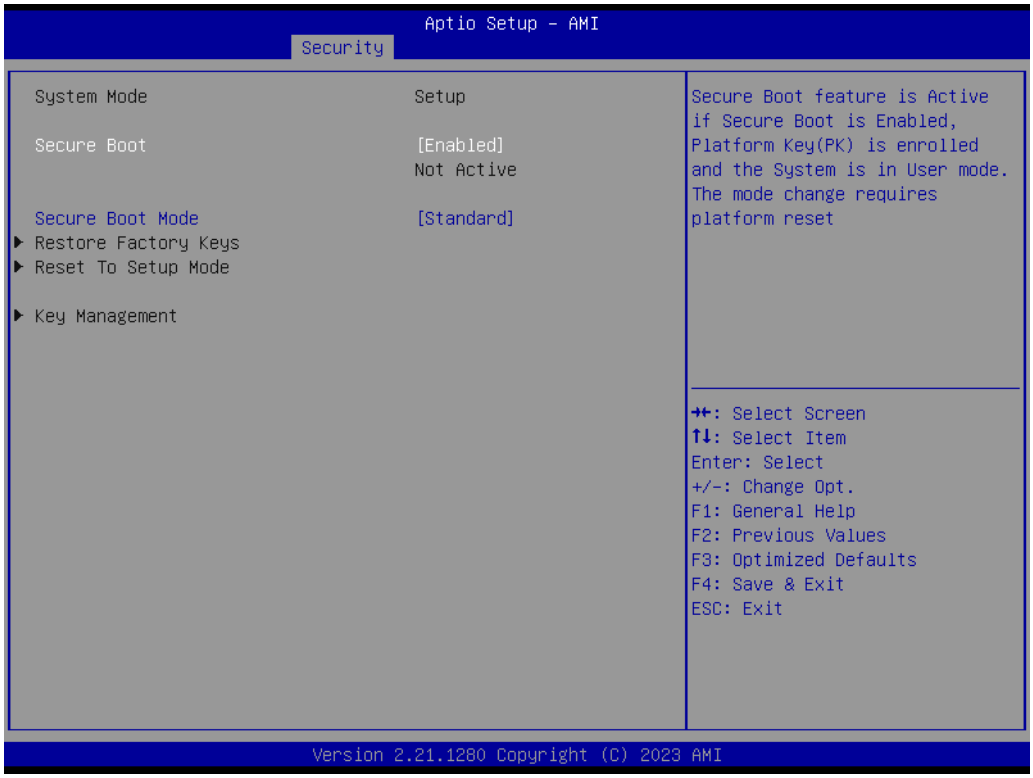


Figure 3.82 Secure Boot

- **Secure Boot**
  Secure Boot feature is Active if Secure Boot is Enabled.
  Platform Key(PK) is enrolled and the System is in User mode.
  The mode change requires platform reset.
- **Secure Boot Mode**
  Secure Boot mode options:
  Standard or Custom.
  In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.

3.2.5 Boot Setup

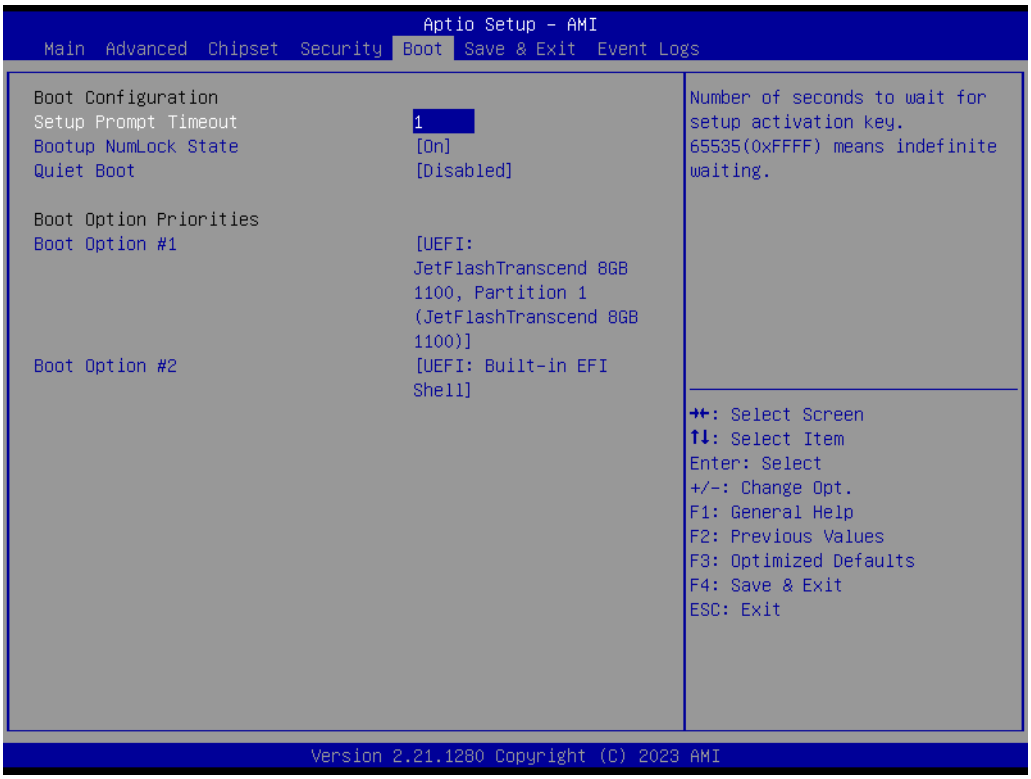


Figure 3.83 Boot

- **Setup Prompt Timeout**
  Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
- **Bootup NumLock State**
  Select the keyboard NumLock state.
- **Quiet Boot**
  Enables or disables Quiet Boot option.
- **Boot Option #1**
  Sets the system boot order.

3.2.6 Save & Exit

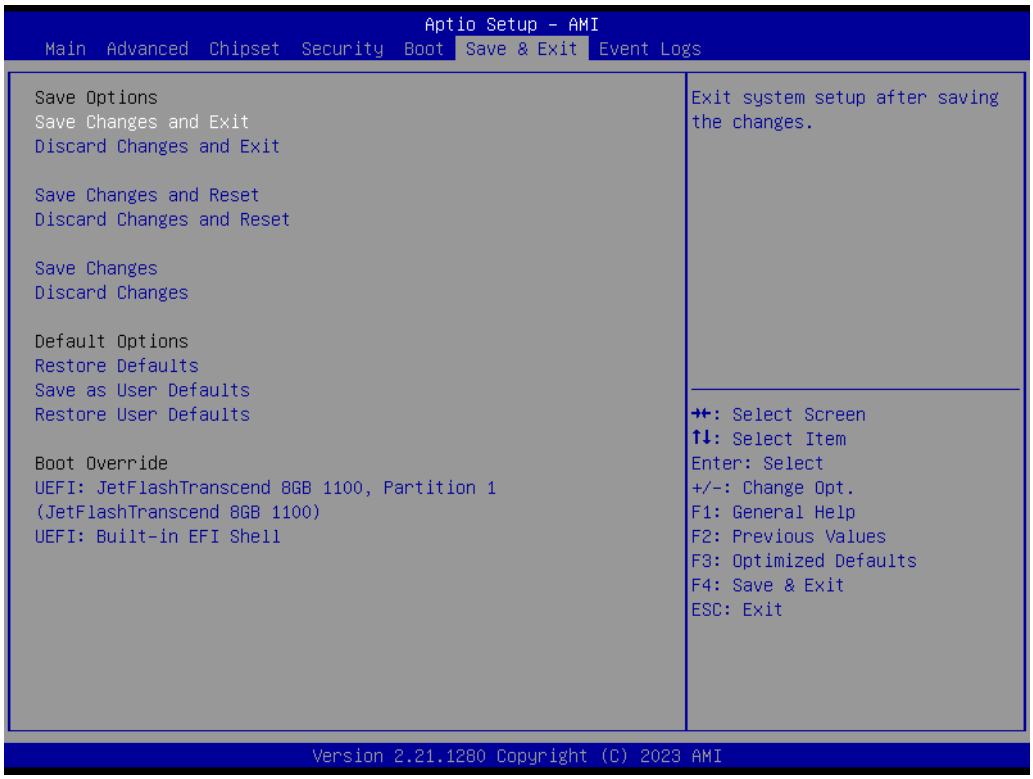


Figure 3.84 Save & Exit

- **Save Changes and Exit**
  Exit system setup after saving the changes.
- **Discard Changes and Exit**
  Exit system setup without saving any changes.
- **Save Changes and Reset**
  Reset the system after saving the changes.
- **Discard Changes and Reset**
  Reset system setup without saving any changes.
- **Save Changes**
  Save Changes done so far to any of the setup options.
- **Discard Changes**
  Discard Changes done so far to any of the setup options.
- **Restore Defaults**
  Restore/Load Default values for all the setup options.
- **Save as User Defaults**
  Save the changes done so far as User Defaults.
- **Restore User Defaults**
  Restore the User Defaults to all the setup options.

3.2.7 Event Logs

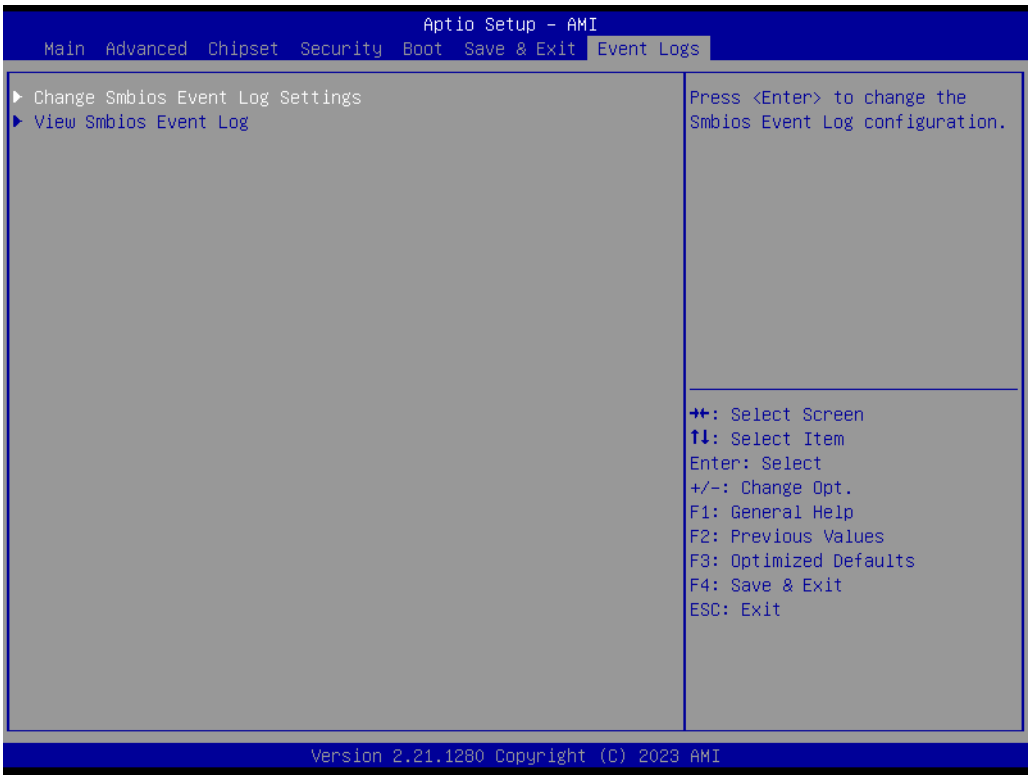


Figure 3.85 Event Logs

- **Change Smbios Event Log Settings**
  Press <Enter> to change the Smbios Event Log configuration.
- **View Smbios Event Log**
  Press <Enter> to view the Smbios Event Log records.

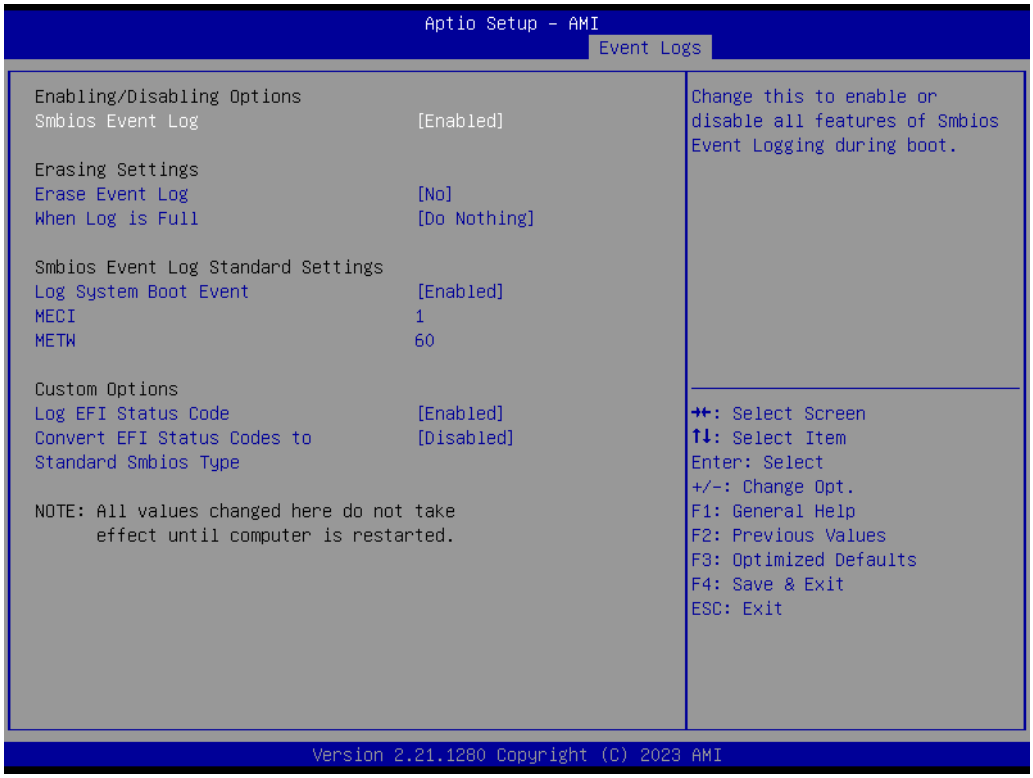


Figure 3.86 Change Smbios Event Log Settings

- **Smbios Event Log**
  Change this to enable or disable all features of Smbios Event Logging during boot.
- **Erase Event Log**
  Choose options for erasing Smbios Event Log. Erasing is done prior to any logging activation during reset.
- **When Log is Full**
  Choose options for reactions to a full Smbios Event Log.
- **Log System Boot Event**
  Choose option to enable/disable logging of System boot event
- **MECI**
  Mutiple Event Count Increment: The number of occurrences of a duplicate event that must pass before the multiple-event counter of log entry is updated.The value ranges from 1 to 255.
- **METW**
  Mutiple Event Time Window: The number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes.
- **Log EFI Status Code**
  Enable or disable the logging of EFI Status Codes as OEM reserved type E0 (if not already converted to legacy).
- **Convert EFI Status Codes to Standard Smbios Type**
  Enable or disable the converting of EFI Status Codes to Standard Smbios Types (Not all may be translated).

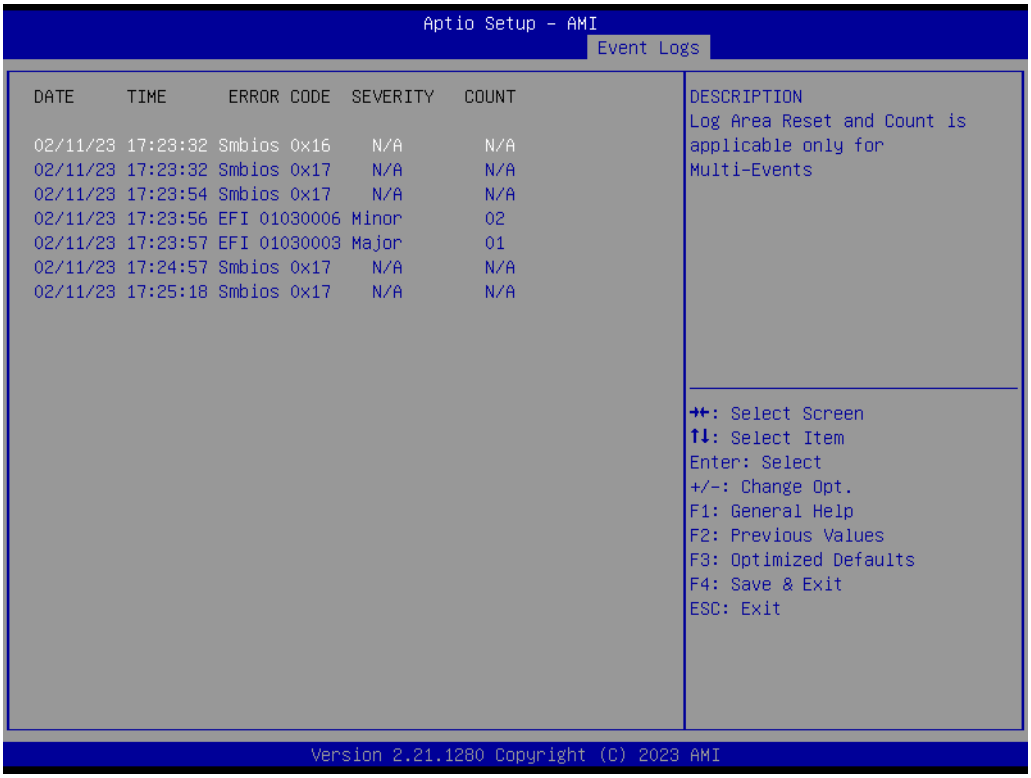


Figure 3.87 View Smbios Event Log

Chapter 4

S/W Introduction and Installation

- S/W Introduction
- Driver Installation
- Advantech iManager

4.1 S/W Introduction

Advantech Embedded Software Services is dedicated to enriching the quality of life through the fusion of Advantech platforms and Microsoft Windows embedded technology. Our mission involves empowering the embedded computing community by seamlessly integrating Windows Embedded software products into Advantech platforms. By doing so, we relieve customers from the complexities of managing multiple vendors, including hardware suppliers, system integrators, and embedded OS distributors. Ultimately, our objective is to make Windows Embedded Software solutions effortlessly accessible and broadly accessible to the embedded computing community.

4.2 Driver Installation

The Intel Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured.

4.2.1 Windows Driver Setup

To install the drivers on a windows-based OS, please connect to the Internet and go to http://support.advantech.com.tw to download the drivers that you want to install and follow the Driver Setup instructions to complete the installation.

4.2.2 Other OS

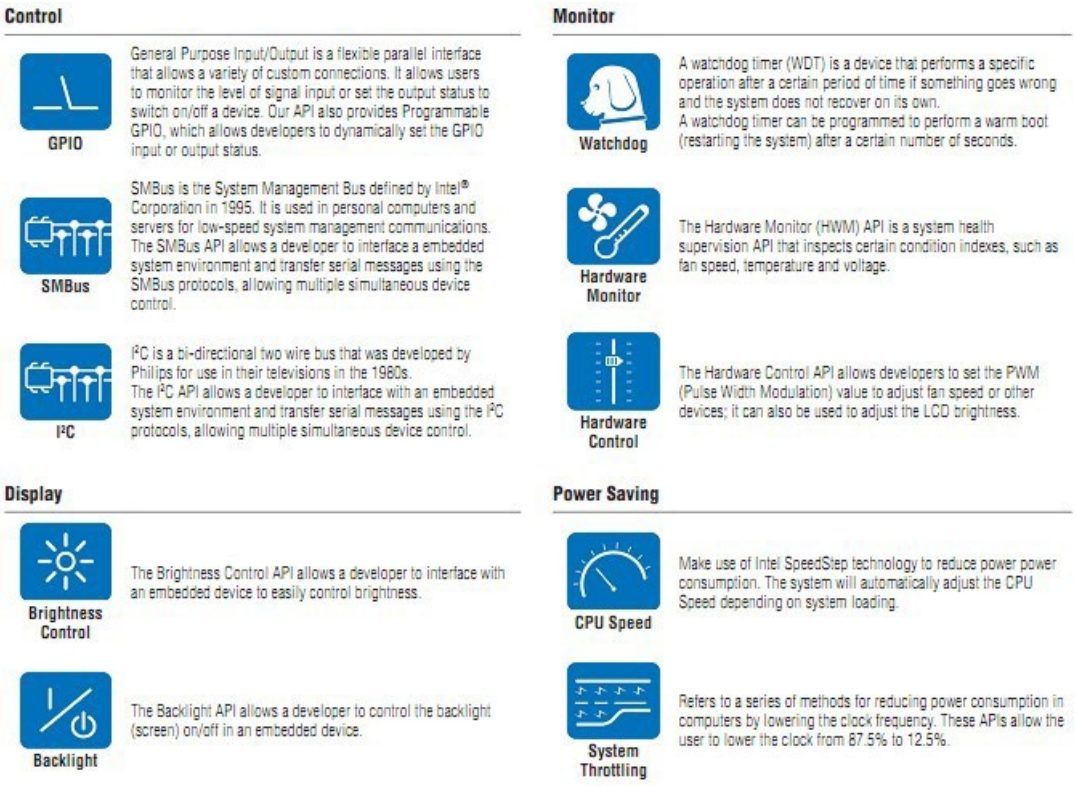
Linux Ubuntu

4.3 Advantech iManager

Advantech's platforms are equipped with iManager, a micro-controller that offers embedded capabilities for system integrators. These embedded features have been shifted from the OS/BIOS level to the board level, enhancing reliability and streamlining integration.

iManager operates independently of the operating system, capable of tracking boot times and device running hours, monitoring device health, and offering an advanced watchdog to promptly address errors. Furthermore, iManager includes a secure and encrypted EEPROM for safeguarding critical security keys and customer data.

All embedded functions can be configured through the API, providing corresponding utilities for demonstration. These APIs adhere to the PICMG EAPI (Embedded Application Programmable Interface) standards, simplifying the integration of these embedded features, expediting development schedules, and ensuring software continuity when upgrading hardware. For more in-depth guidance on utilizing the APIs and utilities, please consult the Advantech iManager 2.0 Software API User Manual.



Appendix A

Pin Assignment

This appendix details information about the hardware pin assignments of the SOM-E780 CPU System on Module.

Sections include:

- SOM-E780 Pin Assignments

A.1 SOM-E780 Pin Assignments

This section gives SOM-E780 pin assignments on COM HPC connector which is compliant with COM-HPC® Server Size E module with proprietary pinout definitions. For more details about how to use these pins and get design reference, please contact Advantech for a design guide, checklist, reference schematic, and other hardware/software supports.

Table A.1: J1 Connector Rows A and B

Pin#	Row A Description	SOM-E780 Difference	Pin#	Row B Description	SOM-E780 Difference
J1.A1	VCC		J1.B1	VCC	
J1.A2	VCC		J1.B2	PWRBTN#	
J1.A3	VCC		J1.B3	VCC	
J1.A4	VCC		J1.B4	THERMTRIP#	
J1.A5	VCC		J1.B5	VCC	
J1.A6	VCC		J1.B6	TAMPER#	
J1.A7	VCC		J1.B7	VCC	
J1.A8	VCC		J1.B8	SUS_S3#	
J1.A9	VCC		J1.B9	VCC	
J1.A10	GND		J1.B10	WD_STROBE#	
J1.A11	BATLOW#		J1.B11	WD_OUT	
J1.A12	PLTRST#		J1.B12	GND	
J1.A13	GND		J1.B13	USB5-	NA
J1.A14	USB7-	NA	J1.B14	USB5+	NA
J1.A15	USB7+	NA	J1.B15	GND	
J1.A16	GND		J1.B16	USB4-	NA
J1.A17	USB6-	NA	J1.B17	USB4+	NA
J1.A18	USB6+	NA	J1.B18	GND	
J1.A19	GND		J1.B19	RSVD	
J1.A20	ETH4_RX-	A_PCIe0_TX-	J1.B20	RSVD	
J1.A21	ETH4_RX+	A_PCIe0_TX+	J1.B21	RSVD	
J1.A22	GND		J1.B22	RSVD	VCC_5V_SBY
J1.A23	ETH5_RX-	A_PCIe1_TX-	J1.B23	RSVD	VCC_5V_SBY
J1.A24	ETH5_RX+	A_PCIe1_TX+	J1.B24	VCC_5V_SBY	
J1.A25	GND		J1.B25	USB67_OC#	NA
J1.A26	ETH6_RX-	A_PCIe2_TX-	J1.B26	USB45_OC#	NA
J1.A27	ETH6_RX+	A_PCIe2_TX+	J1.B27	USB23_OC#	
J1.A28	GND		J1.B28	USB01_OC#	
J1.A29	ETH7_RX-	A_PCIe3_TX-	J1.B29	SML1_CLK	NA
J1.A30	ETH7_RX+	A_PCIe3_TX+	J1.B30	SML1_DAT	NA
J1.A31	GND		J1.B31	PMCALERT#	NA
J1.A32	RSVD	EN_12V_CB	J1.B32	SML0_CLK	NA
J1.A33	RSVD		J1.B33	SML0_DAT	NA
J1.A34	GND		J1.B34	USB_P-D_ALERT#	NA
J1.A35	ETH4_TX-	A_PCIe4_TX-	J1.B35	USB_PD_I2C_-CLK	NA

Table A.1: J1 Connector Rows A and B					
J1.A36	ETH4_TX+	A_PCIe4_TX+	J1.B36	USB_PD_I2C_-DAT	NA
J1.A37	GND		J1.B37	USB_RT_ENA	NA
J1.A38	ETH5_TX-	A_PCIe5_TX-	J1.B38	USB1_LSRX	NA
J1.A39	ETH5_TX+	A_PCIe5_TX+	J1.B39	USB1_LSTX	NA
J1.A40	GND		J1.B40	USB0_LSRX	NA
J1.A41	ETH6_TX-	A_PCIe6_TX-	J1.B41	USB0_LSTX	NA
J1.A42	ETH6_TX+	A_PCIe6_TX+	J1.B42	GND	
J1.A43	GND		J1.B43	USB0_AUX-	NA
J1.A44	ETH7_TX-	A_PCIe7_TX-	J1.B44	USB0_AUX+	NA
J1.A45	ETH7_TX+	A_PCIe7_TX+	J1.B45	RSVD	
J1.A46	GND		J1.B46	RSVD	
J1.A47	USB1_AUX-	NA	J1.B47	VCC_BOOT_SPI	
J1.A48	USB1_AUX+	NA	J1.B48	BOOT_SPI_CS#	
J1.A49	GND		J1.B49	BSEL0	
J1.A50	eSPI_IO0	LPC_LAD0	J1.B50	BSEL1	
J1.A51	eSPI_IO1	LPC_LAD1	J1.B51	BSEL2	
J1.A52	eSPI_IO2	LPC_LAD2	J1.B52	eSPI_ALERT0#	LPC_SERIRQ
J1.A53	eSPI_IO3	LPC_LAD3	J1.B53	eSPI_ALERT1#	NA
J1.A54	eSPI_CLK	P0_LPCCLK1	J1.B54	eSPI_CS0#	LPC_LFRAM E
J1.A55	GND		J1.B55	eSPI_CS1#	NA
J1.A56	PCIe_-CLKREQ0_LO#	NA	J1.B56	eSPI_RST#	LPC_RST
J1.A57	PCIe_-CLKREQ0_HI#	NA	J1.B57	GND	
J1.A58	GND		J1.B58	PCIe_BMC_RX-	
J1.A59	PCIe_BMC_TX-		J1.B59	PCIe_BMC_RX+	
J1.A60	PCIe_BMC_TX+		J1.B60	GND	
J1.A61	GND		J1.B61	PCIe08_RX-	
J1.A62	PCIe08_TX-		J1.B62	PCIe08_RX+	
J1.A63	PCIe08_TX+		J1.B63	GND	
J1.A64	GND		J1.B64	PCIe09_RX-	
J1.A65	PCIe09_TX-		J1.B65	PCIe09_RX+	
J1.A66	PCIe09_TX+		J1.B66	GND	
J1.A67	GND		J1.B67	PCIe10_RX-	
J1.A68	PCIe10_TX-		J1.B68	PCIe10_RX+	
J1.A69	PCIe10_TX+		J1.B69	GND	
J1.A70	GND		J1.B70	PCIe11_RX-	
J1.A71	PCIe11_TX-		J1.B71	PCIe11_RX+	
J1.A72	PCIe11_TX+		J1.B72	GND	
J1.A73	GND		J1.B73	PCIe12_RX-	
J1.A74	PCIe12_TX-		J1.B74	PCIe12_RX+	
J1.A75	PCIe12_TX+		J1.B75	GND	
J1.A76	GND		J1.B76	PCIe13_RX-	
J1.A77	PCIe13_TX-		J1.B77	PCIe13_RX+	
J1.A78	PCIe13_TX+		J1.B78	GND	
J1.A79	GND		J1.B79	PCIe14_RX-	
J1.A80	PCIe14_TX-		J1.B80	PCIe14_RX+	

Table A.1: J1 Connector Rows A and B					
J1.A81	PCIe14_TX+		J1.B81	GND	
J1.A82	GND		J1.B82	PCIe15_RX-	
J1.A83	PCIe15_TX-		J1.B83	PCIe15_RX+	
J1.A84	PCIe15_TX+		J1.B84	GND	
J1.A85	GND		J1.B85	TEST#	NA
J1.A86	VCC_RTC		J1.B86	RSMRST_OUT#	
J1.A87	SUS_CLK	NA	J1.B87	UART1_TX	
J1.A88	GPIO_00		J1.B88	UART1_RX	
J1.A89	GPIO_01		J1.B89	UART1_RTS#	
J1.A90	GPIO_02		J1.B90	UART1_CTS#	
J1.A91	GPIO_03		J1.B91	IPMB_CLK	
J1.A92	GPIO_04		J1.B92	IPMB_DAT	
J1.A93	GPIO_05		J1.B93	GP_SPI_MOSI	NA
J1.A94	GPIO_06		J1.B94	GP_SPI_MISO	NA
J1.A95	GPIO_07		J1.B95	GP_SPI_CS0#	NA
J1.A96	GPIO_08		J1.B96	GP_SPI_CS1#	NA
J1.A97	GPIO_09		J1.B97	GP_SPI_CS2#	NA
J1.A98	GPIO_10		J1.B98	GP_SPI_CS3#	NA
J1.A99	GPIO_11		J1.B99	GP_SPI_CLK	NA
J1.A100	TYPE0		J1.B100	GP_SPI_ALERT#	NA

Table A.2: J1 Connector Rows C and D					
Pin#	**Row C Description**	**SOM-E780 Difference**	**Pin#**	**Row D Description**	**SOM-E780 Difference**
J1.C1	VCC		J1.D1	VCC	
J1.C2	RSTBTN#		J1.D2	VCC	
J1.C3	VCC		J1.D3	VCC	
J1.C4	CARRIER_HOT#		J1.D4	VCC	
J1.C5	VCC		J1.D5	VCC	
J1.C6	VIN_PWROK		J1.D6	VCC	
J1.C7	VCC		J1.D7	VCC	
J1.C8	SUS_S4_S5#		J1.D8	VCC	
J1.C9	VCC		J1.D9	VCC	
J1.C10	GND		J1.D10	WAKE0#	
J1.C11	FAN_PWMOUT		J1.D11	WAKE1#	
J1.C12	FAN_TACHIN		J1.D12	GND	
J1.C13	GND		J1.D13	USB1-	
J1.C14	USB3-		J1.D14	USB1+	
J1.C15	USB3+		J1.D15	GND	
J1.C16	GND		J1.D16	USB0-	
J1.C17	USB2-		J1.D17	USB0+	
J1.C18	USB2+		J1.D18	GND	
J1.C19	GND		J1.D19	ETH0_RX-	A_PCIe4_RX-
J1.C20	ETH0_TX-	A_PCIe0_RX-	J1.D20	ETH0_RX+	A_PCIe4_RX+
J1.C21	ETH0_TX+	A_PCIe0_RX+	J1.D21	GND	
J1.C22	GND		J1.D22	ETH1_RX-	A_PCIe5_RX-

Table A.2: J1 Connector Rows C and D					
J1.C23	ETH1_TX-	A_PCIe1_RX-	J1.D23	ETH1_RX+	A_PCIe5_RX+
J1.C24	ETH1_TX+	A_PCIe1_RX+	J1.D24	GND	
J1.C25	GND		J1.D25	ETH2_RX-	A_PCIe6_RX-
J1.C26	ETH2_TX-	A_PCIe2_RX-	J1.D26	ETH2_RX+	A_PCIe6_RX+
J1.C27	ETH2_TX+	A_PCIe2_RX+	J1.D27	GND	
J1.C28	GND		J1.D28	ETH3_RX-	A_PCIe7_RX-
J1.C29	ETH3_TX-	A_PCIe3_RX-	J1.D29	ETH3_RX+	A_PCIe7_RX+
J1.C30	ETH3_TX+	A_PCIe3_RX+	J1.D30	GND	
J1.C31	GND		J1.D31	USB3_SSTX-	
J1.C32	USB3_SSRX-		J1.D32	USB3_SSTX+	
J1.C33	USB3_SSRX+		J1.D33	GND	
J1.C34	GND		J1.D34	USB2_SSTX-	
J1.C35	USB2_SSRX-		J1.D35	USB2_SSTX+	
J1.C36	USB2_SSRX+		J1.D36	GND	
J1.C37	GND		J1.D37	USB1_SSTX0-	
J1.C38	USB1_SSRX0-		J1.D38	USB1_SSTX0+	
J1.C39	USB1_SSRX0+		J1.D39	GND	
J1.C40	GND		J1.D40	USB1_SSTX1-	NA
J1.C41	USB1_SSRX1-	NA	J1.D41	USB1_SSTX1+	NA
J1.C42	USB1_SSRX1+	NA	J1.D42	GND	
J1.C43	GND		J1.D43	USB0_SSTX0-	
J1.C44	USB0_SSRX0-		J1.D44	USB0_SSTX0+	
J1.C45	USB0_SSRX0+		J1.D45	GND	
J1.C46	GND		J1.D46	USB0_SSTX1-	NA
J1.C47	USB0_SSRX1-	NA	J1.D47	USB0_SSTX1+	NA
J1.C48	USB0_SSRX1+	NA	J1.D48	GND	
J1.C49	GND		J1.D49	SATA0_RX-	
J1.C50	BOOT_SPI_IO0		J1.D50	SATA0_RX+	
J1.C51	BOOT_SPI_IO1		J1.D51	GND	
J1.C52	BOOT_SPI_IO2		J1.D52	SATA0_TX-	
J1.C53	BOOT_SPI_IO3		J1.D53	SATA0_TX+	
J1.C54	BOOT_SPI_CLK		J1.D54	GND	
J1.C55	GND		J1.D55	SATA1_RX-	
J1.C56	PCIe_REF-CLK0_HI-		J1.D56	SATA1_RX+	
J1.C57	PCIe_REF-CLK0_HI+		J1.D57	GND	
J1.C58	GND		J1.D58	SATA1_TX-	
J1.C59	PCIe_REF-CLK0_LO-		J1.D59	SATA1_TX+	
J1.C60	PCIe_REF-CLK0_LO+		J1.D60	GND	
J1.C61	GND		J1.D61	PCIe00_TX-	
J1.C62	PCIe00_RX-		J1.D62	PCIe00_TX+	
J1.C63	PCIe00_RX+		J1.D63	GND	
J1.C64	GND		J1.D64	PCIe01_TX-	
J1.C65	PCIe01_RX-		J1.D65	PCIe01_TX+	
J1.C66	PCIe01_RX+		J1.D66	GND	

Table A.2: J1 Connector Rows C and D				
J1.C67	GND		J1.D67	PCIe02_TX-
J1.C68	PCIe02_RX-		J1.D68	PCIe02_TX+
J1.C69	PCIe02_RX+		J1.D69	GND
J1.C70	GND		J1.D70	PCIe03_TX-
J1.C71	PCIe03_RX-		J1.D71	PCIe03_TX+
J1.C72	PCIe03_RX+		J1.D72	GND
J1.C73	GND		J1.D73	PCIe04_TX-
J1.C74	PCIe04_RX-		J1.D74	PCIe04_TX+
J1.C75	PCIe04_RX+		J1.D75	GND
J1.C76	GND		J1.D76	PCIe05_TX-
J1.C77	PCIe05_RX-		J1.D77	PCIe05_TX+
J1.C78	PCIe05_RX+		J1.D78	GND
J1.C79	GND		J1.D79	PCIe06_TX-
J1.C80	PCIe06_RX-		J1.D80	PCIe06_TX+
J1.C81	PCIe06_RX+		J1.D81	GND
J1.C82	GND		J1.D82	PCIe07_TX-
J1.C83	PCIe07_RX-		J1.D83	PCIe07_TX+
J1.C84	PCIe07_RX+		J1.D84	GND
J1.C85	GND		J1.D85	NBASET0_MDI0-
J1.C86	SMB_CLK		J1.D86	NBASET0_MDI0+
J1.C87	SMB_DAT		J1.D87	GND
J1.C88	SMB_ALERT#	NA	J1.D88	NBASET0_MDI1-
J1.C89	UART0_TX		J1.D89	NBASET0_MDI1+
J1.C90	UART0_RX		J1.D90	GND
J1.C91	UART0_RTS#		J1.D91	NBASET0_MDI2-
J1.C92	UART0_CTS#		J1.D92	NBASET0_MDI2+
J1.C93	I2C0_CLK		J1.D93	GND
J1.C94	I2C0_DAT		J1.D94	NBASET0_MDI3-
J1.C95	I2C0_ALERT#		J1.D95	NBASET0_MDI3+
J1.C96	I2C1_CLK		J1.D96	GND
J1.C97	I2C1_DAT		J1.D97	NBA-SET0_LINK_-MAX#
J1.C98	NBASET0_SDP		J1.D98	NBA-SET0_LINK_MID#
J1.C99	NBASET0_CTREF	NA	J1.D99	NBA-SET0_LINK_ACT#
J1.C100	TYPE1		J1.D100	TYPE2

Table A.3: J2 Connector Rows E and F

Pin#	Row E Description	SOM-E780 Difference	Pin#	Row F Description	SOM-E780 Difference
J2.E1	RAPID_SHUT-DOWN		J2.F1	ETH2_SDP	VCC
J2.E2	GND		J2.F2	ETH3_SDP	VCC
J2.E3	RSVD	VCC	J2.F3	ETH4_SDP	VCC
J2.E4	RSVD	VCC	J2.F4	ETH5_SDP	VCC
J2.E5	GND		J2.F5	ETH6_SDP	VCC
J2.E6	RSVD	VCC	J2.F6	ETH7_SDP	VCC
J2.E7	RSVD	VCC	J2.F7	ETH4-7_I2C_CLK	GND
J2.E8	GND		J2.F8	ETH4-7_I2C_DAT	GND
J2.E9	RSVD	GND	J2.F9	ETH4-7_INT#	GND
J2.E10	RSVD	GND	J2.F10	ETH4-7_MDIO_-CLK	GND
J2.E11	GND		J2.F11	ETH4-7_MDIO_-DAT	A_PCIe8_RX-
J2.E12	RSVD	A_PCIe8_TX-	J2.F12	ETH4-7_PHY_INT#	A_PCIe8_RX+
J2.E13	RSVD	A_PCIe8_TX+	J2.F13	ETH4-7_PHY_RST#	
J2.E14	GND		J2.F14	ETH4-7_PRSNT#	A_PCIe9_RX-
J2.E15	RSVD	A_PCIe9_TX-	J2.F15	RSVD	A_PCIe9_RX+
J2.E16	RSVD	A_PCIe9_TX+	J2.F16	RSVD	
J2.E17	GND		J2.F17	RSVD	A_PCIe10_RX-
J2.E18	RSVD	A_PCIe10_TX-	J2.F18	RSVD	A_P-CIe10_RX+
J2.E19	RSVD	A_PCIe10_TX+	J2.F19	GND	
J2.E20	GND		J2.F20	PCIe32_RX-	
J2.E21	PCIe32_TX-		J2.F21	PCIe32_RX+	
J2.E22	PCIe32_TX+		J2.F22	GND	
J2.E23	GND		J2.F23	PCIe33_RX-	
J2.E24	PCIe33_TX-		J2.F24	PCIe33_RX+	
J2.E25	PCIe33_TX+		J2.F25	GND	
J2.E26	GND		J2.F26	PCIe34_RX-	
J2.E27	PCIe34_TX-		J2.F27	PCIe34_RX+	
J2.E28	PCIe34_TX+		J2.F28	GND	
J2.E29	GND		J2.F29	PCIe35_RX-	
J2.E30	PCIe35_TX-		J2.F30	PCIe35_RX+	
J2.E31	PCIe35_TX+		J2.F31	GND	
J2.E32	GND		J2.F32	PCIe36_RX-	
J2.E33	PCIe36_TX-		J2.F33	PCIe36_RX+	
J2.E34	PCIe36_TX+		J2.F34	GND	
J2.E35	GND		J2.F35	PCIe37_RX-	
J2.E36	PCIe37_TX-		J2.F36	PCIe37_RX+	
J2.E37	PCIe37_TX+		J2.F37	GND	
J2.E38	GND		J2.F38	PCIe38_RX-	
J2.E39	PCIe38_TX-		J2.F39	PCIe38_RX+	

Table A.3: J2 Connector Rows E and F			
J2.E40	PCIe38_TX+	J2.F40	GND
J2.E41	GND	J2.F41	PCIe39_RX-
J2.E42	PCIe39_TX-	J2.F42	PCIe39_RX+
J2.E43	PCIe39_TX+	J2.F43	GND
J2.E44	GND	J2.F44	PCIe16_RX-
J2.E45	PCIe16_TX-	J2.F45	PCIe16_RX+
J2.E46	PCIe16_TX+	J2.F46	GND
J2.E47	GND	J2.F47	PCIe17_RX-
J2.E48	PCIe17_TX-	J2.F48	PCIe17_RX+
J2.E49	PCIe17_TX+	J2.F49	GND
J2.E50	GND	J2.F50	PCIe18_RX-
J2.E51	PCIe18_TX-	J2.F51	PCIe18_RX+
J2.E52	PCIe18_TX+	J2.F52	GND
J2.E53	GND	J2.F53	PCIe19_RX-
J2.E54	PCIe19_TX-	J2.F54	PCIe19_RX+
J2.E55	PCIe19_TX+	J2.F55	GND
J2.E56	GND	J2.F56	PCIe20_RX-
J2.E57	PCIe20_TX-	J2.F57	PCIe20_RX+
J2.E58	PCIe20_TX+	J2.F58	GND
J2.E59	GND	J2.F59	PCIe21_RX-
J2.E60	PCIe21_TX-	J2.F60	PCIe21_RX+
J2.E61	PCIe21_TX+	J2.F61	GND
J2.E62	GND	J2.F62	PCIe22_RX-
J2.E63	PCIe22_TX-	J2.F63	PCIe22_RX+
J2.E64	PCIe22_TX+	J2.F64	GND
J2.E65	GND	J2.F65	PCIe23_RX-
J2.E66	PCIe23_TX-	J2.F66	PCIe23_RX+
J2.E67	PCIe23_TX+	J2.F67	GND
J2.E68	GND	J2.F68	PCIe48_RX-
J2.E69	PCIe48_TX-	J2.F69	PCIe48_RX+
J2.E70	PCIe48_TX+	J2.F70	GND
J2.E71	GND	J2.F71	PCIe49_RX-
J2.E72	PCIe49_TX-	J2.F72	PCIe49_RX+
J2.E73	PCIe49_TX+	J2.F73	GND
J2.E74	GND	J2.F74	PCIe50_RX-
J2.E75	PCIe50_TX-	J2.F75	PCIe50_RX+
J2.E76	PCIe50_TX+	J2.F76	GND
J2.E77	GND	J2.F77	PCIe51_RX-
J2.E78	PCIe51_TX-	J2.F78	PCIe51_RX+
J2.E79	PCIe51_TX+	J2.F79	GND
J2.E80	GND	J2.F80	PCIe52_RX-
J2.E81	PCIe52_TX-	J2.F81	PCIe52_RX+
J2.E82	PCIe52_TX+	J2.F82	GND
J2.E83	GND	J2.F83	PCIe53_RX-
J2.E84	PCIe53_TX-	J2.F84	PCIe53_RX+
J2.E85	PCIe53_TX+	J2.F85	GND
J2.E86	GND	J2.F86	PCIe54_RX-

Table A.3: J2 Connector Rows E and F					
J2.E87	PCIe54_TX-		J2.F87	PCIe54_RX+	
J2.E88	PCIe54_TX+		J2.F88	GND	
J2.E89	GND		J2.F89	PCIe55_RX-	
J2.E90	PCIe55_TX-		J2.F90	PCIe55_RX+	
J2.E91	PCIe55_TX+		J2.F91	GND	
J2.E92	GND		J2.F92	PCIe_REFCLK2-	
J2.E93	PCIe_REFCLK1-		J2.F93	PCIe_REFCLK2+	
J2.E94	PCIe_REFCLK1+		J2.F94	GND	
J2.E95	GND		J2.F95	PCIe_CLKREQ3#	NA
J2.E96	PCIe_CLKREQ1#	NA	J2.F96	ETH0-3_PRSNT#	NA
J2.E97	PCIe_CLKREQ2#	NA	J2.F97	ETH0-3_PHY_RST#	NA
J2.E98	PCIe_-CLKREQ_OUT0#	NA	J2.F98	ETH0_SDP	NA
J2.E99	PCIe_-CLKREQ_OUT1#	NA	J2.F99	ETH1_SDP	NA
J2.E100	PCIe_PER-ST_IN0#		J2.F100	PCIe_PER-ST_IN1#	

Table A.4: J2 Connector Rows G and H					
Pin#	**Row G Description**	**SOM-E780 Difference**	**Pin#**	**Row H Description**	**SOM-E780 Difference**
J2.G1	RSVD	VCC_5V_SBY	J2.H1	RSVD	VCC
J2.G2	RSVD	VCC	J2.H2	RSVD	VCC
J2.G3	RSVD	VCC	J2.H3	RSVD	VCC
J2.G4	RSVD	VCC	J2.H4	RSVD	VCC
J2.G5	RSVD	VCC	J2.H5	RSVD	VCC
J2.G6	RSVD	VCC	J2.H6	RSVD	VCC
J2.G7	RSVD	VCC	J2.H7	RSVD	GND
J2.G8	RSVD	GND	J2.H8	RSVD	GND
J2.G9	RSVD	GND	J2.H9	RSVD	GND
J2.G10	RSVD	GND	J2.H10	RSVD	GND
J2.G11	RSVD	GND	J2.H11	RSVD	A_PCIe11_TX-
J2.G12	RSVD	A_PCIe11_RX-	J2.H12	RSVD	A_PCIe11_TX+
J2.G13	RSVD	A_PCIe11_RX+	J2.H13	RSVD	
J2.G14	GND		J2.H14	RSVD	A_PCIe12_TX-
J2.G15	RSVD	A_PCIe12_RX-	J2.H15	RSVD	A_P-CIe12_TX+
J2.G16	RSVD	A_PCIe12_RX+	J2.H16	RSVD	
J2.G17	RSVD		J2.H17	RSVD	A_PCIe13_TX-
J2.G18	RSVD	A_PCIe13_RX-	J2.H18	RSVD	A_P-CIe13_TX+
J2.G19	RSVD	A_PCIe13_RX+	J2.H19	GND	
J2.G20	GND		J2.H20	PCIe40_TX-	
J2.G21	PCIe40_RX-		J2.H21	PCIe40_TX+	
J2.G22	PCIe40_RX+		J2.H22	GND	
J2.G23	GND		J2.H23	PCIe41_TX-	

Table A.4: J2 Connector Rows G and H			
J2.G24	PCIe41_RX-	J2.H24	PCIe41_TX+
J2.G25	PCIe41_RX+	J2.H25	GND
J2.G26	GND	J2.H26	PCIe42_TX-
J2.G27	PCIe42_RX-	J2.H27	PCIe42_TX+
J2.G28	PCIe42_RX+	J2.H28	GND
J2.G29	GND	J2.H29	PCIe43_TX-
J2.G30	PCIe43_RX-	J2.H30	PCIe43_TX+
J2.G31	PCIe43_RX+	J2.H31	GND
J2.G32	GND	J2.H32	PCIe44_TX-
J2.G33	PCIe44_RX-	J2.H33	PCIe44_TX+
J2.G34	PCIe44_RX+	J2.H34	GND
J2.G35	GND	J2.H35	PCIe45_TX-
J2.G36	PCIe45_RX-	J2.H36	PCIe45_TX+
J2.G37	PCIe45_RX+	J2.H37	GND
J2.G38	GND	J2.H38	PCIe46_TX-
J2.G39	PCIe46_RX-	J2.H39	PCIe46_TX+
J2.G40	PCIe46_RX+	J2.H40	GND
J2.G41	GND	J2.H41	PCIe47_TX-
J2.G42	PCIe47_RX-	J2.H42	PCIe47_TX+
J2.G43	PCIe47_RX+	J2.H43	GND
J2.G44	GND	J2.H44	PCIe24_TX-
J2.G45	PCIe24_RX-	J2.H45	PCIe24_TX+
J2.G46	PCIe24_RX+	J2.H46	GND
J2.G47	GND	J2.H47	PCIe25_TX-
J2.G48	PCIe25_RX-	J2.H48	PCIe25_TX+
J2.G49	PCIe25_RX+	J2.H49	GND
J2.G50	GND	J2.H50	PCIe26_TX-
J2.G51	PCIe26_RX-	J2.H51	PCIe26_TX+
J2.G52	PCIe26_RX+	J2.H52	GND
J2.G53	GND	J2.H53	PCIe27_TX-
J2.G54	PCIe27_RX-	J2.H54	PCIe27_TX+
J2.G55	PCIe27_RX+	J2.H55	GND
J2.G56	GND	J2.H56	PCIe28_TX-
J2.G57	PCIe28_RX-	J2.H57	PCIe28_TX+
J2.G58	PCIe28_RX+	J2.H58	GND
J2.G59	GND	J2.H59	PCIe29_TX-
J2.G60	PCIe29_RX-	J2.H60	PCIe29_TX+
J2.G61	PCIe29_RX+	J2.H61	GND
J2.G62	GND	J2.H62	PCIe30_TX-
J2.G63	PCIe30_RX-	J2.H63	PCIe30_TX+
J2.G64	PCIe30_RX+	J2.H64	GND
J2.G65	GND	J2.H65	PCIe31_TX-
J2.G66	PCIe31_RX-	J2.H66	PCIe31_TX+
J2.G67	PCIe31_RX+	J2.H67	GND
J2.G68	GND	J2.H68	PCIe56_TX-
J2.G69	PCIe56_RX-	J2.H69	PCIe56_TX+
J2.G70	PCIe56_RX+	J2.H70	GND

Table A.4: J2 Connector Rows G and H					
J2.G71	GND		J2.H71	PCIe57_TX-	
J2.G72	PCIe57_RX-		J2.H72	PCIe57_TX+	
J2.G73	PCIe57_RX+		J2.H73	GND	
J2.G73	GND		J2.H74	PCIe58_TX-	
J2.G75	PCIe58_RX-		J2.H75	PCIe58_TX+	
J2.G76	PCIe58_RX+		J2.H76	GND	
J2.G77	GND		J2.H77	PCIe59_TX-	
J2.G78	PCIe59_RX-		J2.H78	PCIe59_TX+	
J2.G79	PCIe59_RX+		J2.H79	GND	
J2.G80	GND		J2.H80	PCIe60_TX-	
J2.G81	PCIe60_RX-		J2.H81	PCIe60_TX+	
J2.G82	PCIe60_RX+		J2.H82	GND	
J2.G83	GND		J2.H83	PCIe61_TX-	
J2.G84	PCIe61_RX-		J2.H84	PCIe61_TX+	
J2.G85	PCIe61_RX+		J2.H85	GND	
J2.G86	GND		J2.H86	PCIe62_TX-	
J2.G87	PCIe62_RX-		J2.H87	PCIe62_TX+	
J2.G88	PCIe62_RX+		J2.H88	GND	
J2.G89	GND		J2.H89	PCIe63_TX-	
J2.G90	PCIe63_RX-		J2.H90	PCIe63_TX+	
J2.G91	PCIe63_RX+		J2.H91	GND	
J2.G92	GND		J2.H92	PCIe_REF-CLKIN0-	NA
J2.G93	PCIe_REFCLK3-		J2.H93	PCIe_REF-CLKIN0+	NA
J2.G94	PCIe_REFCLK3+		J2.H94	GND	
J2.G95	GND		J2.H95	PCIe_REF-CLKIN1-	NA
J2.G96	ETH0-3_I2C_CLK	NA	J2.H96	PCIe_REF-CLKIN1+	NA
J2.G97	ETH0-3_I2C_DAT	NA	J2.H97	GND	
J2.G98	ETH0-3_PHY_INT#	NA	J2.H98	ETH0-3_MDIO_-CLK	NA
J2.G99	ETH0-3_INT#	NA	J2.H99	ETH0-3_MDIO_-DAT	NA
J2.G100	PCIe_WAKE_OUT0#	NA	J2.H100	PCIe_WAKE_OUT1#	NA

Appendix B

Watchdog Timer

This appendix gives you information about the watchdog timer programming on the SOM-E780 CPU System on Module.

Sections include:

- Programming the Watchdog Timer

B.1 Programming the Watchdog Timer

Table B.1: Programming the Watchdog Timer

Trigger Event	Note
IRQ	BIOS setting default disable**
NMI	N/A
SCI	Power button event
Power Off	Support
H/W Restart	Support
External WDT	Support

** WDT new driver support automatically selects an available IRQ number from the BIOS, and then sets it to EC. Only Win8.1 and Win10 support it.

In other OS, it will still use an IRQ number from the BIOS setting as usual. For details, please refer to the iManager & Software API User Manual.

Appendix C

Programming GPIO

This appendix details illustration of the General Purpose Input and Output pin settings.

Sections include:

- GPIO Register

C.1 GPIO Register

Table C.1: GPIO Register	
GPIO Byte Mapping	**H/W Pin Name**
BIT0	GPIO0
BIT1	GPIO1
BIT2	GPIO2
BIT3	GPIO3
BIT4	GPIO4
BIT5	GPIO5
BIT6	GPIO6
BIT7	GPIO7
BIT8	GPIO8
BIT9	GPIO9
BIT10	GPIO10
BIT11	GPIO11

For details, please refer to the iManager and Software API User Manual.

Appendix D

System Assignments

This appendix gives you the information about the system resource allocation on the SOM-E780 CPU System on Module.

Sections include:

- System I/O ports
- Interrupt Assignments
- 1st MB Memory Map

D.1 System I/O Ports

Table D.1: System I/O Ports

Addr.Range(Hex)	Device
0x00000299-0x0000029A	Motherboard resources
0x000002C0-0x000002DF	Motherboard resources
0x000002A0-0x000002BF	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x0000029E-0x000002AD	Motherboard resources
0x00000060-0x0000006F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x000002F0-0x000002F7	Motherboard resources
0x00000062-0x00000062	Microsoft ACPI-Compliant Embedded Controller
0x00000066-0x00000066	Microsoft ACPI-Compliant Embedded Controller
0x00000070-0x00000071	System CMOS/real time clock
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000020-0x00000021	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x00000000-0x000002FF	PCI Express Root Complex
0x00000000-0x000002FF	Direct memory access controller
0x00000300-0x000003AF	PCI Express Root Complex
0x000003E0-0x00000CF7	PCI Express Root Complex
0x000003B0-0x000003DF	PCI Express Root Complex
0x00001000-0x00003FFF	PCI Express Root Complex
0x00004000-0x00004FFF	PCI Express Root Complex
0x00005000-0x00006FFF	PCI Express Root Complex
0x00007000-0x0000FFFF	PCI Express Root Complex
0x0000F000-0x0000F07F	Microsoft Basic Display Adapter
0x0000F000-0x0000F07F	PCI Express Root Port
0x00000040-0x00000043	System timer
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x0000006F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000B1-0x000000B1	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x000004D0-0x000004D1	Motherboard resources

Table D.1: System I/O Ports	
0x0000040B-0x0000040B	Motherboard resources
0x000004D6-0x000004D6	Motherboard resources
0x00000C00-0x00000C01	Motherboard resources
0x00000C14-0x00000C14	Motherboard resources
0x00000C50-0x00000C51	Motherboard resources
0x00000C52-0x00000C52	Motherboard resources
0x00000C6C-0x00000C6C	Motherboard resources
0x00000C6F-0x00000C6F	Motherboard resources
0x00000CD0-0x00000CD1	Motherboard resources
0x00000CD2-0x00000CD3	Motherboard resources
0x00000CD4-0x00000CD5	Motherboard resources
0x00000CD6-0x00000CD7	Motherboard resources
0x00000CD8-0x00000CDF	Motherboard resources
0x00000800-0x0000089F	Motherboard resources
0x00000B00-0x00000B0F	Motherboard resources
0x00000B20-0x00000B3F	Motherboard resources
0x00000900-0x0000090F	Motherboard resources
0x00000910-0x0000091F	Motherboard resources
0x0000FE00-0x0000FEFE	Motherboard resources
0x00000061-0x00000061	System speaker
0x00000081-0x00000083	Direct memory access controller
0x00000087-0x00000087	Direct memory access controller
0x00000089-0x0000008B	Direct memory access controller
0x0000008F-0x0000008F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller

D.2 Interrupt Assignments

Table D.2: Interrupt Assignments

Interrupt#	Interrupt Source
IRQ 7	AMD GPIO Controller
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 4294967285	PCI Express Root Port
IRQ 4294967284	PCI Express Root Port
IRQ 4294967266	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967265	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967264	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967263	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967262	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967261	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967260	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967259	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967258	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967257	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967256	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967255	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967254	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967253	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967252	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967251	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967250	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967249	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967248	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967247	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967246	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967245	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967244	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967243	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967242	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967241	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967240	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967239	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967238	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967237	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967236	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967235	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967234	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967233	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967232	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967231	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967230	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967229	Intel® Ethernet Controller (3) I225-LM

Table D.2: Interrupt Assignments	
IRQ 4294967228	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967227	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967226	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967225	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967224	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967223	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967222	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967221	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967220	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967219	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967218	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967217	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967216	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967215	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967214	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967213	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967212	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967211	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967210	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967209	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967208	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967207	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967206	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967205	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967204	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967203	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967202	Intel® Ethernet Controller (3) I225-LM
IRQ 4294967274	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967273	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967272	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967271	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967270	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967269	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967268	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967267	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 6	Motherboard resources
IRQ 55	High Definition Audio Controller
IRQ 55	Microsoft ACPI-Compliant System
IRQ 54	Microsoft ACPI-Compliant System
IRQ 56	Microsoft ACPI-Compliant System
IRQ 57	Microsoft ACPI-Compliant System
IRQ 58	Microsoft ACPI-Compliant System
IRQ 59	Microsoft ACPI-Compliant System
IRQ 60	Microsoft ACPI-Compliant System
IRQ 61	Microsoft ACPI-Compliant System
IRQ 62	Microsoft ACPI-Compliant System
IRQ 63	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 64	Microsoft ACPI-Compliant System
IRQ 65	Microsoft ACPI-Compliant System
IRQ 66	Microsoft ACPI-Compliant System
IRQ 67	Microsoft ACPI-Compliant System
IRQ 68	Microsoft ACPI-Compliant System
IRQ 69	Microsoft ACPI-Compliant System
IRQ 70	Microsoft ACPI-Compliant System
IRQ 71	Microsoft ACPI-Compliant System
IRQ 72	Microsoft ACPI-Compliant System
IRQ 73	Microsoft ACPI-Compliant System
IRQ 74	Microsoft ACPI-Compliant System
IRQ 75	Microsoft ACPI-Compliant System
IRQ 76	Microsoft ACPI-Compliant System
IRQ 77	Microsoft ACPI-Compliant System
IRQ 78	Microsoft ACPI-Compliant System
IRQ 79	Microsoft ACPI-Compliant System
IRQ 80	Microsoft ACPI-Compliant System
IRQ 81	Microsoft ACPI-Compliant System
IRQ 82	Microsoft ACPI-Compliant System
IRQ 83	Microsoft ACPI-Compliant System
IRQ 84	Microsoft ACPI-Compliant System
IRQ 85	Microsoft ACPI-Compliant System
IRQ 86	Microsoft ACPI-Compliant System
IRQ 87	Microsoft ACPI-Compliant System
IRQ 88	Microsoft ACPI-Compliant System
IRQ 89	Microsoft ACPI-Compliant System
IRQ 90	Microsoft ACPI-Compliant System
IRQ 91	Microsoft ACPI-Compliant System
IRQ 92	Microsoft ACPI-Compliant System
IRQ 93	Microsoft ACPI-Compliant System
IRQ 94	Microsoft ACPI-Compliant System
IRQ 95	Microsoft ACPI-Compliant System
IRQ 96	Microsoft ACPI-Compliant System
IRQ 97	Microsoft ACPI-Compliant System
IRQ 98	Microsoft ACPI-Compliant System
IRQ 99	Microsoft ACPI-Compliant System
IRQ 100	Microsoft ACPI-Compliant System
IRQ 101	Microsoft ACPI-Compliant System
IRQ 102	Microsoft ACPI-Compliant System
IRQ 103	Microsoft ACPI-Compliant System
IRQ 104	Microsoft ACPI-Compliant System
IRQ 105	Microsoft ACPI-Compliant System
IRQ 106	Microsoft ACPI-Compliant System
IRQ 107	Microsoft ACPI-Compliant System
IRQ 108	Microsoft ACPI-Compliant System
IRQ 109	Microsoft ACPI-Compliant System
IRQ 110	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 111	Microsoft ACPI-Compliant System
IRQ 112	Microsoft ACPI-Compliant System
IRQ 113	Microsoft ACPI-Compliant System
IRQ 114	Microsoft ACPI-Compliant System
IRQ 115	Microsoft ACPI-Compliant System
IRQ 116	Microsoft ACPI-Compliant System
IRQ 117	Microsoft ACPI-Compliant System
IRQ 118	Microsoft ACPI-Compliant System
IRQ 119	Microsoft ACPI-Compliant System
IRQ 120	Microsoft ACPI-Compliant System
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IRQ 140	Microsoft ACPI-Compliant System
IRQ 141	Microsoft ACPI-Compliant System
IRQ 142	Microsoft ACPI-Compliant System
IRQ 143	Microsoft ACPI-Compliant System
IRQ 144	Microsoft ACPI-Compliant System
IRQ 145	Microsoft ACPI-Compliant System
IRQ 146	Microsoft ACPI-Compliant System
IRQ 147	Microsoft ACPI-Compliant System
IRQ 148	Microsoft ACPI-Compliant System
IRQ 149	Microsoft ACPI-Compliant System
IRQ 150	Microsoft ACPI-Compliant System
IRQ 150	Trusted Platform Module 2.0
IRQ 151	Microsoft ACPI-Compliant System
IRQ 152	Microsoft ACPI-Compliant System
IRQ 153	Microsoft ACPI-Compliant System
IRQ 154	Microsoft ACPI-Compliant System
IRQ 155	Microsoft ACPI-Compliant System
IRQ 156	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 157	Microsoft ACPI-Compliant System
IRQ 158	Microsoft ACPI-Compliant System
IRQ 159	Microsoft ACPI-Compliant System
IRQ 160	Microsoft ACPI-Compliant System
IRQ 161	Microsoft ACPI-Compliant System
IRQ 162	Microsoft ACPI-Compliant System
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IRQ 199	Microsoft ACPI-Compliant System
IRQ 200	Microsoft ACPI-Compliant System
IRQ 201	Microsoft ACPI-Compliant System
IRQ 202	Microsoft ACPI-Compliant System
IRQ 203	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 204	Microsoft ACPI-Compliant System
IRQ 256	Microsoft ACPI-Compliant System
IRQ 257	Microsoft ACPI-Compliant System
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IRQ 301	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 302	Microsoft ACPI-Compliant System
IRQ 303	Microsoft ACPI-Compliant System
IRQ 304	Microsoft ACPI-Compliant System
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Table D.2: Interrupt Assignments	
IRQ 349	Microsoft ACPI-Compliant System
IRQ 350	Microsoft ACPI-Compliant System
IRQ 351	Microsoft ACPI-Compliant System
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Table D.2: Interrupt Assignments	
IRQ 396	Microsoft ACPI-Compliant System
IRQ 397	Microsoft ACPI-Compliant System
IRQ 398	Microsoft ACPI-Compliant System
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IRQ 400	Microsoft ACPI-Compliant System
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Table D.2: Interrupt Assignments	
IRQ 443	Microsoft ACPI-Compliant System
IRQ 444	Microsoft ACPI-Compliant System
IRQ 445	Microsoft ACPI-Compliant System
IRQ 446	Microsoft ACPI-Compliant System
IRQ 447	Microsoft ACPI-Compliant System
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IRQ 476	Microsoft ACPI-Compliant System
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IRQ 480	Microsoft ACPI-Compliant System
IRQ 481	Microsoft ACPI-Compliant System
IRQ 482	Microsoft ACPI-Compliant System
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IRQ 487	Microsoft ACPI-Compliant System
IRQ 488	Microsoft ACPI-Compliant System
IRQ 489	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 490	Microsoft ACPI-Compliant System
IRQ 491	Microsoft ACPI-Compliant System
IRQ 492	Microsoft ACPI-Compliant System
IRQ 493	Microsoft ACPI-Compliant System
IRQ 494	Microsoft ACPI-Compliant System
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IRQ 497	Microsoft ACPI-Compliant System
IRQ 498	Microsoft ACPI-Compliant System
IRQ 499	Microsoft ACPI-Compliant System
IRQ 500	Microsoft ACPI-Compliant System
IRQ 501	Microsoft ACPI-Compliant System
IRQ 502	Microsoft ACPI-Compliant System
IRQ 503	Microsoft ACPI-Compliant System
IRQ 504	Microsoft ACPI-Compliant System
IRQ 505	Microsoft ACPI-Compliant System
IRQ 506	Microsoft ACPI-Compliant System
IRQ 507	Microsoft ACPI-Compliant System
IRQ 508	Microsoft ACPI-Compliant System
IRQ 509	Microsoft ACPI-Compliant System
IRQ 510	Microsoft ACPI-Compliant System
IRQ 511	Microsoft ACPI-Compliant System
IRQ 4294967292	PCI Express Root Port
IRQ 4294967291	PCI Express Root Port
IRQ 4294967294	PCI Express Root Port
IRQ 4294967293	PCI Express Root Port
IRQ 0	System timer
IRQ 4294967283	Standard SATA AHCI Controller
IRQ 4294967290	PCI Express Root Port
IRQ 4294967289	PCI Express Root Port
IRQ 10	
IRQ 4294967288	PCI Express Root Port
IRQ 4294967287	PCI Express Root Port
IRQ 4294967286	PCI Express Root Port
IRQ 4294967282	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967281	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967280	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967279	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967278	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967277	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967276	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967275	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)

D.3 1st MB Memory Map

Table D.3: 1st MB Memory Map

Addr. Range (Hex)	Device
0xFED81500-0xFED818FF	AMD GPIO Controller
0xF8900000-0xF89FFFFF	PCI Express Root Port
0xF8700000-0xF88FFFFF	PCI Express Root Port
0xF8700000-0xF88FFFFF	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
0xC2300000-0xC23FFFFF	Intel® Ethernet Controller (3) I225-LM
0xC2400000-0xC2403FFF	Intel® Ethernet Controller (3) I225-LM
0xF2000000-0xF20FFFFF	AMD USB 3.10 eXtensible Host Controller - 1.10 (Microsoft)
0xF2000000-0xF20FFFFF	PCI Express Root Port
0xE0000000-0xEFFFFFFF	System board
0xC2080000-0xC2083FFF	High Definition Audio Controller
0xA0000-0xBFFFF	PCI Express Root Complex
0xC0000-0xDFFFF	PCI Express Root Complex
0xF6700000-0xF89FFFFF	PCI Express Root Complex
0xF0000000-0xF24FFFFF	PCI Express Root Complex
0xF4500000-0xF66FFFFF	PCI Express Root Complex
0xB0000000-0xC35FFFFF	PCI Express Root Complex
0xB0000000-0xC35FFFFF	Microsoft Basic Display Adapter
0xB0000000-0xC35FFFFF	PCI Express Root Port
0xC2600000-0xC26FFFFF	PCI Express Root Port
0xC2500000-0xC25FFFFF	PCI Express Root Port
0xC1000000-0xC1FFFFFF	Microsoft Basic Display Adapter
0xC1000000-0xC1FFFFFF	PCI Express Root Port
0xB8000000-0xB9FFFFFF	Microsoft Basic Display Adapter
0xFED40000-0xFED44FFF	Trusted Platform Module 2.0
0xC2200000-0xC24FFFFF	PCI Express Root Port
0xF2300000-0xF23007FF	Standard SATA AHCI Controller
0xF2300000-0xF23007FF	PCI Express Root Port
0xF6600000-0xF66FFFFF	PCI Express Root Port
0xF6500000-0xF65FFFFF	PCI Express Root Port
0xFEDC2000-0xFEDC2FFF	
0xF2400000-0xF24FFFFF	PCI Express Root Port
0xFEDC0000-0xFEDC0FFF	Motherboard resources
0xFEE00000-0xFEE00FFF	Motherboard resources
0xFED80000-0xFED814FF	Motherboard resources
0xFED81900-0xFED8FFFF	Motherboard resources
0xFEC10000-0xFEC10FFF	Motherboard resources
0xFF000000-0xFFFFFFFF	Motherboard resources

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