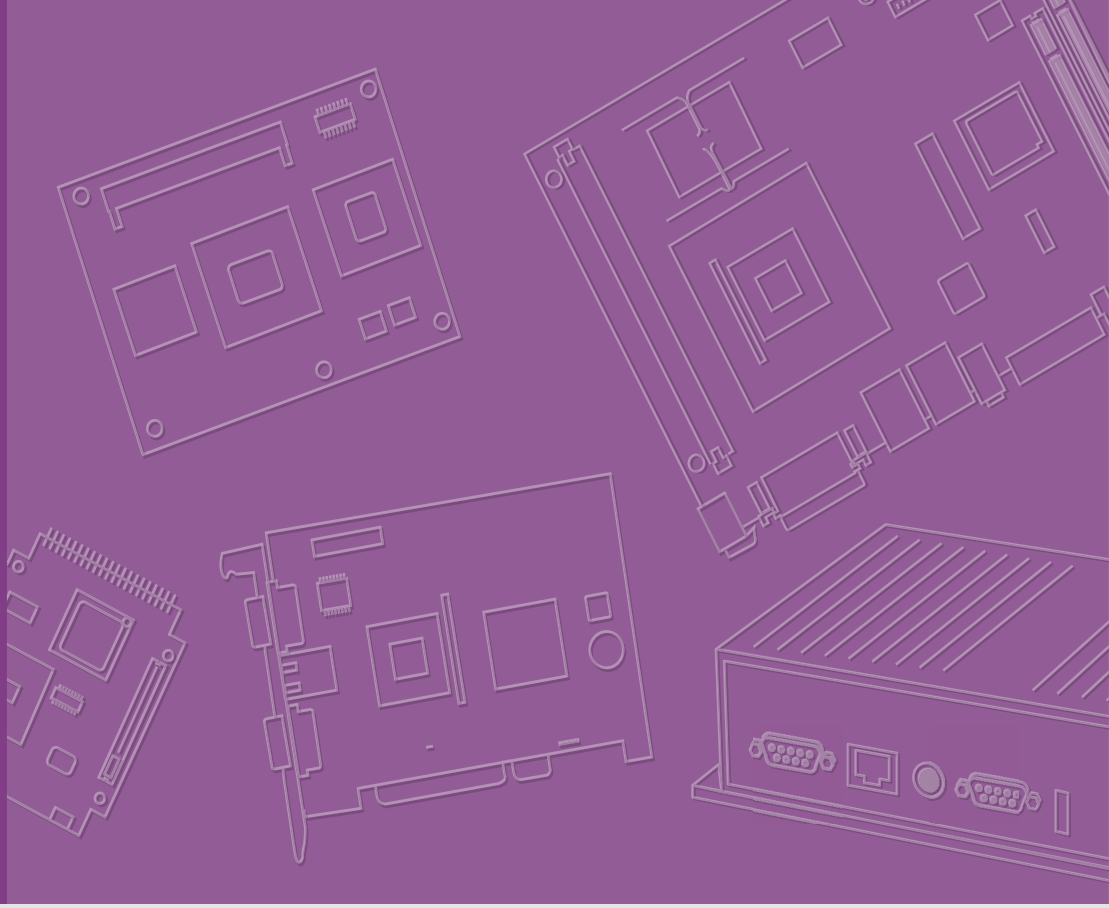

User Manual

SOM-A350

Intel® Core™ Ultra Processors (Meteor Lake U/H) COM-HPC Client Size A Module

ADVANTECH

Enabling an Intelligent Planet

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Acknowledgments

Product Warranty (2 Years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Part No. 2006A35000 Edition 1

Printed in China October 2024

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Test conditions for passing also include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

FM

This equipment has passed FM certification. According to the National Fire Protection Association, work sites are categorized into different classes, divisions, and groups based on hazard considerations. This equipment is compliant with the specifications for Class I, Division 2, Groups A, B, C, and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions and Notes

Warning! *Warnings indicate conditions that if not observed can cause personal injury!*

Caution! *Cautions are included to help prevent hardware damage and data losses. For example,*

"Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions."

Note! *Notes provide additional, optional information.*

Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all feedback in writing to support@advantech.com.

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

Part No.	Description	Quantity
-	SOM-A350 COM module	1
1970005956T001	Heatspreader of SOM-A350	1

Selection Guide with P/N

Part No.	CPU	Cores (P+E)	Default TDP	cTDP	Base Freq. (P/E Cores)	Max. Turbo Freq. (P/E Cores)	Graphics Execution Units	Operating Temp.
SOM-A350C7H-S4A1	Core Ultra 7 155H	16C (6P+8E +2LPE)	45W	20W-45W	1.4GHz/ 0.9GHz	4.8GHz/ 3.8GHz	128EU	0~60 °C
SOM-A350C5H-S2A1	Core Ultra 5 125H	14C (4P+8E +2LPE)	45W	20W-45W	1.2GHz/ 0.7GHz	4.5GHz/ 3.6GHz	112EU	0~60 °C
SOM-A350C7U-S7A1	Core Ultra 7 155U	12C (2P+8E +2LPE)	28W	12W-28W	1.7GHz/ 1.2GHz	4.8GHz/ 3.8GHz	64EU	0~60 °C
SOM-A350C5U-S3A1	Core Ultra 5 125U	12C (2P+8E +2LPE)	28W	12W-28W	1.3GHz / 0.8GHz	4.3GHz/ 3.6GHz	64EU	0~60 °C

Development Board

Part No.	Description
SOM-DH3000-00A2	COM-HPC Development Board for Client Pinout with 10mm High Board to Board Connector (Meteor Lake-U/H)

Optional Accessory

Part No.	Description
1970005961T001	QFCS 120x95x26.55mm

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.

Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped and damaged.
    - The equipment shows obvious signs of breakage.
15. Do not leave the equipment in an environment with a storage temperature of below 40 °C (-40 °F) or above 85°C (185 °F), as this may damage the components. The equipment should be kept in a controlled environment.
16. CAUTION: Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
17. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator’s position does not exceed 70 dB (A).

DISCLAIMER: These instructions are provided according to IEC 704-1 standards. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Acronyms

Term	Definition/Meaning
AC'97	Audio CODEC (Coder-Decoder)
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PC-AT systems
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system
CAN	Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow microcontrollers to communicate with each other within a vehicle without a host computer
DDI	Digital Display Interface – containing DisplayPort, HDMI/DVI, and SDVO
EAPI	Embedded Application Programmable Interface Software interface for COM Express® specific industrial function ■ System information ■ Watchdog timer ■ I2C Bus ■ Flat-panel brightness control ■ User storage area ■ GPIO
GbE	Gigabit Ethernet
GPIO	General purpose input output
HDA	Intel High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio that is capable of playing back more channels at higher quality than AC'97
I2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuit, primarily used to read and load register values
ME	Management Engine
PC-AT	"Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel based personal computer in 1990s
PEG	PCI Express Graphics
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information
TPM	Trusted Platform Module, chip to enhance the security features of a computer system
UEFI	Unified Extensible Firmware Interface
WDT	Watchdog Timer

Contents

Chapter 1

General Information

This chapter details background information on the SOM-A350 CPU Computer on Module.

Sections include:

- Introduction
- Functional Block Diagram
- Product Specifications

1.1 Introduction

The Advantech SOM-A350 is a cutting-edge COM-HPC Client Module that incorporates 14th Gen Intel® Core™ processors (Meteor Lake U/H), delivering robust 8-core computing performance while operating within a 45Watt TDP envelope. This module is purpose-built for testing equipment and high-end medical applications, offering exceptional capabilities.

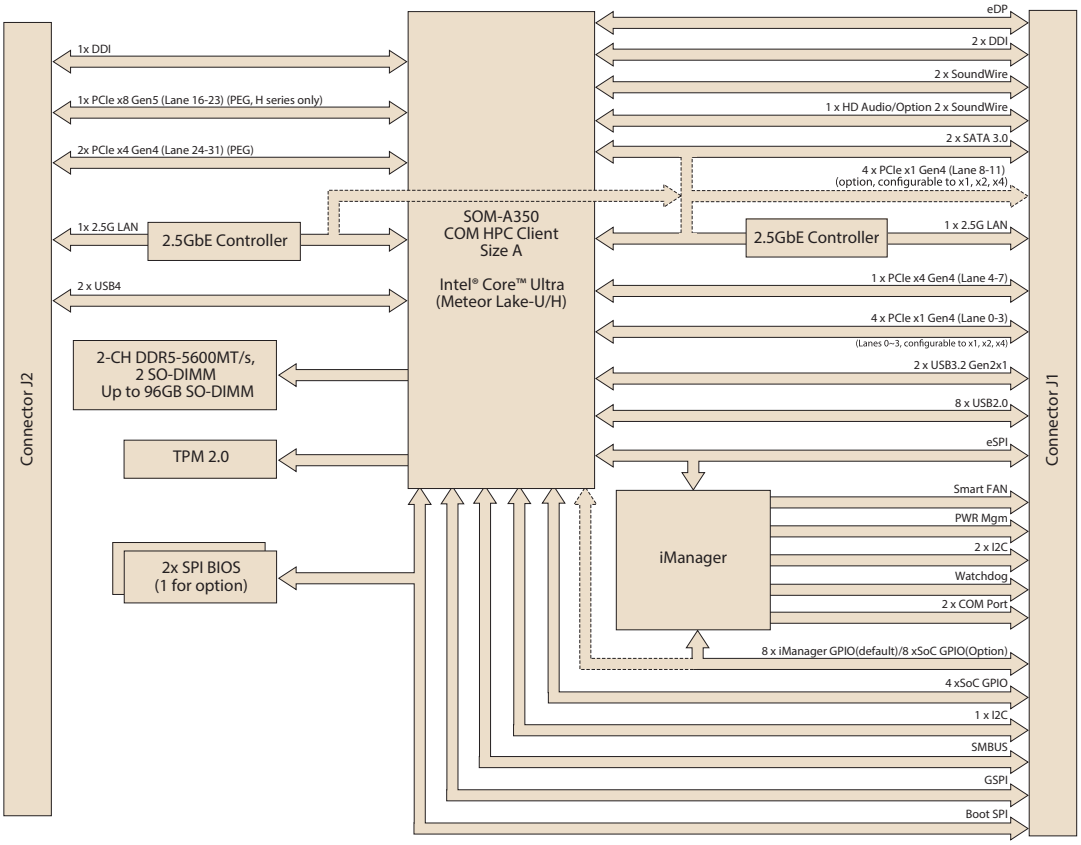
SOM-A350 is equipped with Intel Iris Xe graphics and comes pre-loaded with Advantech's comprehensive EdgeAI Suite software toolkit, ensuring seamless integration into AI-driven applications. It is thoughtfully designed to support up to 96GB of DDR5 memory operating at 5600MHz, and it features a wide range of high-speed I/O interfaces, including PCIe Gen 5 (16GT/s), 2.5Gbase-T, and USB 3.2 Gen2

(10Gbps).What sets the SOM-A350 apart is its ability to drive three independent 8K displays via DisplayPort 1.4/HDMI 2.1, in addition to offering an eDP interface and three DDI interfaces. Furthermore, it can be configured to handle two 8K HDR outputs simultaneously, making it a standout solution for graphics-intensive applications.

With an onboard TPM2.0 for enhanced security, a 12V power input, and the ability to operate within a wide temperature range of 0 to 60°C (by the inclusion of a heat spreader and QFCS), the SOM-A350 is both reliable and versatile.

To cater to a variety of requirements, Advantech has integrated its iManager (SUSI 4) software, which offers support for multi-level watchdog timers, voltage and temperature monitoring, thermal protection and mitigation, LCD backlight control, and embedded storage management. It's worth noting that all Advantech COM-HPC modules come with iManager and WISE-PaaS/RMM for comprehensive functionality and management capabilities.

1.2 Functional Block Diagram



1.3 Product Specification

1.3.1 Compliance

- PICMG CO-HPC Revision 1.2
- Size - 95 x 120 mm (3.74 x 4.72 in)
- Pin-out Type Client Type compatible

1.3.2 Feature List

Table 1.1: Feature List

Feature Type	Connector	Feature	COM HPC Define		SOM-A350
			Max.	Min.	
Video	J1	eDP	1	0	1
	J1	DDI0	1	1	1
	J1	DDI1	1	0	1
	J2	DDI2	1	0	1
PCIe	J1	PCI Express x1	16	4	12
	J2	PCI Express x1	32	0	16
Other Serial	J1	SMBus	1	1	1
	J1	I2C Bus	2	2	2
	J1	IPMB	1	0	0
	J1	UART	2	0	2
Ethernet	J1-J2	NBASE-T (max. 10G)	2	1	2
	J2	ETH KR (max 25G)	2	0	0
	J2	ETH KR CEI	1	0	0
USB	J1	USB 2.0	8	4	8
	J1	USB 3.2 Gen 2x1	2	0	2
	J1	USB 3.2 Gen 2x2	4	0	0
	J1-J2	USB4	4	0	2
Audio	J1	Soundwire / DMIC	2	0	2
	J1	I2S / 2xSNDW	1	0	1
	J1	HD Audio	1	0	1
Storage	J1	SATA	2	0	2
SPI	J1	eSPI	1	0	1
	J1	BOOT_SPI	1	1	1
	J1	GP_SPI	1	1	1
Misc	J1	GPIO	12	12	12
	J1	MISC	1	0	0
Others	J1	Watchdog Timer	1	0	1
	J1	Secondary Fan PWM	1	1	1
	J1	Thermal Protection	1	1	1
Power	J1	VCC pins	28	28	28
	J1-J2	Standby Power	2	0	2
	J1-J2	GND	207	207	207
	J1-J2	RSVD	30	0	30

1.3.3 Processor System

Table 1.2: Processor System					
CPU	**Cores (P+E)**	**Base Freq. (P/E Cores)**	**Max. Turbo Freq. (P/ECores)**	**Cache (MB)**	**cTDP(W)**
Core Ultra 7-155H	16C(6P+8E +2LPE)	1.4GHz/ 0.9GHz	4.8GHz/ 3.8GHz	24	20W-45W
Core Ultra 5-125H	14C(4P+8E +2LPE)	1.2GHz/ 0.7GHz	4.5GHz/ 3.6GHz	18	20W-45W
Core Ultra 7-155U	12C(2P+8E +2LPE)	1.7GHz/ 1.2GHz	4.8GHz/ 3.8GHz	12	12-28W
Core Ultra 5-125U	12C(2P+8E +2LPE)	1.3GHz / 0.8GHz	4.3GHz/ 3.6GHz	12	12-28W

1.3.4 Memory

There are a total of 2 memory sockets on SOM-A350. 1 pc on the front side and 1pc on the rear side by default. This solution supports max. 96GB capacity (non ECC memory modules with all SKUs.) with 262-pin DDR5 SO-DIMM sockets (dual-channel).

1.3.5 Graphics/Audio

Graphics Core: Intel® Xe LPG supports DX12.2, OGL4.6, OCL3.0, and MPEG2/ AVC/HEVC/VP9/JPEG/AV1 HW decode/encode/transcode acceleration.

Table 1.3: Graphics/Audio			
CPU	**Graphic Core**	**Base Freq.**	**Max Freq.**
Core Ultra 7-155H	Intel® Xe LPG	1.4GHz	2.25GHz
Core Ultra 5-125H	Intel® Xe LPG	1.2GHz	2.2GHz
Core Ultra 7-155U	Intel® Xe LPG	1.7GHz	1.95GHz
Core Ultra 5-125U	Intel® Xe LPG	1.3GHz	1.85GHz

- Dual display:
  - eDP+DDI1
  - DDI1+DDI2
- Triple display:
  - eDP+DDI1+DDI2
  - DDI1+DDI2+DDI3
- Quad display:
  - eDP+DDI1+DDI2+DDI3

1.3.6 Expansion Interfaces

- **PCI Express Graphics (PEG)**
  PEG: supports 8 lanes compliant with PCIe Gen 5 (32.0 GT/s) configurable to PEG x8 (H series only) and 8 lanes compliant to PCIe Gen 4 (16.0 GT/s) specifications configurable to 2 PEG x4.

Table 1.4: PCI Express Graphics (PEG)																
Client Type	Primary J2															
PCIe Lane	P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31
Default	x8 (H series only)								x4				x4			

- **PCI Express**
  PCI Express: By default, supports 8 PCIe lanes with additional 4 lanes available, compliant with PCIe Gen 4 (16.0 GT/s) specifications. These lanes can be bifurcate into PCIe x4, x2, and x1 configurations. For more information, please reach out to Advantech sales or FAE.

Table 1.5: PCI Express

Client Type	Primary J1											
PCIe Lane	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11
Default	x4				x4				N/A	N/A	N/A	N/A
Option	x4				x4				x4			

1.3.7 Serial Bus

- **SMBus**
  Supports SMBus 2.0 specifications.
- **I²C Bus**
  Supports I²C bus 7-bit and 10-bit address modes. Support standard mode up to 100 Kb/s, fast mode up to 400 Kb/s.

1.3.8 I/O

- **Gigabit Ethernet**
  Ethernet: Intel® I226 Gigabit LAN supports 10/100/1000 Mbps & 2.5 Gbps Speed.
- **SATA**
  Supports 2x ports SATA Gen3 (6.0 Gb/s), backward compliant to SATA Gen2 (3.0 Gb/s) and Gen1 (1.5 Gb/s). The maximum data rate is 600 MB/s. Supports AHCI 1.3.1 mode (does not support IDE mode).
- **USB 3.2/USB 2.0**
  Supports 2x USB 3.2 Gen2x1 (10 Gbps) ports and 8x USB 2.0 (480 Mbps) ports which are reverse compatible to USB1.x. For USB 3.2, product supports LPM (U0, U1, U2, and U3) for power efficiency.
  Notice: To meet USB 3.2 Gen2x1 performance, Advantech strongly recommends using a certificated cable.
- **USB 2.0**

Table 1.6: USB 2.0

Client Type	P0	P1	P2	P3	P4	P5	P6	P7
SoC	P0	P1	P2	P3	P4	P5	P6	P7
J1	OC_01		OC_23		OC_45		OC_67	
SoC USB_OC#	OC_0		OC_1		OC_1		OC_3	

- **SPI Bus**
  Supports BIOS flash only. SPI clock can be 14MHz, with capacity up to 256Mb.
- **GPIO**
  12 programmable general purpose input/output (GPIO).
- **Watchdog Timer**
  Supports multi-level watchdog time-out output. Provides 1-65535 level, from a 100ms to 109.22 minute intervals.
- **Serial Port**
  2 x 2-wire serial port (Tx/Rx) supports 16550 UART compliance.
  - Programmable FIFO or character mode
  - 16-byte FIFO buffer on transmitter and receiver in FIFO mode
  - Programmable serial-interface characteristics: 5, 6, 7, or 8-bit character

- Even, odd, or no parity bit selectable
- 1, 1.5, or 2 stop bit selectable
- Baud rate up to 115.2K

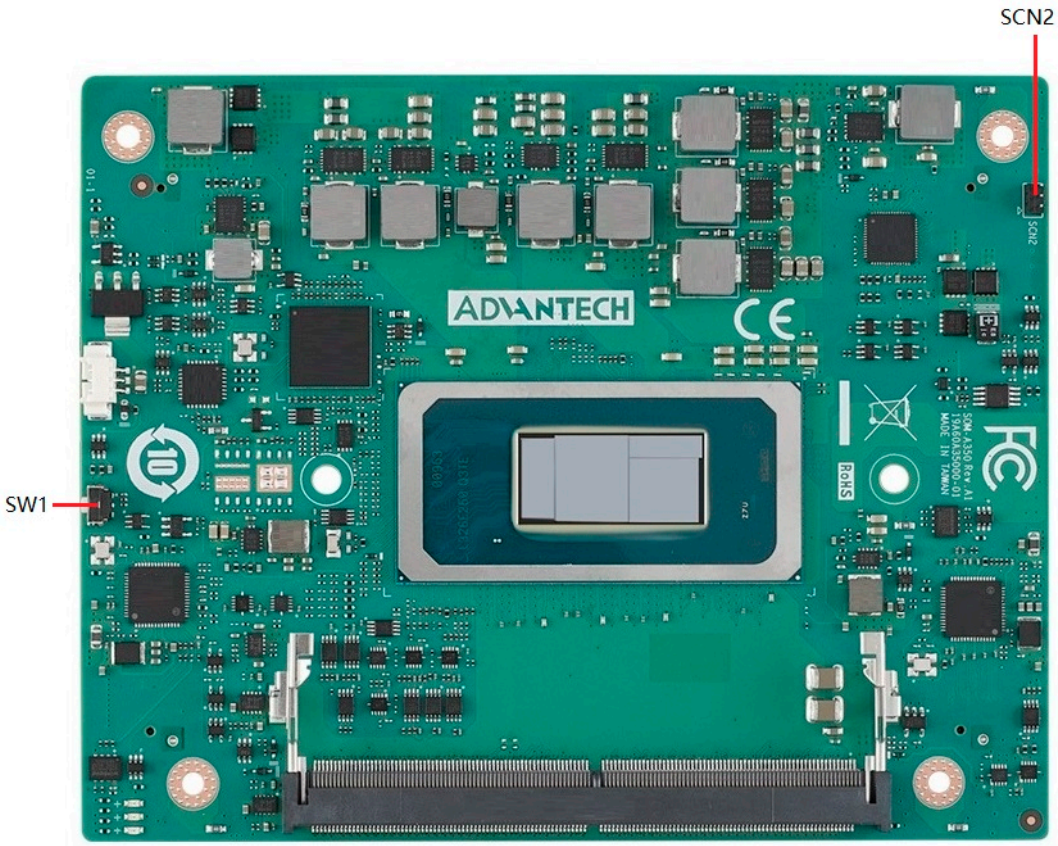
- **TPM**
  Supports TPM 2.0 module by default.
- **Smart Fan**
  Supports 1x Fan PWM control signals and 1x tachometer input for fan speed detection. Provides 1 on module with connector and the other to the carrier board following PICMG COM-HPC Carrier Design Guide R1.2 specifications.
- **BIOS**
  The BIOS chip is on module by default. Users can place BIOS chip on the carrier board with appropriate design and jumper setting in BSEL#[2:0].

Table 1.7: BIOS

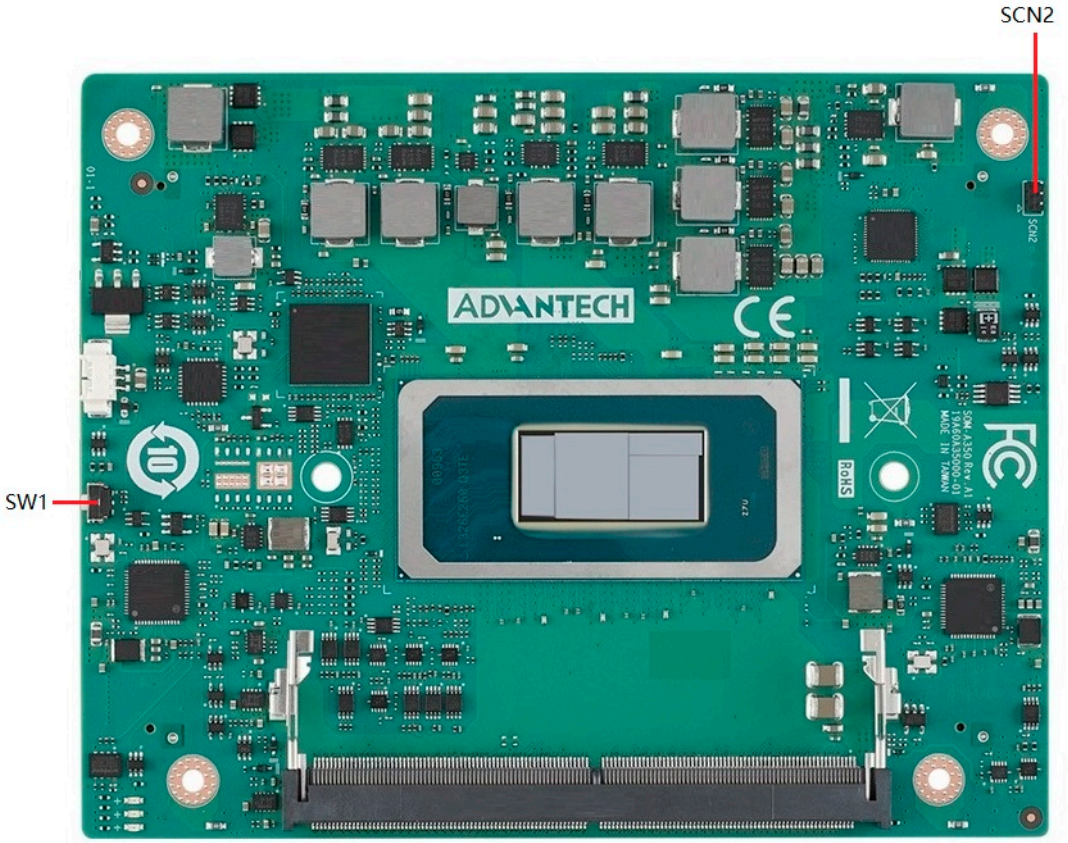
BSEL #2	BSEL #1	BSEL S#0	Boot up destination/function
NA	NA	Open	Boot from Module's SPI BIOS
NA	NA	GND	Boot from Carrier SPI BIOS

Note: If system COMS is cleared, Advantech strongly suggests going to the BIOS setup menu and loading default settings on the first boot up.

The standard module has no jumper at SCN2, so BIOS settings are kept without an RTC coin battery. If requiring to restore the BIOS to default settings, follow the steps below:



1. Remove the coin battery.
2. Push button on SW1.
3. Turn on power supply.
4. The system will boot up a few times.
5. The BIOS will load default settings successfully.



1. Remove the coin battery.
2. Push button on SW1.
3. Turn on power supply.
4. The system will boot up a few times.
5. The BIOS will load default settings successfully.

1.3.9 Power Management

- **Power Supply**
  Supports both ATX and AT power modes. VSB is for suspended power and is optional if not required by standby (suspend-to-RAM) support. The RTC battery is optional if date/timekeeping is not required.
  - Vin: 8V~20V
  - VSB: 5V +/- 5% (Suspend power)
  - RTC Battery Power: 2.0V – 3.3V
- **PWROK**
  Power-good from the main power supply. A high value indicates the power level is good. This signal can be used to postpone module startup to allow carrier-based FPGAs or other configurable devices time to be programmed.
- **Power Sequence**
  Referring to PICMG COM Express COM-HPC R1.2 specifications.
- **Wake Event**
  Various wake event support allows users to apply different scenarios.
  - Wake-on-LAN(WOL): Wake to S0 from S4/S5
  - USB Wake: Wake to S0 from S4
  - PCIe Device Wake: depends on user inquiry and may need customized BIOS

- **Advantech S5 ECO Mode (Deep Sleep Mode)**
  Advantech iManager provides additional features allowing the system to enter a very low suspended power mode – S5 ECO mode. In this mode, the module will cut all power, including suspended and active power to the chipset, and keep an on-module controller active. Only power under 50MW will be consumed, meaning user battery packs can last longer. While this mode is enabled in the BIOS, the system (or mod- ule) only allows power button boot instead of other methods such as WOL.

1.3.10 Environment

- **Temperature**
  - Operating: 0 ~ 60 °C (32 ~ 140 °F)
  - Storage: -40 ~ 85 °C (-40 ~ 185 °F)
- **Humidity**
  - Operating: 40 °C @ 95% relative humidity, non-condensing
  - Storage: 60 °C @ 95% relative humidity, non-condensing
- **Vibrations**
  IEC60068-2-64: Random vibration test under operation mode, 3.5 Grms.
- **Drop Test (Shock)**
  Federal Standard 101 Method 5007 test procedure with standard packing.
- **EMC**
  CE EN55022 Class B and FCC Certifications: validated with standard development boards in Advantech chassis.

1.3.11 MTBF

Please refer Advantech SOM-A350 Refresh Series Reliability Prediction report on the website: Link: http://com.advantech.com

1.3.12 OS Support

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft Windows Embedded technology." We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows Embedded software solutions easily and widely available to the embedded computing community.

To install drivers, please connect to the website http://support.advantech.com.tw to download the setup file.

1.3.13 Advantech iManager

Supports APIs for GPIO, smart fan control, multi-stage watchdog timer, temperature sensor, and hardware monitoring. Follows PICMG EAPI 1.0 specifications with backward compatibility.

1.3.14 Power Consumption

Table 1.9: Power Consumption Table (Watt.)

VCC=12V, VSB=5V	Active Power Domain			Suspend Power Domain		Mechanical off
Power State	S0 Max. Load	S0 Burn-in	S0 Idle	S5	S5 Deep Sleep	RTC (uA)
SOM-A350C7H-S4A1	82.47W	70.74W	5.34W	0.80W	0.31W	4.31μA

- **Hardware Configurations:**
  1. MB: SOM-A350C7H-S4A1
  2. DRAM: 48GB DDR5 5600MHz x 2pcs.
  3. Carrier board: SOM-DH3000-00A2
- **Test Condition:**
  1. Test temperature: room temperature (about 25 °C)
  2. Test voltage: rated voltage DC +12V
  3. Test loading:
     - Maximum load mode: According to Intel thermal/power test tools.
     - Burn-in mode: Burn-in test V8.1 Pro (1023) for 64 bit Windows. (CPU, RAM, 2D&3D Graphics and Disk with 100%)
     - Idle mode: DUT power management off and not running any program.

1.3.15 Performance

To compare performance or benchmark data with other modules, please refer to “Advantech COM Performance & Power Consumption Table.”

1.3.16 Pin Description

Advantech provides useful checklists for schematic design and layout routing. The schematic checklist will specify details about each pin’s electrical properties and how to connect it in different scenarios. The layout checklist will specify the layout constraints and recommendations for trace length, impedance, and other necessary information during design.

Please contact your regional Advantech branch office to acquire design documents and further advanced support.

Chapter 2

Mechanical Information

This chapter details mechanical information for the SOM-A350 CPU Computer on Module.

Sections include:

- Board Information
- Mechanical Drawings
- Assembly Drawings

2.1 Board Information

The figures below demonstrate the main chips on SOM-A350 Computer-on-Module.

Be aware of these positions while designing your customer's carrier board to avoid mechanical damage and to improve thermal dissipation performance.

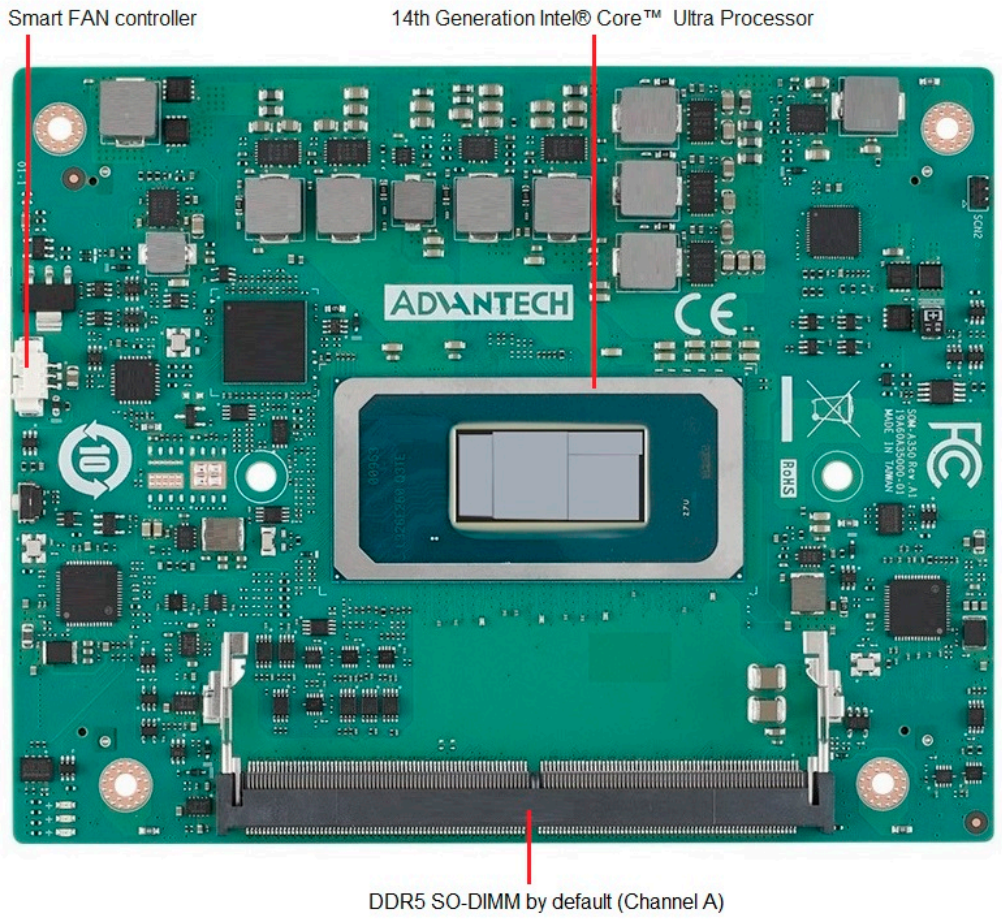


Figure 2.1 Board Chips – Front

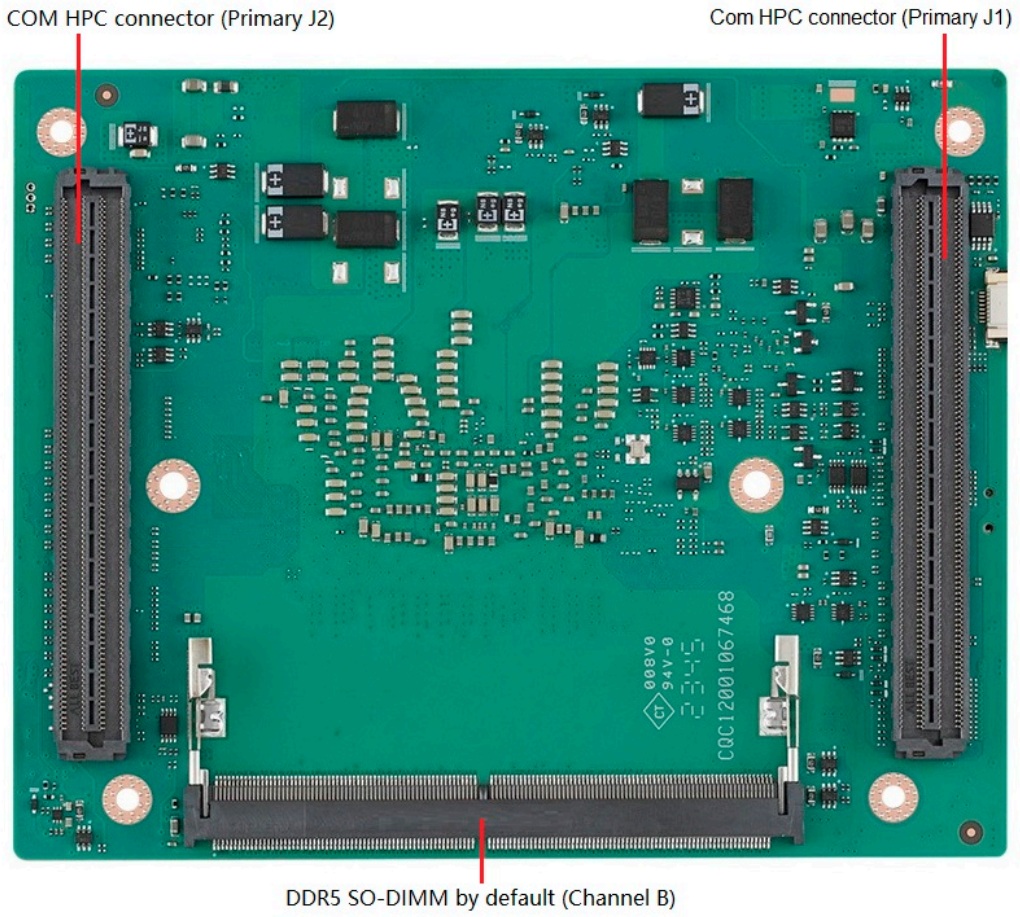


Figure 2.2 Board Chips – Rear

2.2 Mechanical Diagram

For more details regarding 2D/3D models, please visit the Advantech COM support service website http://com.advantech.com.

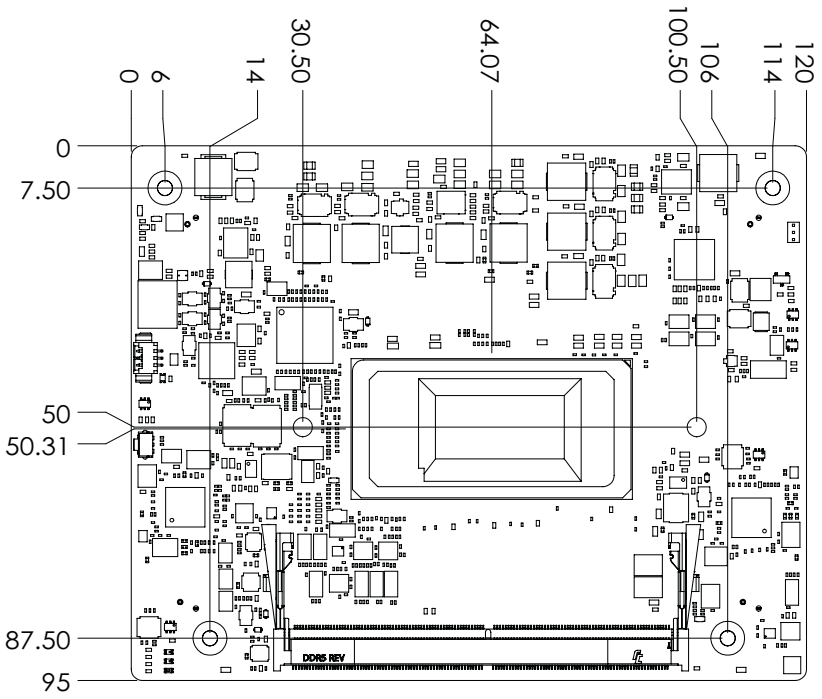


Figure 2.3 Board Mechanical Diagram – Front

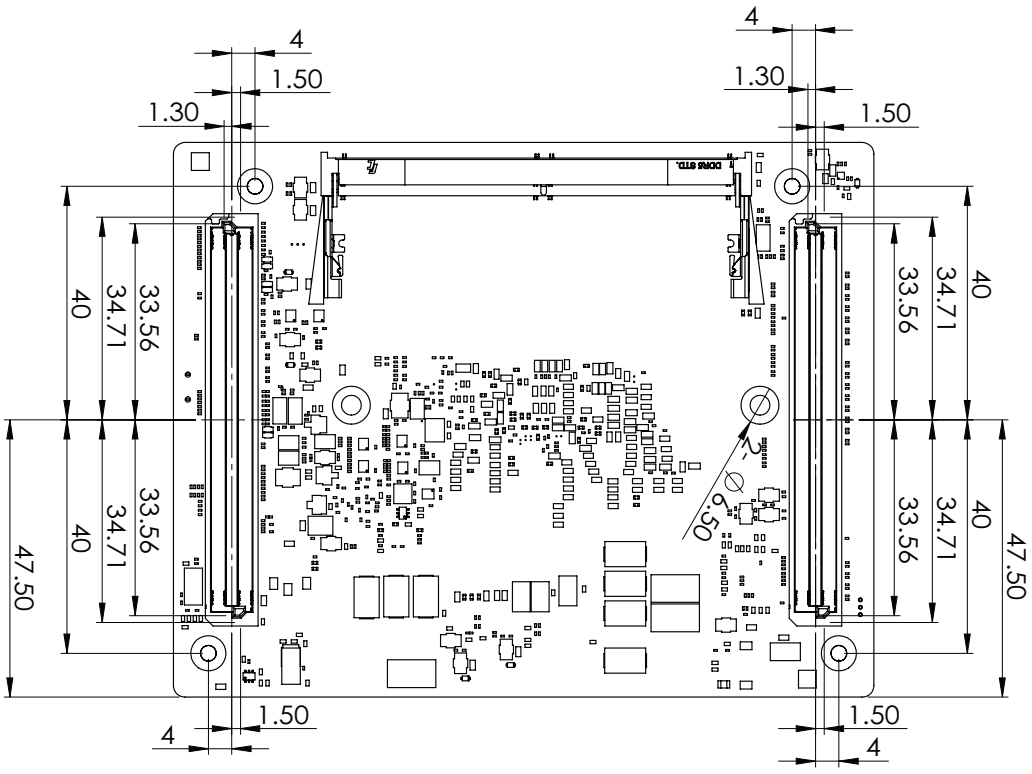


Figure 2.4 Board Mechanical Diagram – Rear

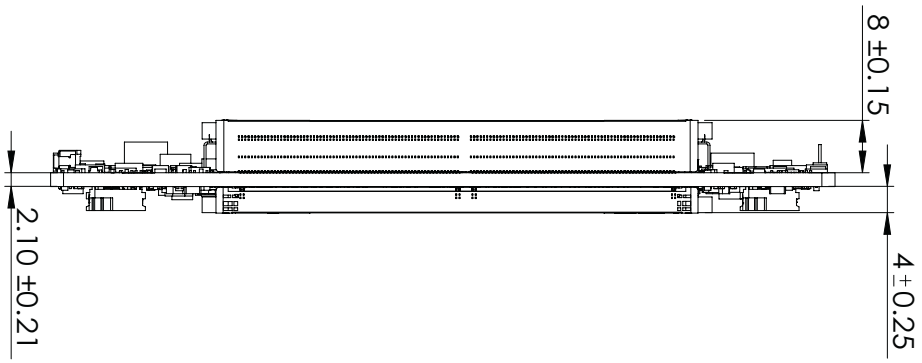


Figure 2.5 Board Mechanical Diagram – Side 1

2.3 Assembly Diagram

These figures demonstrate the order of assembly needed when attaching the thermal module and COM module to the carrier board.

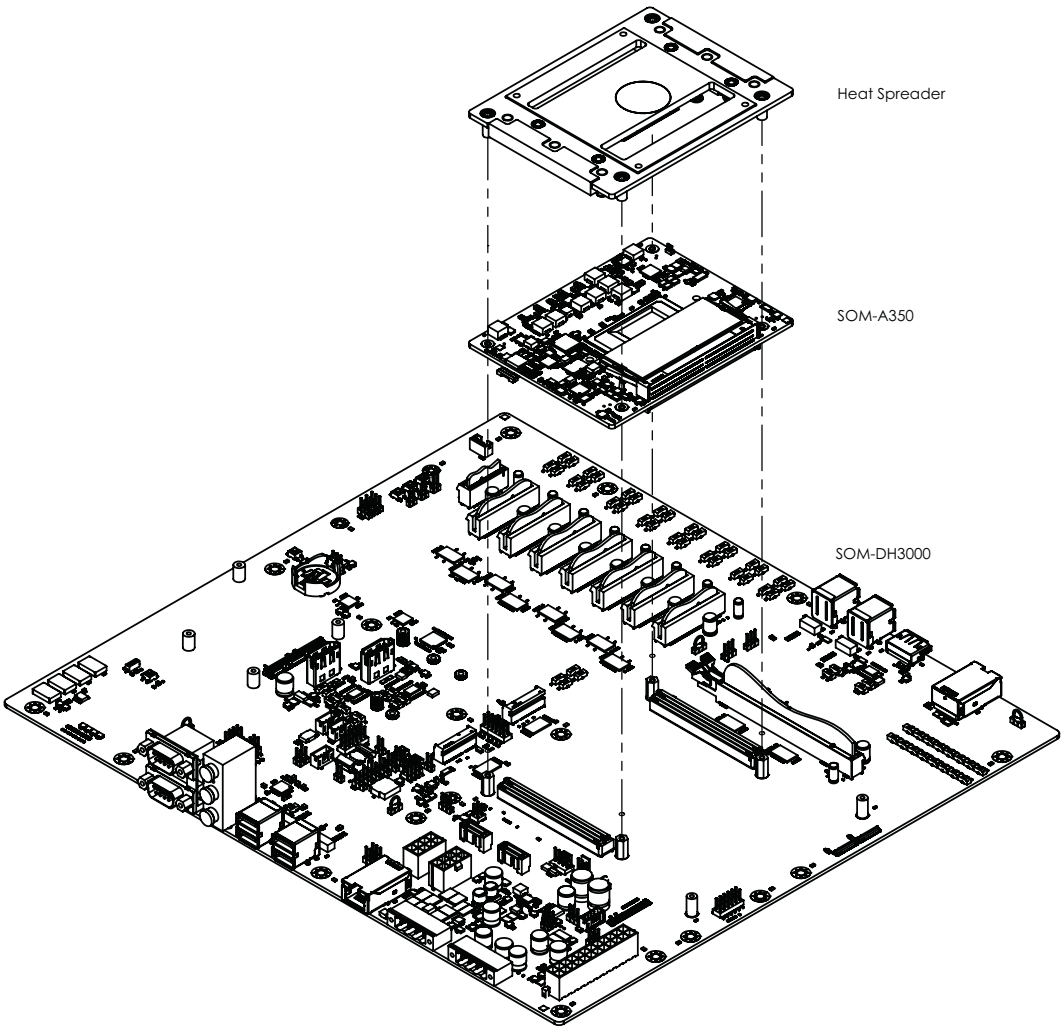


Figure 2.6 Assembly Diagram

There are 2 reserved screw holes for SOM-A350 to assemble the heat spreader.

2.4 Assembly Diagram

Since the COM-HPC board-to-board connector consists of 400 pins per connector, it is essential to vertically align the module and carrier board during assembly. Please adhere to the recommended orientation, as illustrated in the provided figures, to prevent any potential damage to the board-to-board connector.

Chapter 3

AMI BIOS

This chapter details BIOS setup information for the SOM-A350 CPU computer-on module.

Sections include:

- Introduction
- Entering Setup
- Hot/Operation Key
- Exit BIOS Setup Utility

3.1 Introduction

AMI BIOS has been integrated into many motherboards for over a decade. The AMI BIOS Setup Utility enables users to modify the BIOS settings and control various system features. This chapter describes the basic navigation of the BIOS Setup Utility.

Figure 3.1 Setup Program Initial Screen

AMI's BIOS ROM has a built-in setup program that allows users to modify the basic system configuration. This information is stored in flash ROM so it retains the Setup information when the power is turned off.

3.2 Entering Setup

Turn on the computer and then press <DEL> or <ESC> to enter the Setup menu.

3.3 Main Setup

When users first enter the BIOS Setup Utility, users will see the Main setup screen.

Users can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.

Figure 3.2 Main Setup Screen

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

- **System time/System date**

  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.4 Advanced BIOS Features Setup

Select the Advanced tab from the SOM-A350 setup screen to enter the Advanced BIOS Setup screen. Users can select any item in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. Users can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens are shown below. The sub menus are described on the following pages.

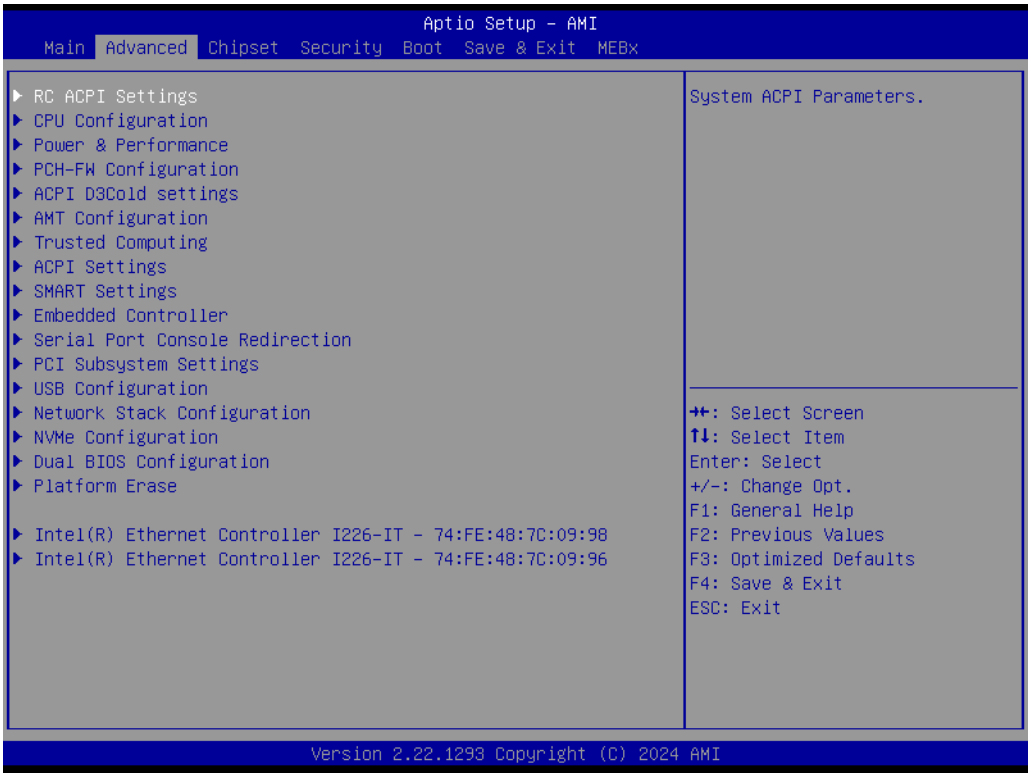


Figure 3.3 Advanced BIOS Features Setup Screen

- **RC ACPI Settings**
  System ACPI Parameters.
- **CPU Configuration**
  CPU Configuration Parameters.
- **Power & Performance**
  Power & Performance Options.
- **PCH-FW Configuration**
  Configure Management Engine Technology Parameters.
- **AMT Configuration**
  Configure Intel(R) Active Management Technology Parameters.
- **Trusted Computing**
  Trusted Computing Settings.
- **ACPI Settings**
  ACPI Sleep State.
- **SMART Settings**
  System SMART Settings.
- **Embedded Controller**
  Embedded Controller Parameters.

- **Serial Port Console Redirection**
  Console Redirection Settings.
- **PCI Subsystem Settings**
  PCI Subsystem Settings
- **USB Configuration**
  USB Configuration Parameters.
- **Network Stack Configuration**
  Network Stack Settings.
- **NVMe Configuration**
  NVMe Device Options Settings.
- **Dual BIOS Configuration**
  Dual BIOS configuration. (If 2 flashes be equipped on module.)
- **Platform Erase**
  Platform Erase
- **Intel® Ethernet Controller I226-LMvP**
  Configure Gigabit Ethernet device parameters.

3.4.1 RC ACPI Settings

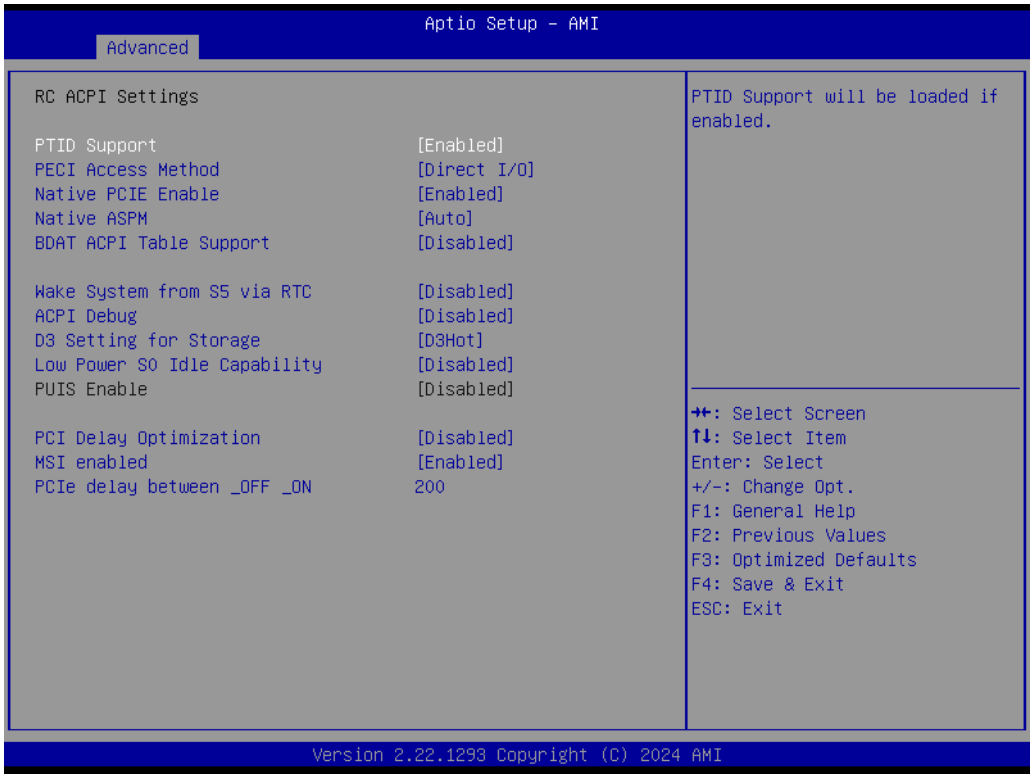


Figure 3.4 RC ACPI Settings

- **PTID Support**
  PTID Support will be loaded if enabled.
- **PCIE Access Method**
  PCIE Access Method is Direct I/O or ACPI.
- **Native PCIE Enable**
  Bit-PCIe Native*control
  0-~Hot Plug

1- SHPC Native Hot Plug control
2- 2-~Power Management Events
3- 3-PCIe Advanced Error Reporting control
4- 4-PCIe Capability Structure control
5- Latency Tolerance Reporting control

- **Native ASPM**
  Enabled-OS Controlled ASPM, Disabled-BIOS Controlled ASPM.
- **BDAT ACPI Table Support**
  Enables support for the BDAT ACPI table.
- **Wake System from S5 via RTC**
  Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified.
- **ACPI Debug**
  Open a memory buffer for storing debug strings. Reenter SETUP after enabling to see the buffer address. Use method ADBG to write strings to buffer.
- **D3 Setting for Storage**
  RTD3 support for Storage. PCIE storage PEP constraint needs to be set as D0/F1 (Intel Advanced->ACPI Settings->PEP PCIe Storage) when this setup is disabled/D3Hot.
- **Low Power S0 Idle Capability**
  This variable determines if we enable ACPI Lower Power S0 Idle Capability (Mutually exclusive with Smart connect). While this is enabled, it also disables 8524 timer for SLP_S0 support.
- **PCI Delay Optimization**
  Experimental ACPI additions for FW latency optimizations.
- **MSI enabled**
  When disabled, MSI support is disabled in FADT.
- **PCIe delay between_OFF_ON**
  PCIe delay between _OFF _ON.

3.4.2 CPU Configuration

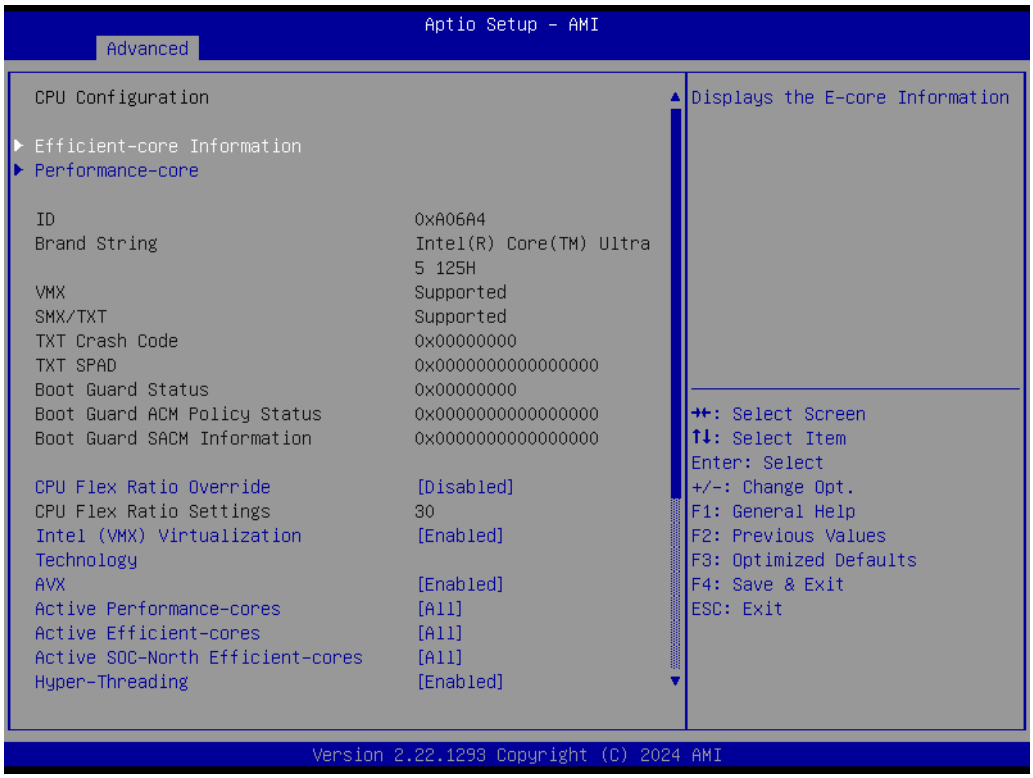


Figure 3.5 CPU Configuration

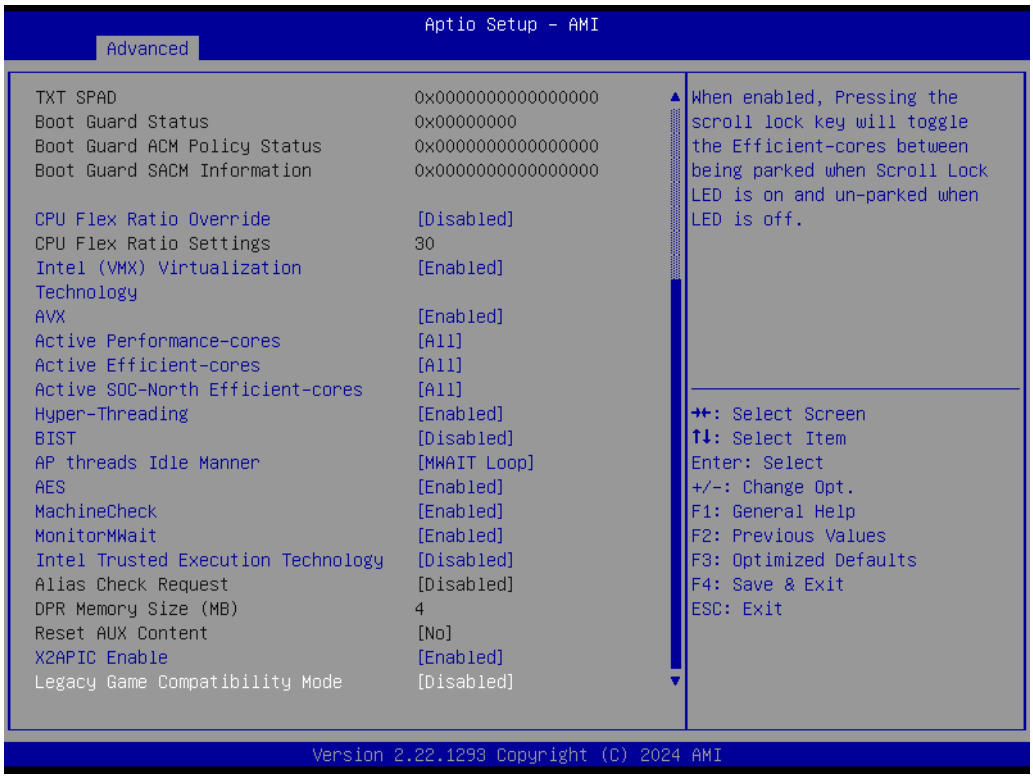


Figure 3.6 CPU Configuration

- **Efficient-core Information**
  Displays the E-core Information
- **Performance-core**
  Displays the P-core Information.
- **CPU Flex Ratio Override**
  Enable or Disable CPU Flex Ratio Programming.
- **Intel (VMX) Virtualization Technology**
  When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
- **AVX**
  Enable/Disable the AVX and AVX2 Instructions.
- **Active Performance-cores**
  Number of P-cores to enable in each processor package, Note: Number of Cores and E-cores are looked at together.When both are {0,0}, Pcode will enable all cores.
- **Active Efficient-cores**
  Number of E-cores to enable in each processor package, Note: Number of Cores and E-cores are looked at together.When both are {0,0}, Pcode will enable all cores.
- **Active SOC-North Efficient-cores**
  Number of SOC-North Efficient-cores to enable in SOC North.
- **Hyper-Threading**
  Enable or Disable Hyper-Threading Technology.
- **BIST**
  Enable/Disable BIST (Built-In Self Test) on reset.
- **AP threads Idle Manner**
  AP threads Idle Manner for waiting signal to run.
- **AES**
  Enable/Disable AES (Advanced Encryption Standard).
- **MachineCheck**
  Enable/Disable Machine Check.
- **MonitorMWait**
  Enable/Disable MonitorMwait, if Disable MonitorMwait, the AP threads Idle Manner should not set in MWAIT Loop.
- **Intel Trusted Execution Technology**
  Enables utilization of additional hardware capabilities provided by Intel (R)
  Trusted Execution Technology. Changes require a full power cycle to take effect.
- **X2APIC Enable**
  Enable/Disable X2APIC Operating Mode. When this option is configured as ‘Enabled’, ‘VT-d’ option must be ‘Enabled’ and ‘X2APIC’ Opt Out ‘option must be ‘Disabled’ as well. This option will be grayed out when ’VT-d’ option is configured as ‘Disabled’.
- **Legacy Game Compatibility Mode**
  When enabled, Pressing the scroll lock key will toggle the Efficient-cores between being parked when Scroll Lock LED is on and un-parked when LED is off.

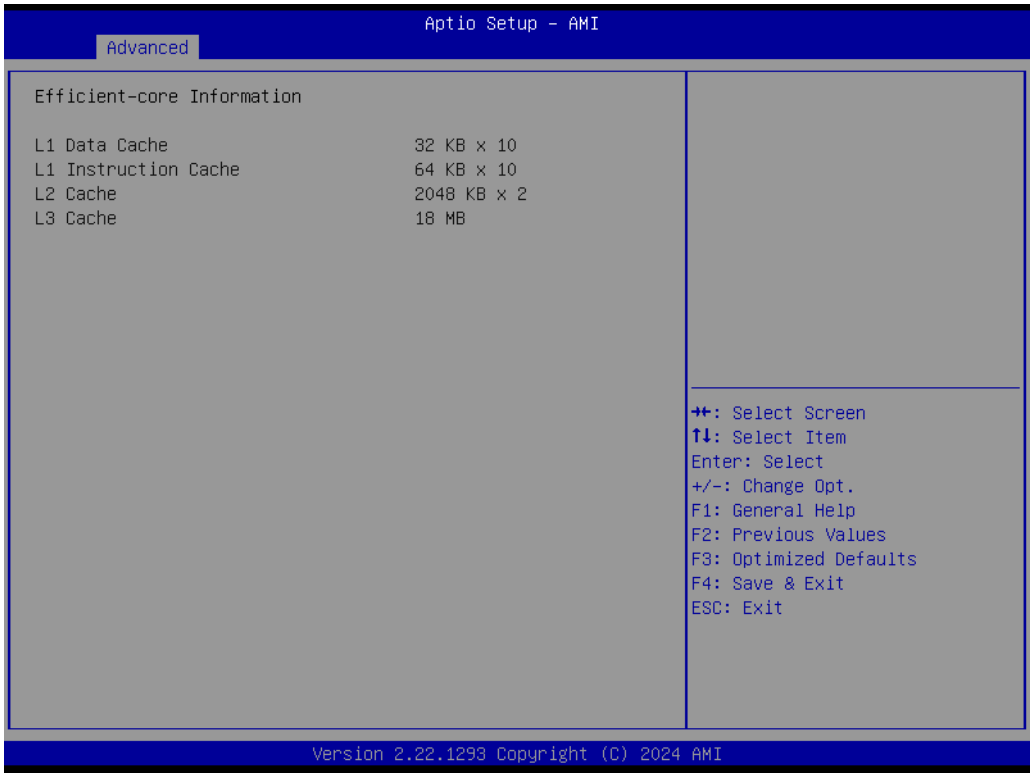


Figure 3.7 Efficient-core Information

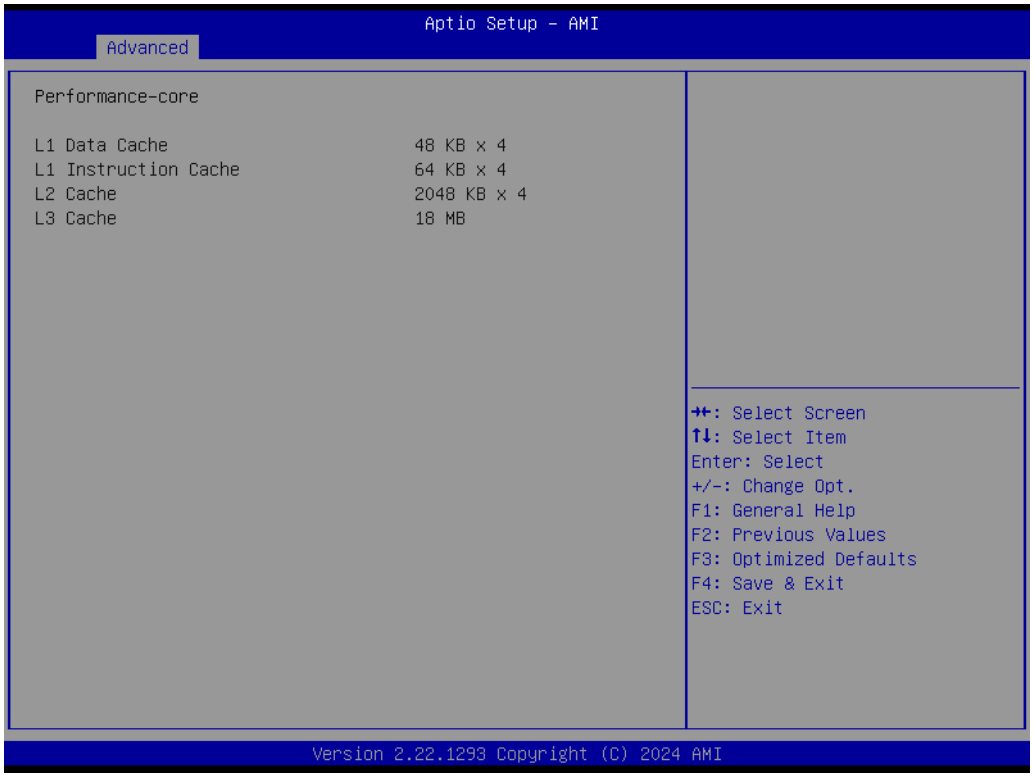


Figure 3.8 Performance-core

3.4.3 Power & Performance

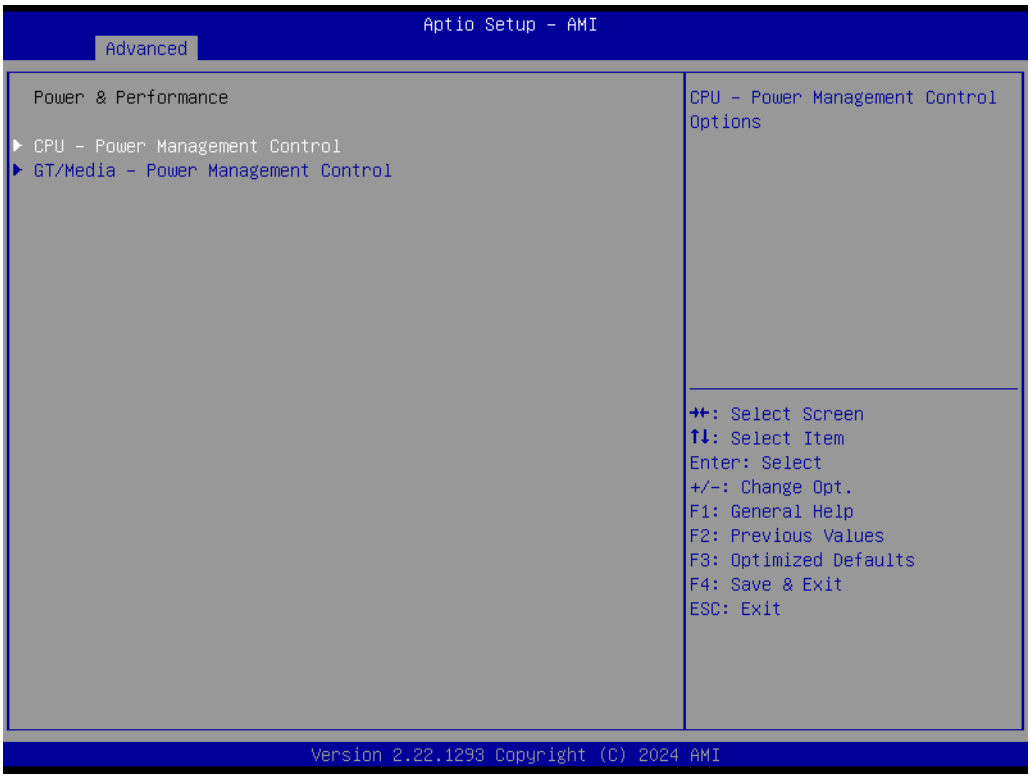


Figure 3.9 Power & Performance

- **CPU - Power Management Control**
  CPU - Power Management Control Options.
- **GT/Media - Power Management Control**
  GT/Media - Power Management Control Options.

3.4.3.1 CPU - Power Management Control

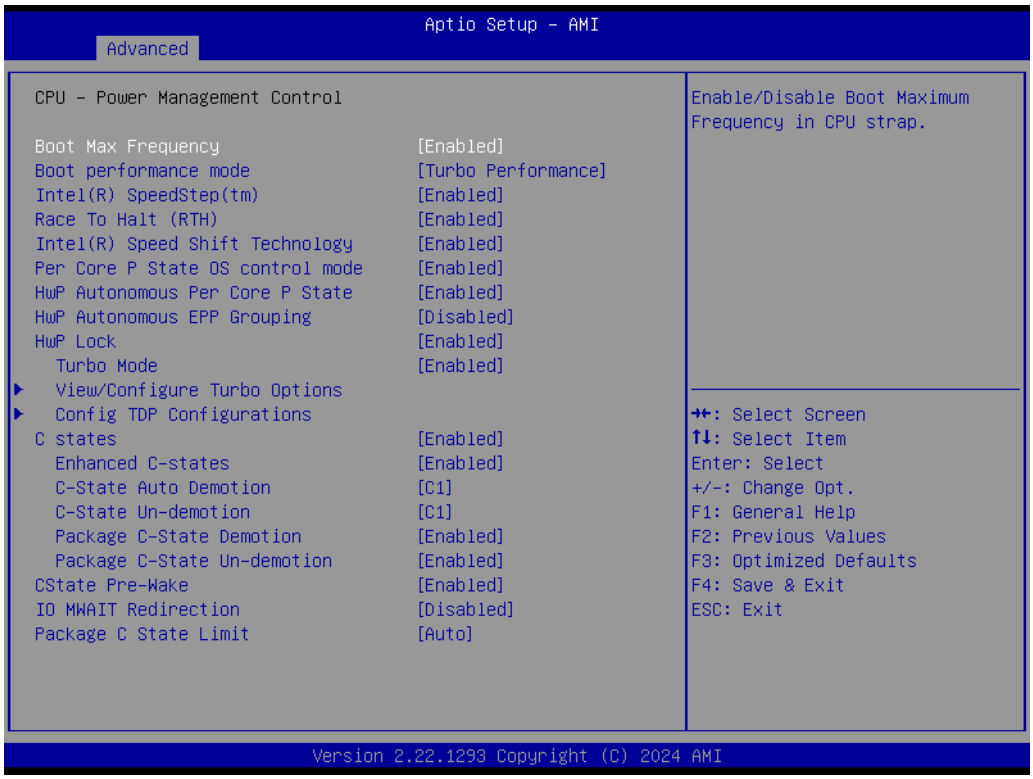


Figure 3.10 CPU-Power Management Control

- **Boot Max Frequency**
  Enable/Disable Boot Maximum Frequency in CPU strap.
- **Boot performance mode**
  Select the performance state that the BIOS will set starting from reset vector.
- **Intel(R) SpeedStep(tm)**
  Allows more than two frequency ranges to be supported.
- **Race To Halt(RTH)**
  Enable/Disable Race To Halt feature. RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall power.
- **Intel(R) Speed Shift Technology**
  Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.
- **Per Core P State OS control mode**
  Enable/Disable Per Core state OS control mode. When set, ,the highetst core request is used for all other core requests.
- **HwP Autonomous Per Core P State**
  Disable Autonomous PCPS Autonomous will request the same value for all cores all the time.
- **HwP Autonomous EPP Grouping**
  Enable EPP grouping Autonomous will request the same values for all cores with same EPP. Disable EPP grouping autonomous will not necessarily request same values for all cores with same EPP.
- **HwP Lock**
  Enable/Disable HWP Lock support in Misc Power Management MSR.
- **Turbo Mode**

Enable/Disable processor Turbo Mode.

- **View/Configure Turbo Options**
  View/Configure Turbo Options.
- **Config TDP Configurations**
  cTDP (Assured Power) Configurations.
- **C states**
  Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.
- **Enhanced C-states**
  Enable/Disable C1E. When enabled, CPU will switch to minimum speed when all cores enter C-State.
- **C-State Auto Demotion**
  Configure C-State Auto Demotion
- **C-State Un-demotion**
  Configure C-State Un-demotion.
- **Package C-State Demotion**
  Package C-State Demotion.
- **Package C-State Un-demotion**
  Package C-State Un-demotion.
- **CState Pre-Wake**
  Disable-to 1 to disable the Cstate Pre-Wake.
- **IO MWAIT Redirection**
  When set. Will map IO_read instuctions sent to IO registers PMG_IO_BASE_ADDRBASE+offset to MWAIT(offset).
- **Package C State Limit**
  Maximum Package C State Limit Setting. Cpu Default: Leaves to Factory default value. Auto: Initializes to deepest available Package C State Limit.

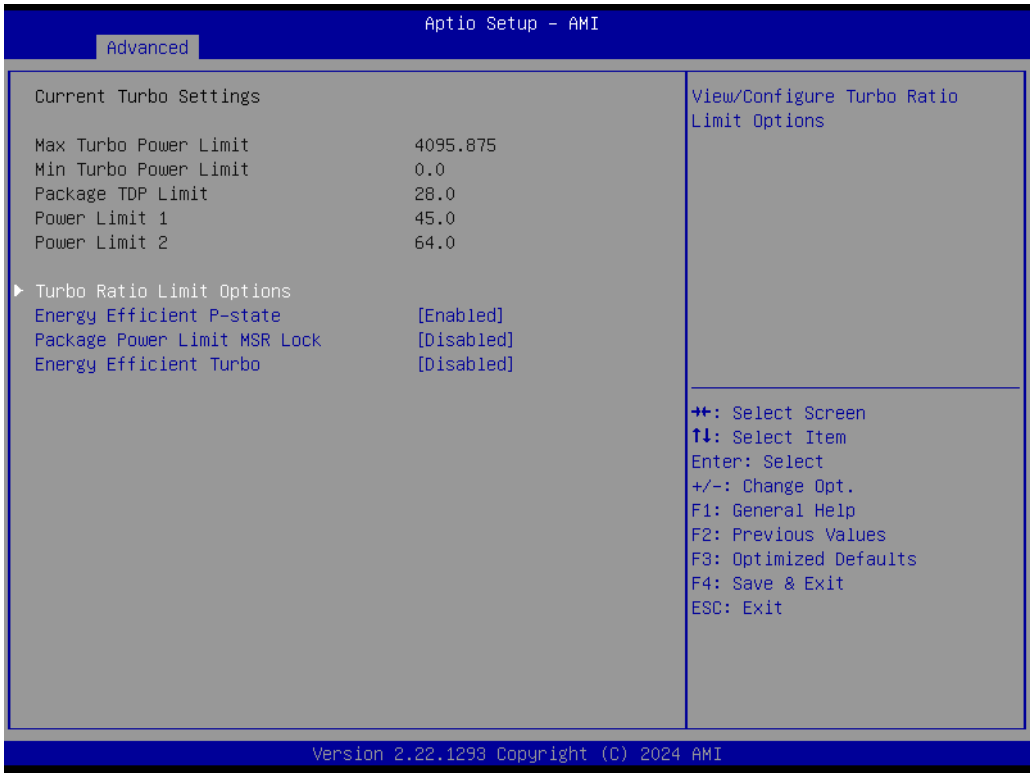


Figure 3.11 Current Turbo Settings

- **Turbo Ratio Limit Options**
  View/Configure Turbo Ratio Limit Options.
- **Energy Efficient P-state**
  Enable/Disable Enerfy Efficient P-state feature. When set to 0. will disable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID Function will read 0 indicating no support for Energy Efficient policy setting. When set to 1 will enable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID Function will read 1 indicating Energy Efficient policy setting is supported.
- **Package Power Limit MSR Lock**
  Enable/Disable locking of Package Power Limit settings. When enabled, PACKAGE_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.
- **?Energy Efficient Turbo**
  Enable/Disable Energy Efficient Turbo Feature. This feature will opportunistically lower the turbo frequency to increase efficiency. Recommended only to disable in overclocking situations where turbo frequency must remain constant. Otherwise, leave enabled.

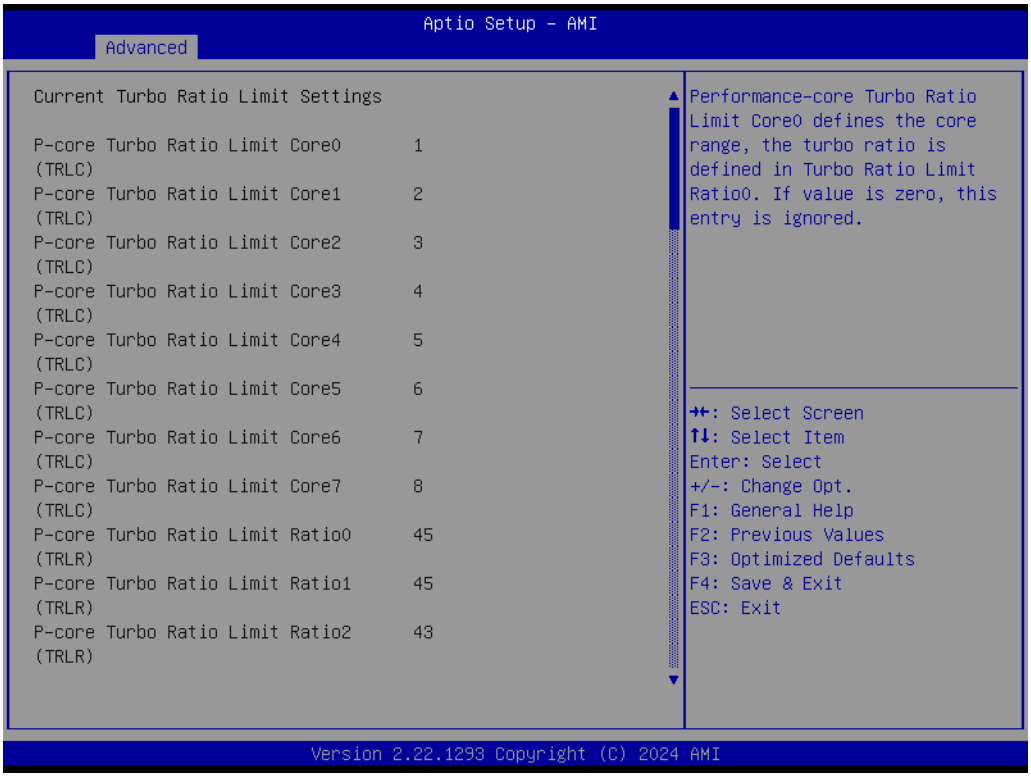


Figure 3.12 Current Turbo Ratio Limit Settings

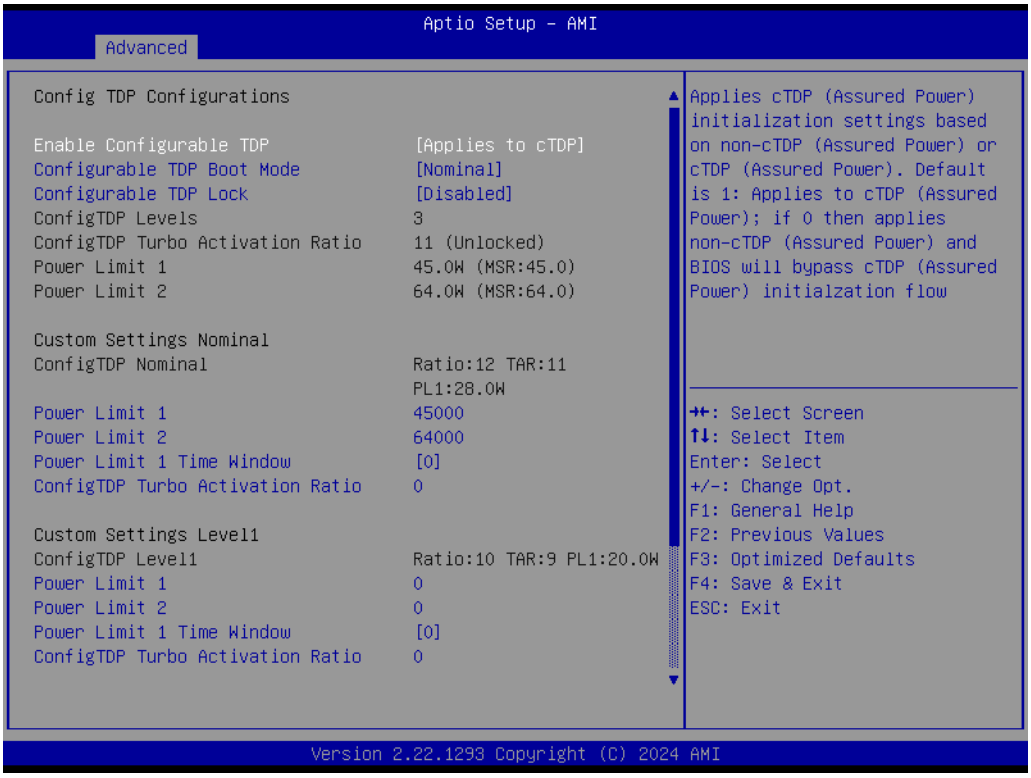


Figure 3.13 Config TDP Configurations

- **Enable Configurable TDP**

  Applies cTDP (Assured Power) initialization settings based on non-cTDP (Assured Power) or cTDP (Assured Power). Default is 1: Applies to cTDP (Assured Power)?if 0 then applies non-cTDP (Assured Power) and BIOS will bypass cTDP (Assured Power) initialization flow.

- **Configurable TDP Boot Mode**

  cTDP (Assured Power) Mode as Nominal/Level1/Level2/Deactivate TDP (Base Power) selection. Deactivate option will set MSR to Nominal and MMIO to Zero.

- **Configurable TDP Lock**

  cTDP (Assured Power) Mode Lock sets the Lock bits on TURBO_ACTIVATION_RATIO and CONFIG_TDP_CONTROL. Note: When cTDP (Assured Power) Lock is enabled Custom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.

- **Power Limit 1**

  Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.50W, enter 12500. Overlocking SKU: Value must be between Max and Min Power Limits. Other SKUs: This value must be between Min Power Limit and Processor Base (TDP) Limit.

- **Power Limit 2**

  Power Limit 2 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.

- **Power Limit 1 Time Window**

  Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0=default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which Processor Base Power (TDP) value should be maintained.

- **ConfigTDP Turbo Activation Ratio**

  Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don’t use custom value.

- **Power Limit 1**

  Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.50W, enter 12500. Overlocking SKU: Value must be between Max and Min Power Limits. Other SKUs: This value must be between Min Power Limit and Processor Base (TDP) Limit.

- **Power Limit 2**

  Power Limit 2 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.

- **Power Limit 1 Time Window**

  Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0=default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which Processor Base Power (TDP) value should be maintained.

- **ConfigTDP Turbo Activation Ratio**

  Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don’t use custom value.

3.4.3.2 GT/Media-Power Management Control

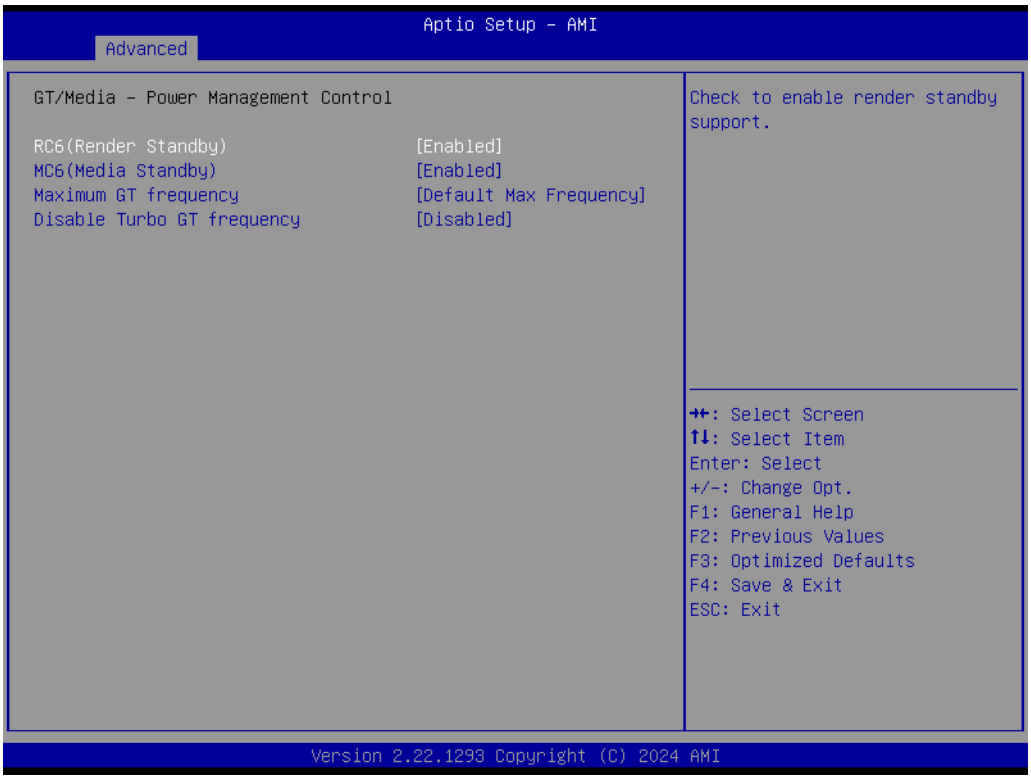


Figure 3.14 GT/Media-Power Management Control

- **RC6(Render Standby)**
  Check to enable render standby support.
- **MC6(Media Standby)**
  Check to enable Media standby support.
- **Maximum GT frequency**
  Maximum GT frequency limited by the user. Choose between 2400MHx(RPN) and 6900MHz(RP0). Value beyond the range will be clipped to min/max supported by SKU.
- **Disable Turbo GT frequency**
  Enabled: Disable Turbo GT frequency. Disabled: GT frequency is not limited.

3.4.4 PCH-FW Configuration

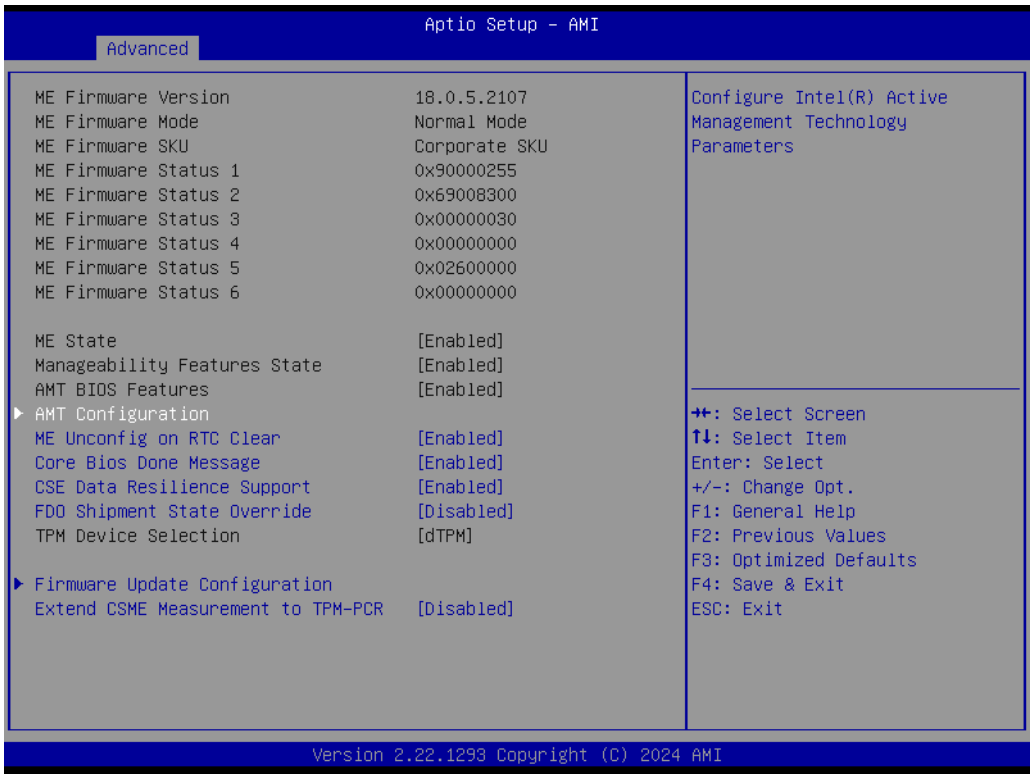


Figure 3.15 PCH-FW Configuration

- **AMT Configuration**
  Configure Intel(R) Active Management Technology Parameters.
- **ME Unconfig on RTC Clear**
  When Disabled ME will not be unconfigured on RTC clear.
- **Core Bios Done Message**
  Enable/Disabled Core Bios Done message sent to ME.
- **CSE Data Resilience Support**
  Enable/Disable CSE Data Resilience Support.
- **FD0 Shipment State Override**
  Enable/Disable FD0 Shipment State Override. BIOS will override soft strap setting when enabled.
- **Firmware Update Configuration**
  Configure Intel(R) Active Management Technology Parameters.
- **Extend CSME Measurement to TPM-PCR**
  Enable/Disable Extend CSME Measurement to TPM-PCR[0] and AMT Config to TPM-PCR[1].

3.4.5 ACPI D3Cold settings

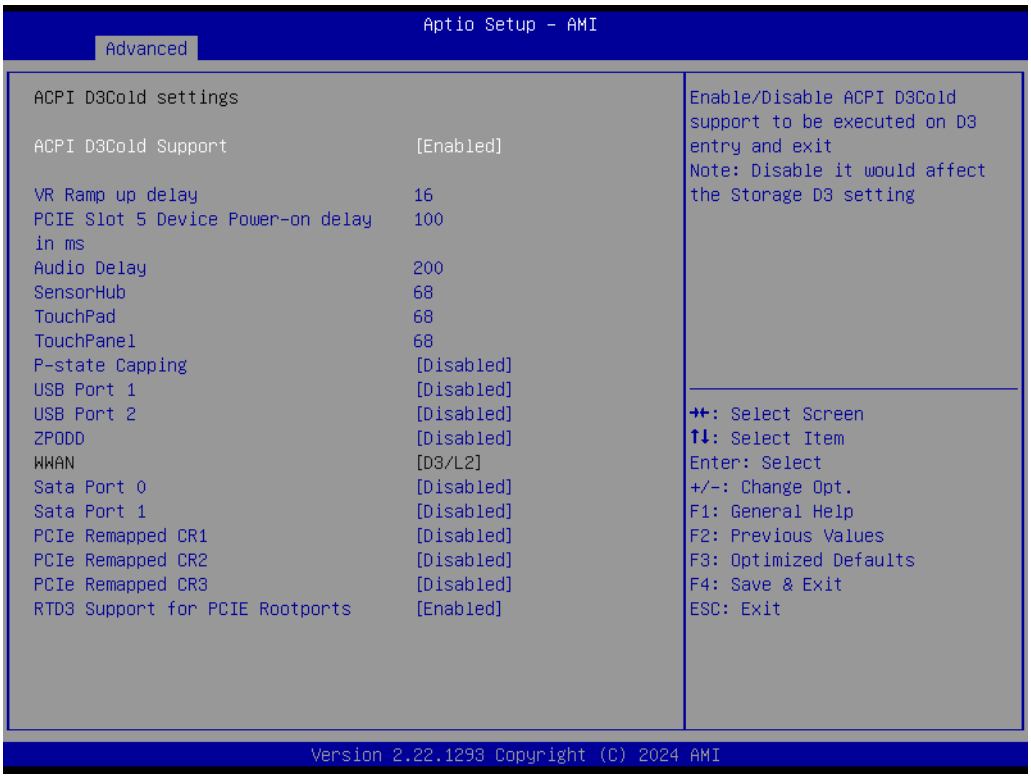


Figure 3.16 ACPI D3Cold settings

- **ACPI D3Cold Support**
  Enable/Disable ACPI D3Cold support to be executed on D3 entry and exit. Note: Disable it would affect the storage D3 setting.
- **VR Ramp up to delay**
  Delay between subsequent VR ramp up if they are all Turn ON at the same time.
- **PCIE Slot 5 Device Power-on delay**
  Delay between applying core power and Deasserting PERST#
- **Audio Delay**
  Delay after applying power to HD Audio(Realtek) codec device.
- **SensorHub**
  Delay after applying power to SensorHub device.
- **TouchPad**
  Delay after applying power to Touchpad device.
- **TouchPanel**
  Delay in PR-ON after applying power to TouchPanel device.
- **P-state Capping**
  Set _PPC and send ACPI notification.
- **USB Port 1**
  USB RTD3 support. Super Speed: USB3.0 devices will be exposed as RTD3 capable. High Speed: USB2.0 devices will be exposed as RTD3 capable. Disabled: USB RTD3 support disabled. For SawtoothPeak USB Port1(Below) is Superspeed and Port2(Top) is HighSpeed. Check respective board configuration to know about USB port position.

- **USB Port 2**
  USB RTD3 support. Super Speed: USB3.0 devices will be exposed as RTD3 capable. High Speed: USB2.0 devices will be exposed as RTD3 capable. Disabled: USB RTD3 support disabled. For SawtoothPeak USB Port1(Below) is Superspeed and Port2(Top) is HighSpeed. Check respective board configuration to know about USB port position.
- **ZPODD**
  Zero Power ODD option is applicable only for the board with ZPODD support.
- **Sata Port 0**
  Setup option to control the SATA port RTD3 functionality.
- **Sata Port 1**
  Setup option to control the SATA port RTD3 functionality.
- **PCIe Remapped CR1**
  PCIe RTD3 setup conflicts with SATA RTD3. Platform specific.
- **PCIe Remapped CR2**
  PCIe RTD3 setup conflicts with SATA RTD3. Platform specific.
- **PCIe Remapped CR3**
  PCIe RTD3 setup conflicts with SATA RTD3. Platform specific.
- **RTD3 Support for PCIE Rootports**
  Enable/Disable PCIE RTD3 Support.

3.4.6 AMT Configuration

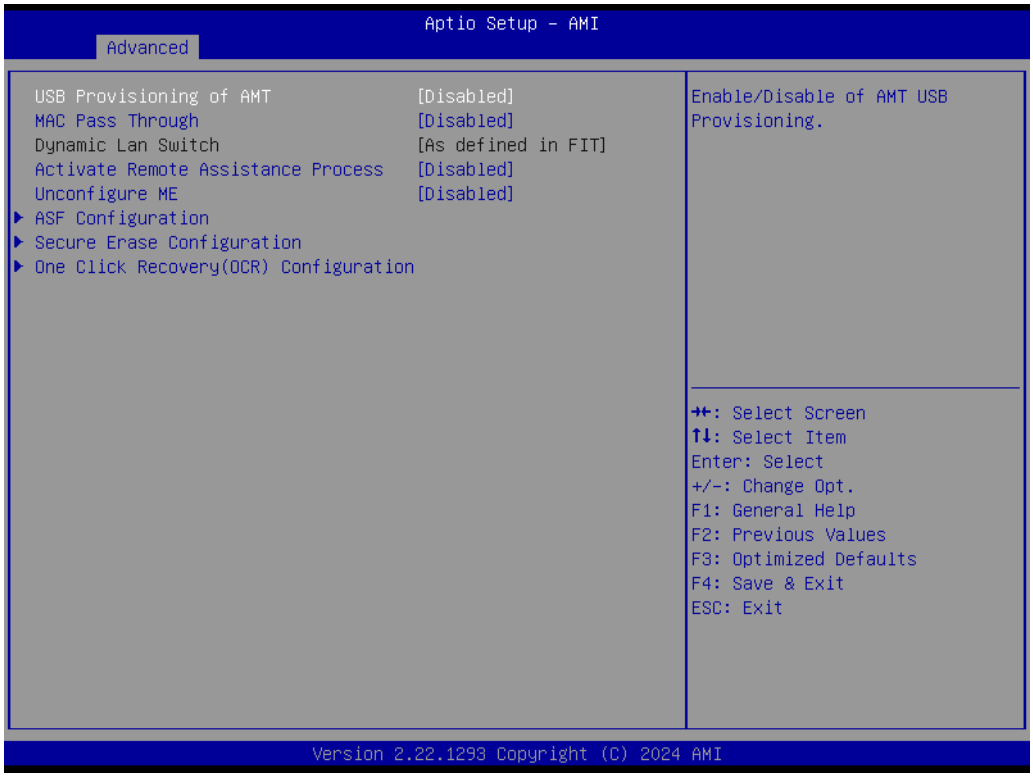


Figure 3.17 AMT Configuration

- **USB Provisioning of AMT**
  Enable/Disable of AMT USB Provisioning.
- **MAC Pass Through**

Enable/Disable MAC Pass Through function.

- **Activate Remote Assistance Process**
  Tiger CIRA boot Note: Network Access must be activated first from MEBx Setup.
- **Unconfigure ME**
  Unconfigure ME with resetting MEBx password to default on next boot.
- **ASF Configuration**
  Configure Alert Standard Format parameters.
- **Secure Erase Configuration**
  Secure Erase configuration menu.
- **One Click Recovery(OCR) Configuration**
  Configuration setting for One Click Recovery. This allows access for AMT to boot a recovery IS application.

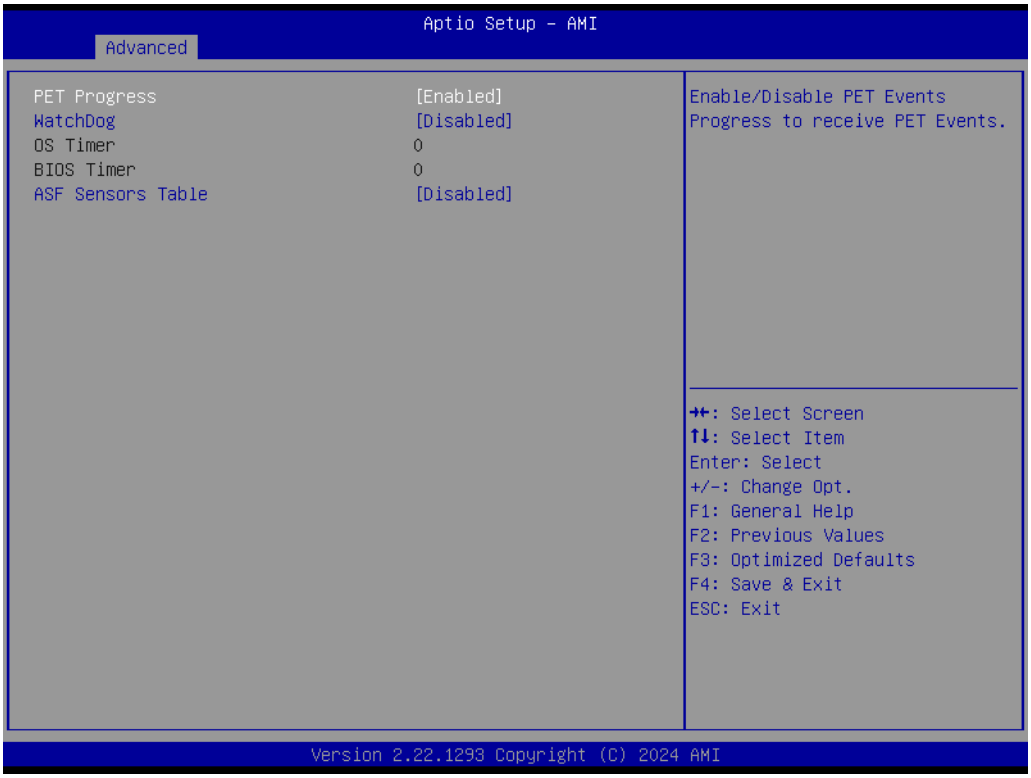


Figure 3.18 ASF Configuration

- **PET Process**
  Enable/Disable PET Events Progress to receive PET Events.
- **WatchDog**
  Enable/Disable WatchDog Timer.
- **ASF Sensors Table**
  Adds ASF Sensor Table into ASF! ACPI Table.

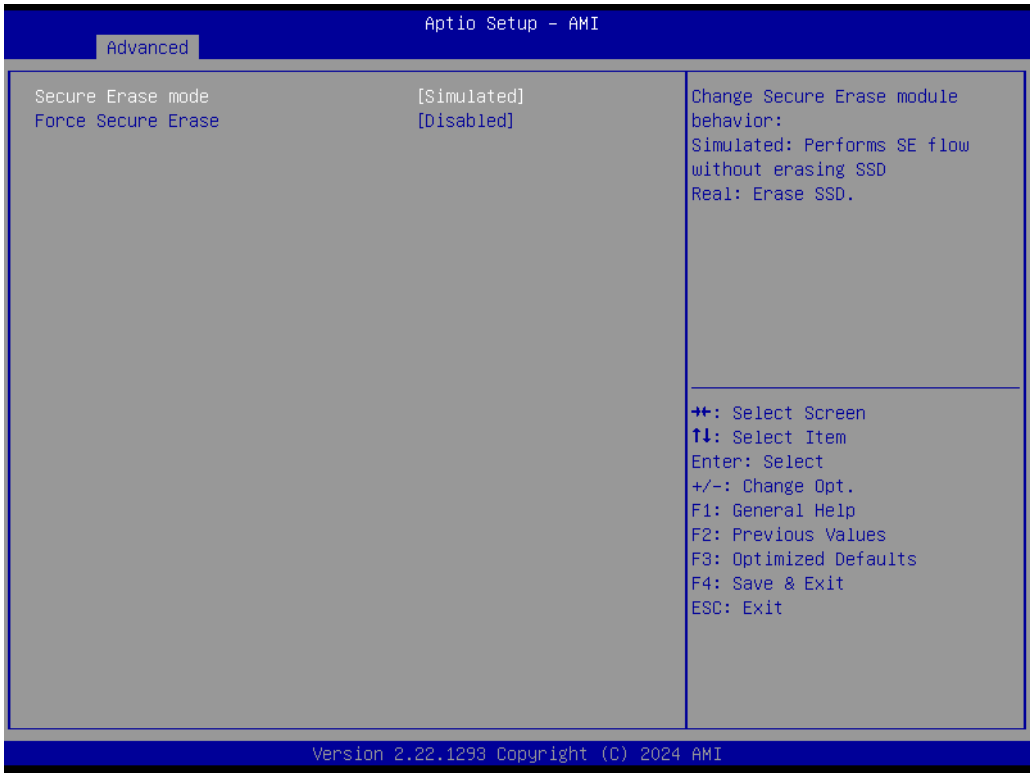


Figure 3.19 Secure Erase Configuration

- **Secure Erase mode**
  Change Secure Erase module behavior: Simulated: Performs SE flow without erasing SSD Real: Erase SSD.
- **Force Secure Erase**
  Force Secure Erase on next boot.

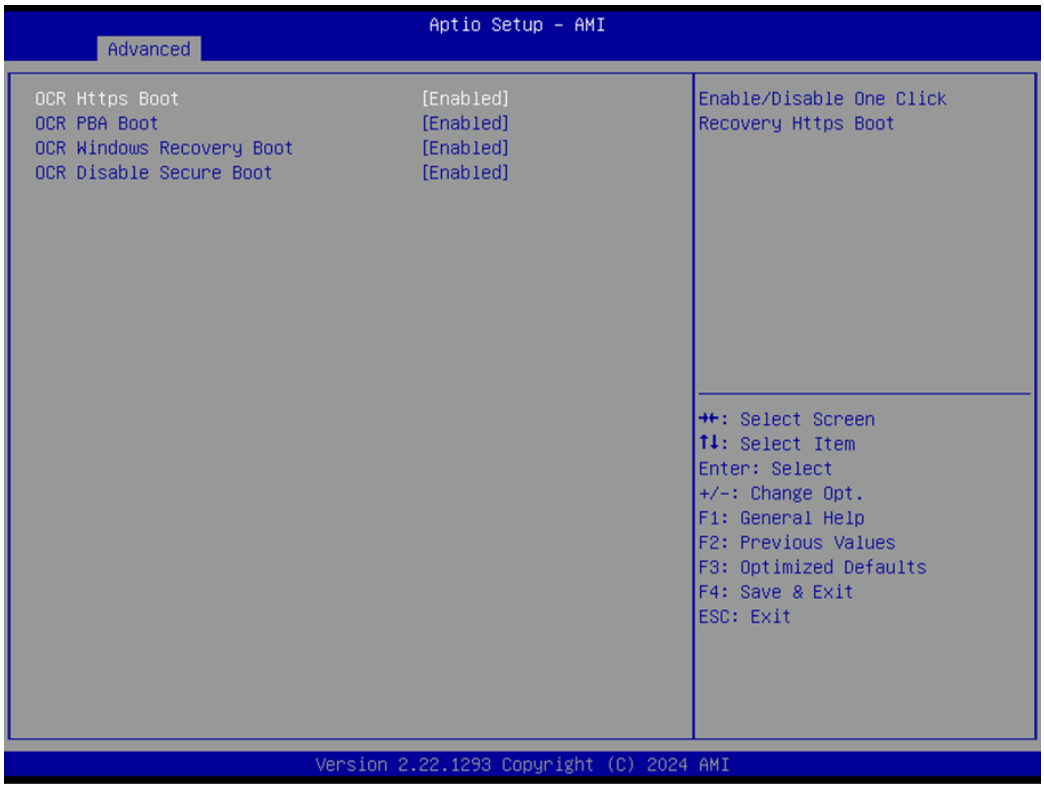


Figure 3.20 One Click Recovery(OCR) Configuration

- **OCR Https Boot**
  Enable/Disable One Click Recovery Https Boot.
- **OCR PBA Boot**
  Enable/Disable One Click Recovery PBA Boot.
- **OCR Windows Recovery Boot**
  Enable/Disable One Click Recovery Windows Recovery Boot.
- **OCR Disable Secure Boot**
  Allows CSME to request SecureBoot to be disabled for One Click Recovery.

3.4.7 Trusted Computing

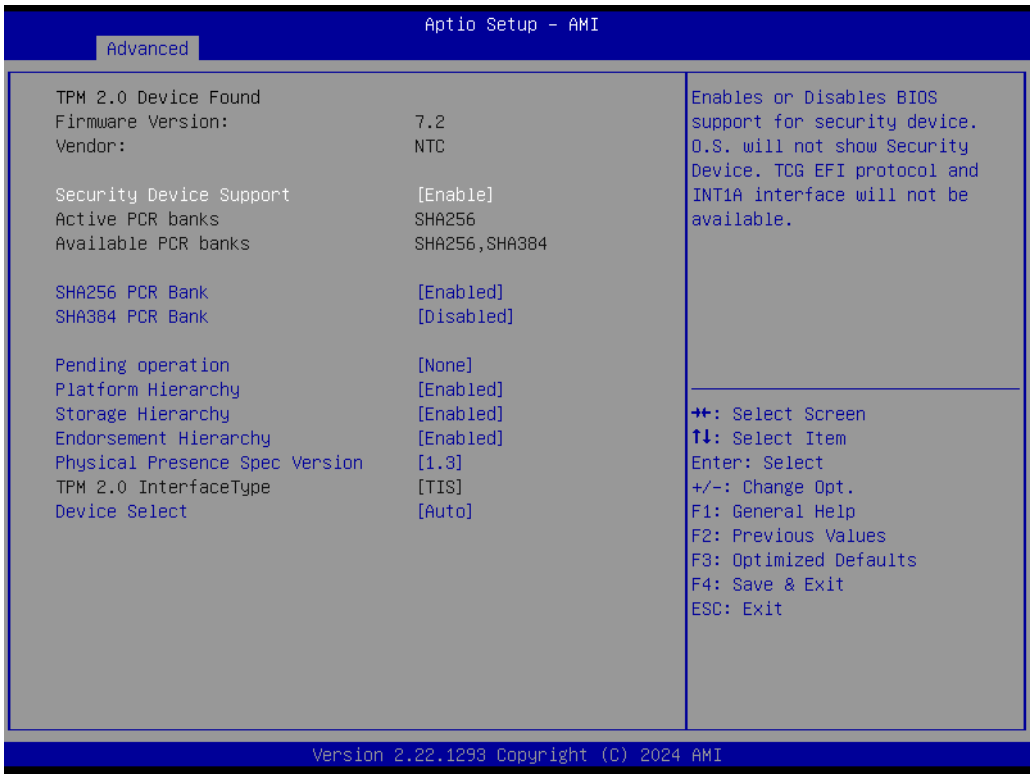


Figure 3.21 Trusted Computing

- **Security Device Support**
  Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
- **SHA256 PCR Bank**
  Enable or Disable SHA256 PCR Bank.
- **SHA384 PCR Bank**
  Enable or Disable SHA384 PCR Bank.
- **Pending operation**
  Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.
- **Platform Hierarchy**
  Enable or Disable Platform Hierarchy.
- **Storage Hierarchy**
  Enable or Disable Storage Hierarchy.
- **Endorsement Hierarchy**
  Enable or Disable Endorsement Hierarchy.
- **Physical Presence Spec Version**
  Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
- **Device Select**
  TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.

3.4.8 ACPI Settings

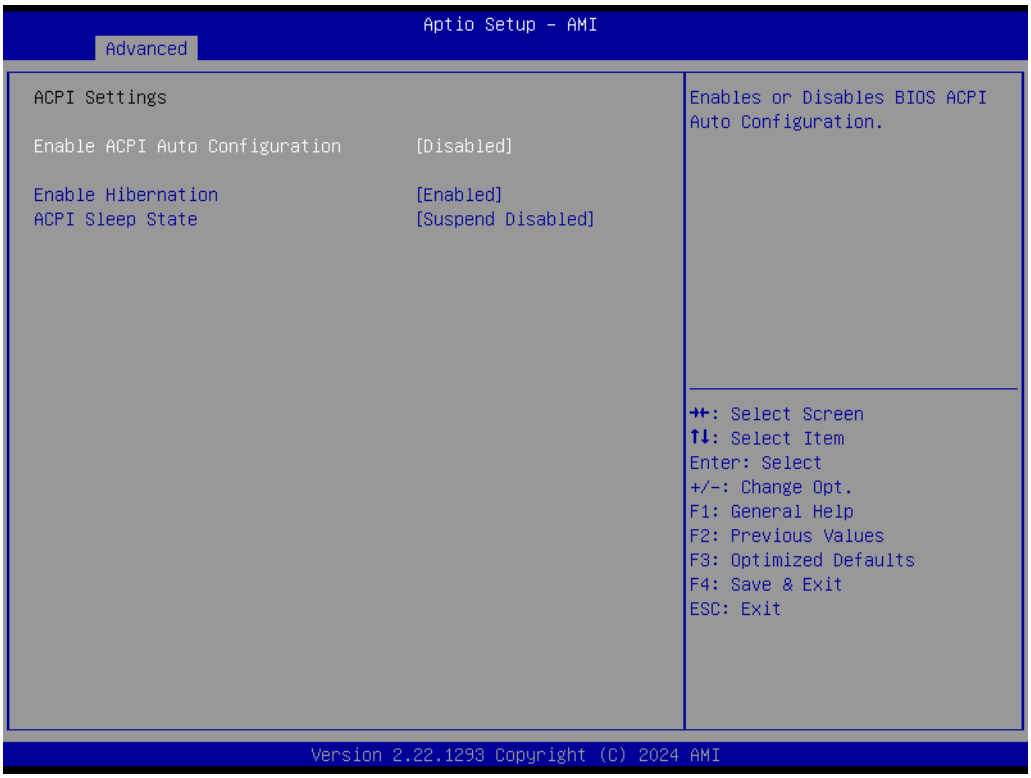


Figure 3.22 ACPI Settings

- **Enable ACPI Auto Configuration**
  Enable or Disable BIOS ACPI Auto Configuration.
- **Enable Hibernation**
- **ACPI Sleep State**

3.4.9 SMART Settings

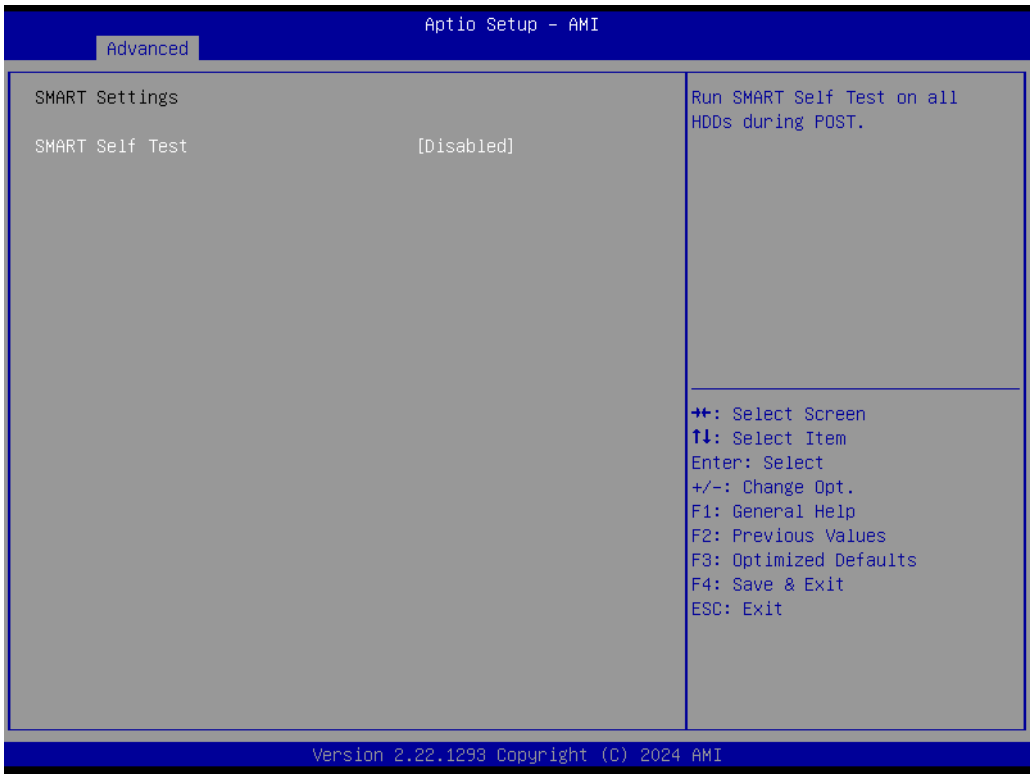


Figure 3.23 SMART Settings

- **SMART Self Test**
  Run SMART Self Test on all HDDs during POST.

3.4.10 Embedded Controller

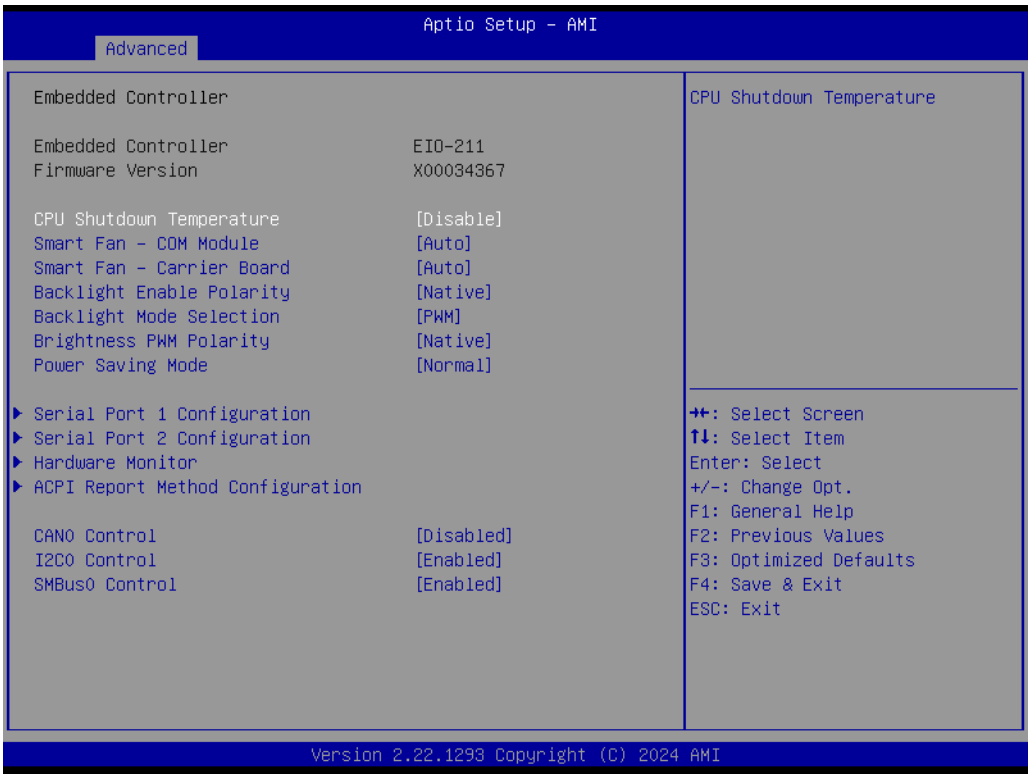


Figure 3.24 Embedded controller

- **CPU Shutdown Temperature**
  CPU Shutdown Temperature.
- **Smart Fan - COM Module**
  Control COM Module Smart FAN function.
- **Smart Fan - Carrier Board**
  Control Carrier Board Smart FAN function. Get value from EC and only set value when Save Changes.
- **Backlight Enable Polarity**
  Switch Backlight Enable Polarity for Native or Invert.
- **Backlight Mode Selection**
  Switch Backlight Control to PWM or DC mode.
- **Brightness PWM Polarity**
  Backlight Control Brightness PWM Polarity for Native or Invert.
- **Power Saving Mode**
  Select Power Saving Mode.
- **Serial Port 1 Configuration**
  Set Parameters of Serial Port 1 (COMA).
- **Serial Port 2 Configuration**
  Set Parameters of Serial Port 2 (COMB).
- **Hardware Monitor**
  Monitor hardware status.
- **ACPI Report Method Configuration**
  Select ACPI Reporting Method for EC Devices.
- **CAN0 Control**

Enable/Disable CAN0 controller on RDC-IS200.

- **I2C0 Control**
  Enable/Disable I2C0 controller on RDC-IS200.
- **SMBus0 Control**

3.4.11 Serial Port Console Redirection

3.4.11.1 Serial Port 1 Configuration

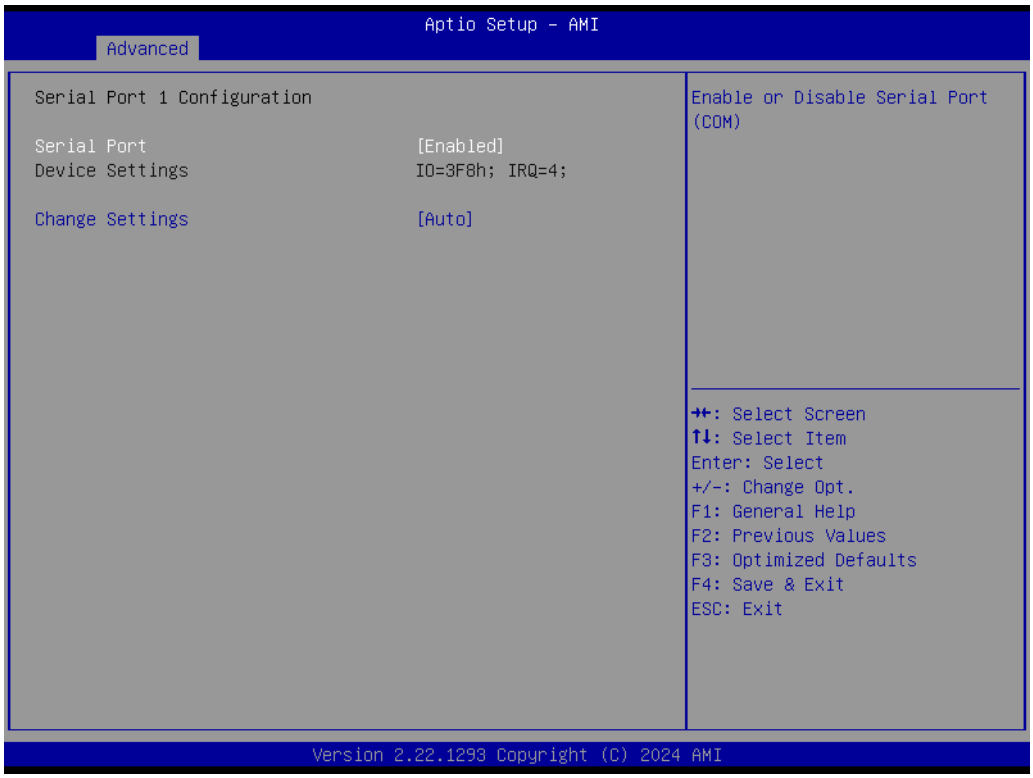


Figure 3.25 Serial Port 1 Configuration

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for Super IO Device.

3.4.11.2 Serial Port 2 Configuration

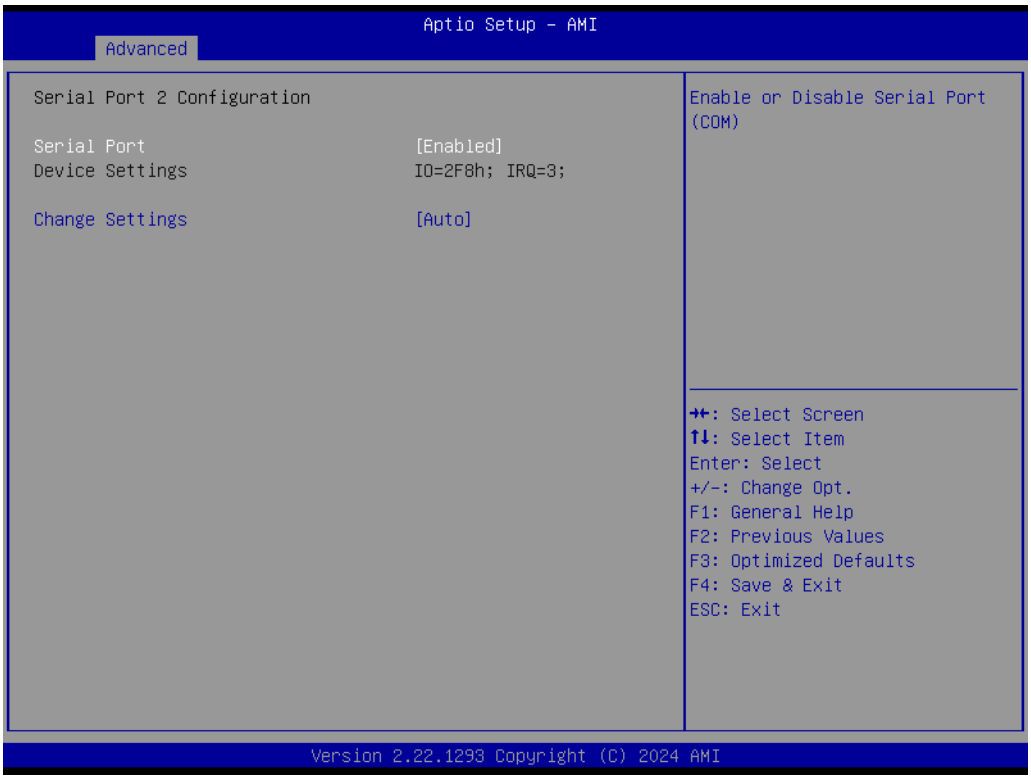


Figure 3.26 Serial Port 1 Configuration

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for Super IO Device.

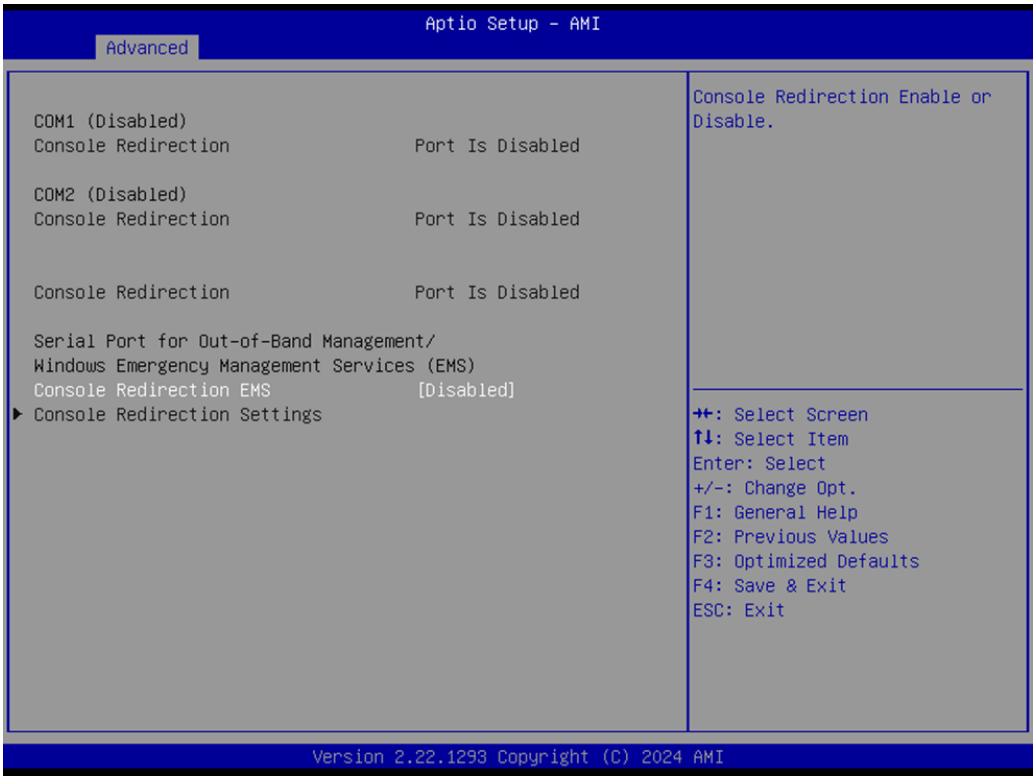


Figure 3.27 Serial Port Console Redirection

- **COM1 Console Redirection**
  Console Redirection Enable or Disable.
- **COM2 Console Redirection**
  Console Redirection Enable or Disable.
- **Console Redirection EMS**
  Console Redirection Enable or Disable.

Figure 3.28 Console Redirection Settings

3.4.12 PCI Subsystem Settings

3.4.12.1 ACPI Report Method Configuration

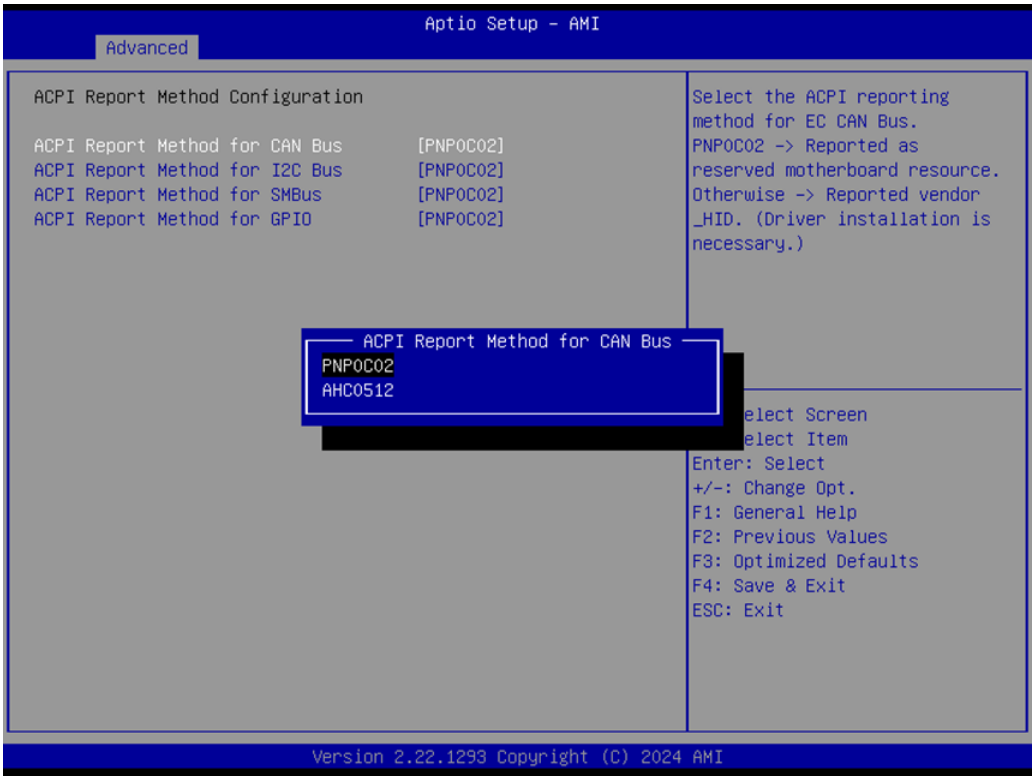


Figure 3.29 ACPI Report Method Configuration

- **ACPI Report Method for CAN Bus**
  Select the ACPI reporting method for EC CAN Bus. PNP0C02 -> Reported as reserved motherboard resource.
  Otherwise -> Reported vendor _HID. (Driver installation is necessary.)
- **ACPI Report Method for I2C Bus**
  Select the ACPI reporting method for EC I2C Bus. PNP0C02 -> Reported as reserved motherboard resource.
  Otherwise -> Reported vendor _HID. (Driver installation is necessary.)
- **ACPI Report Method for SMBus**
  Select the ACPI reporting method for EC SMBus. PNP0C02 -> Reported as reserved motherboard resource.
  Otherwise -> Reported vendor _HID. (Driver installation is necessary.)
- **ACPI Report Method for GPIO**
  Select the ACPI reporting method for EC GPIO.
  PNP0C02 -> Reported as reserved motherboard resource.
  Otherwise -> Reported vendor _HID. (Driver installation is necessary.)

3.4.13 USB Configuration

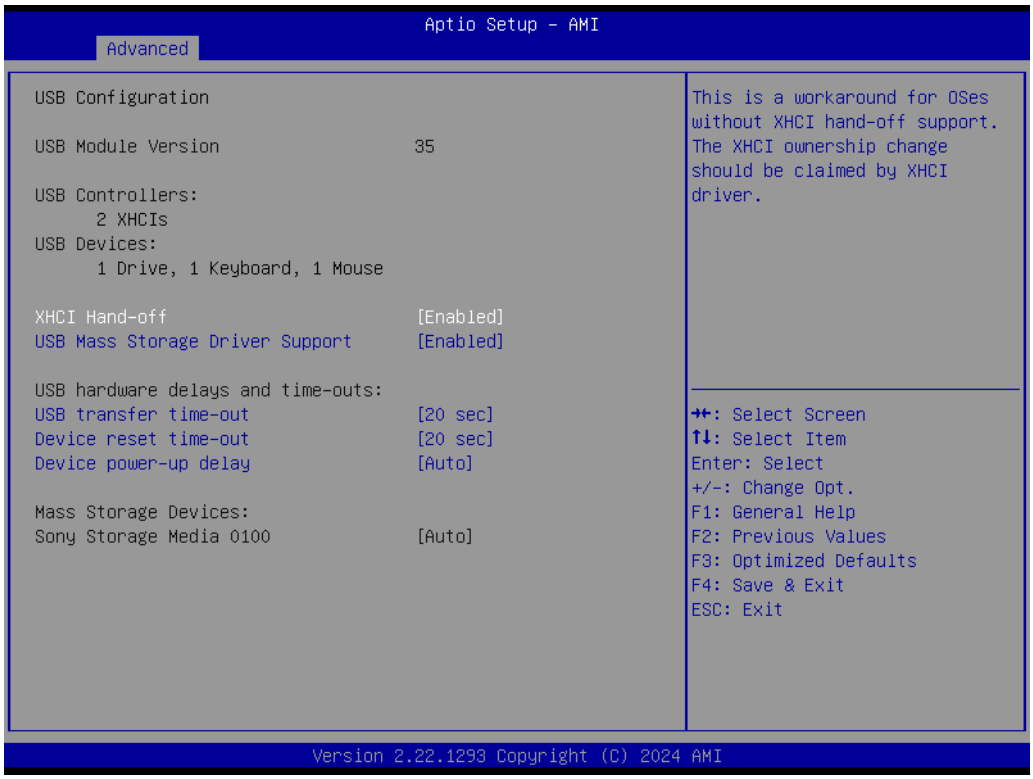


Figure 3.30 USB Configuration

- **XHCI Hand-off**
  This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
- **USB Mass Storage Driver Support**
  Enable/Disable USB Mass Storage Driver Support.
- **USB transfer time-out**
  The time-out value for Control, Bulk, and Interrupt transfers.

- **Device reset time-out**
  USB mass storage device Start Unit command time-out.
- **Device power-up delay**
  Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

3.4.14 Network Stack Configuration

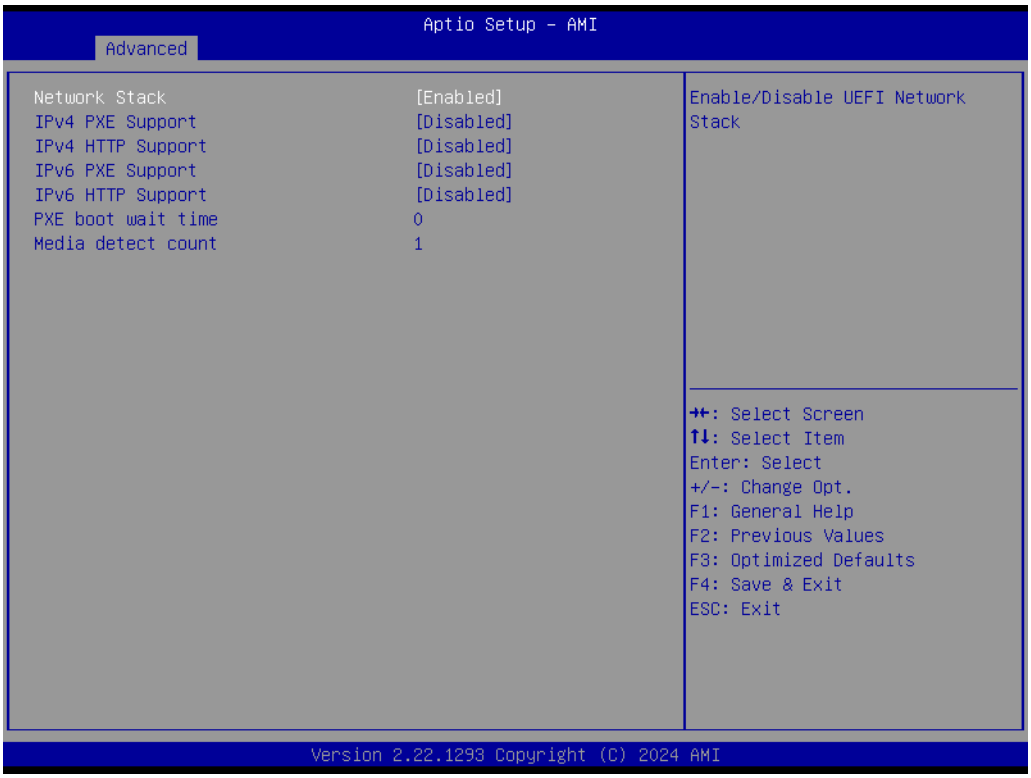


Figure 3.31 Network Stack Configuration

- **Network Stack**
  Enable/Disable UEFI Network Stack.
- **IPv4 PXE support**
  Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
- **IPv4 HTTP Support**
  Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
- **IPv6 PXE Support**
  Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
- **IPv6 HTTP Support**
  Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
- **PXE boot wait time**
  Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
- **Media detect count**

Number of times presence of media will be checked. Use either +/- or numeric keys to set the value.

3.4.15 NVMe Configuration

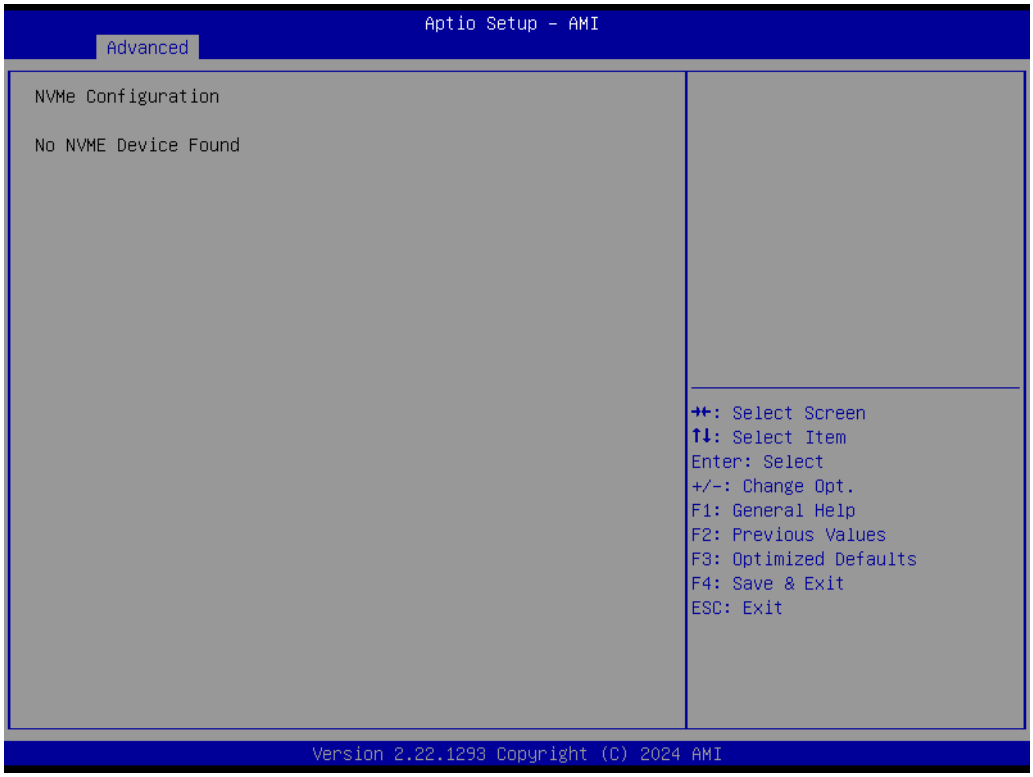


Figure 3.32 NVMe Configuration

3.4.16 Dual BIOS Configuration

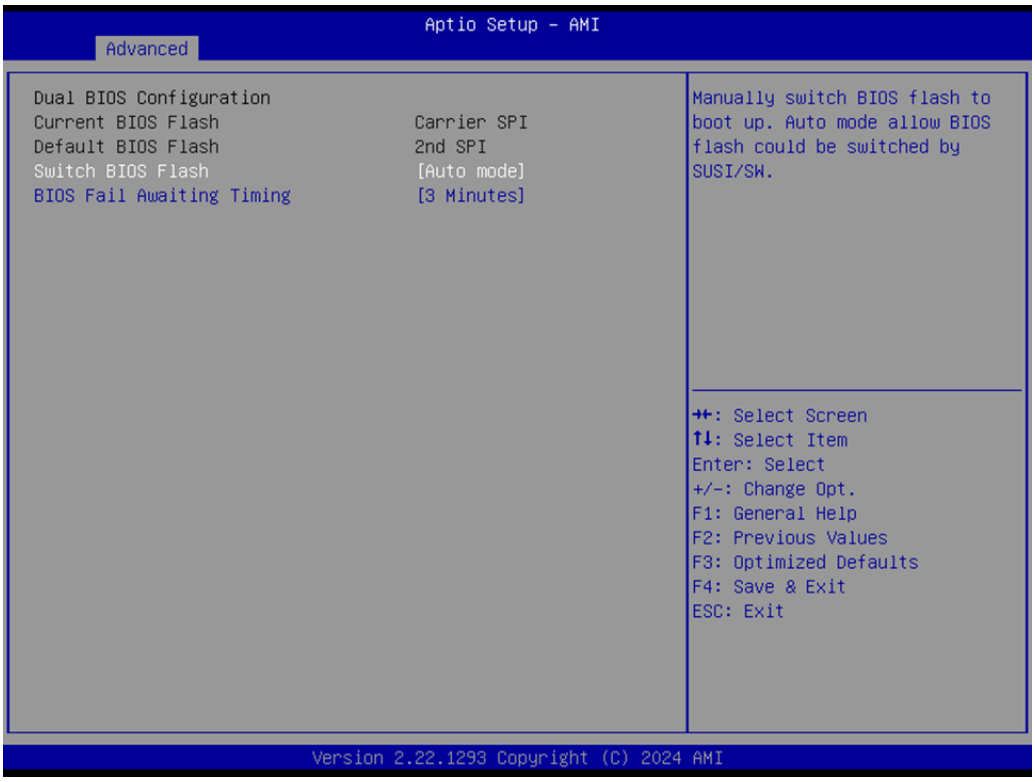


Figure 3.33 Dual BIOS Configuration

- **Switch BIOS Flash**
  Manually switch BIOS flash to boot up. Auto mode allow BIOS flash could be switched by SUSI/SW.
- **BIOS Fail Awaiting Timing**
  Determine specific timing to monitor if BIOS hadn't boot up successfully yet, then BIOS will be switched to another one.

3.4.17 Intel® Ethernet Controller I226-LMvP

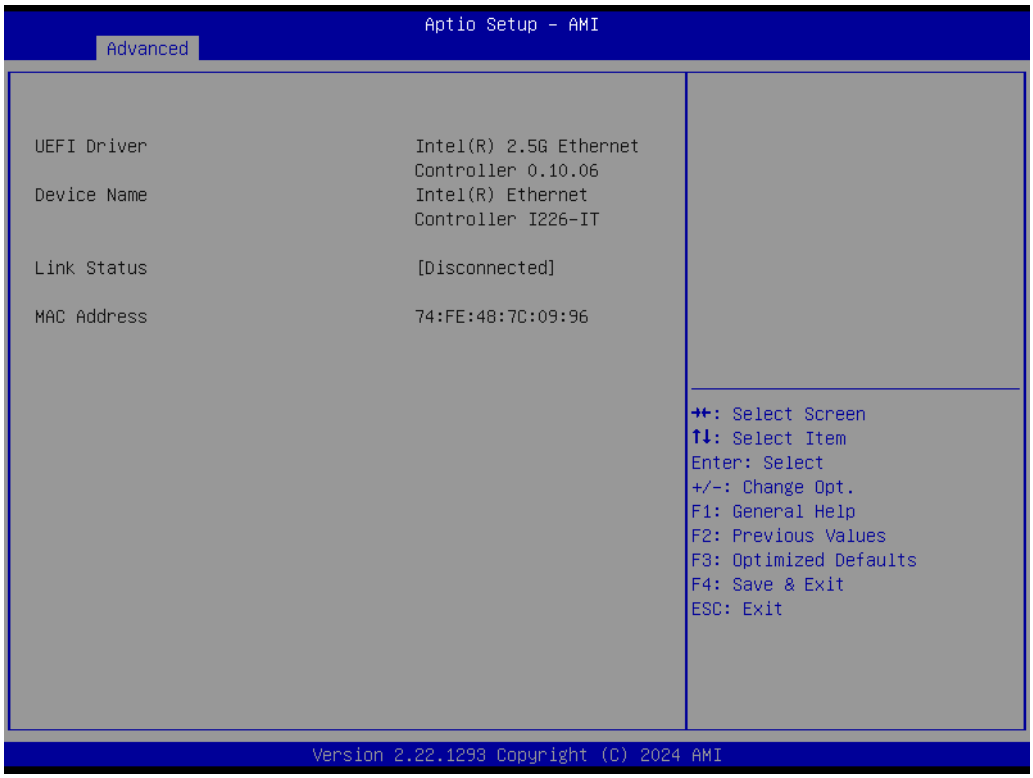


Figure 3.34 Intel® Ethernet Controller I226-LMvP

3.5 Chipset Setup

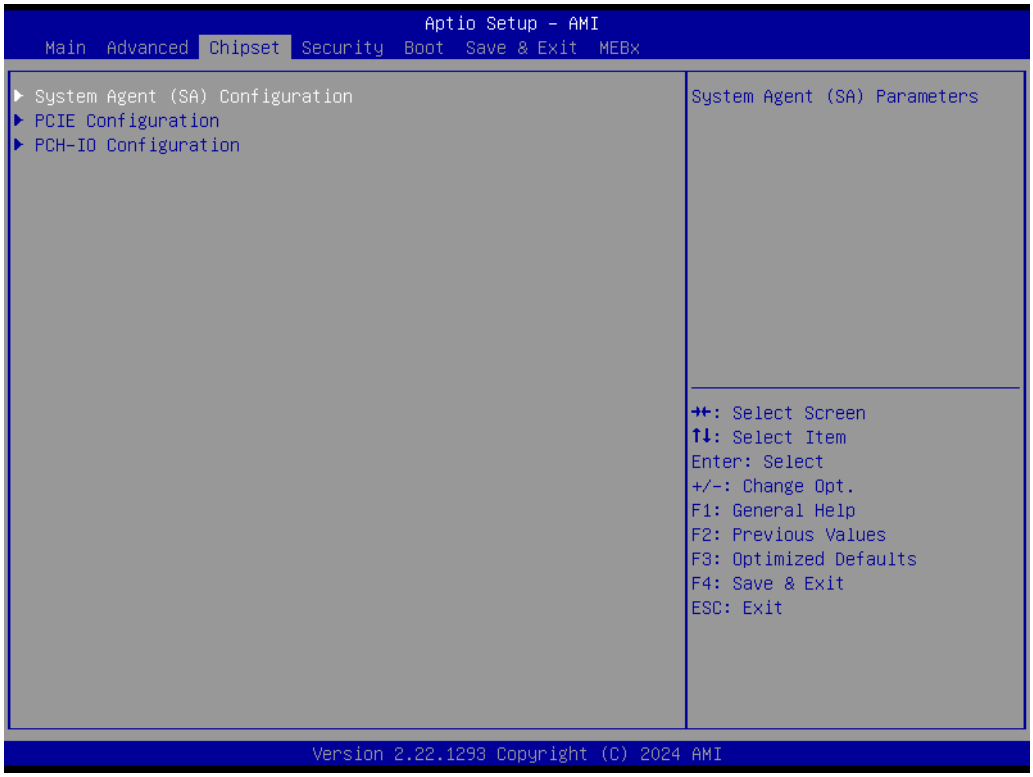


Figure 3.35 Chipset Setup

- **System Agent (SA)Configuration**
  System Agent Parameters
- **PCIE Configuration**
  PCIE Parameters.
- **PCH-IO Configuration**
  PCH Parameters.

3.5.1 System Agent (SA) Configuration

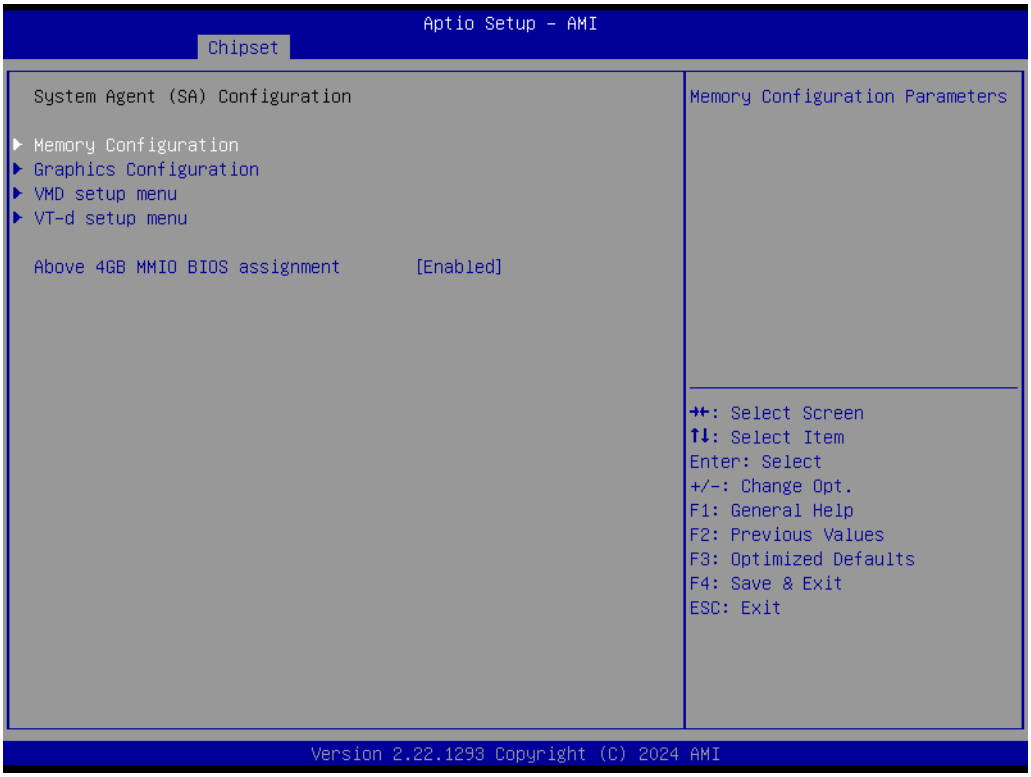


Figure 3.36 System Agent (SA) Configuration

- **Memory Configuration**
  Memory Configuration Parameters.
- **Graphic Configuration**
- **VMD setup menu**
  VMD Configuration.
- **VT-d**
  VT-d capability.
- **Above 4GB MMIO BIOS assignment**
  Enable/Disable above 4GB memory mapped IO BIOS assignment. This is enabled automatically when aperture size is set to 2048MB.

3.5.1.1 Memory Configuration

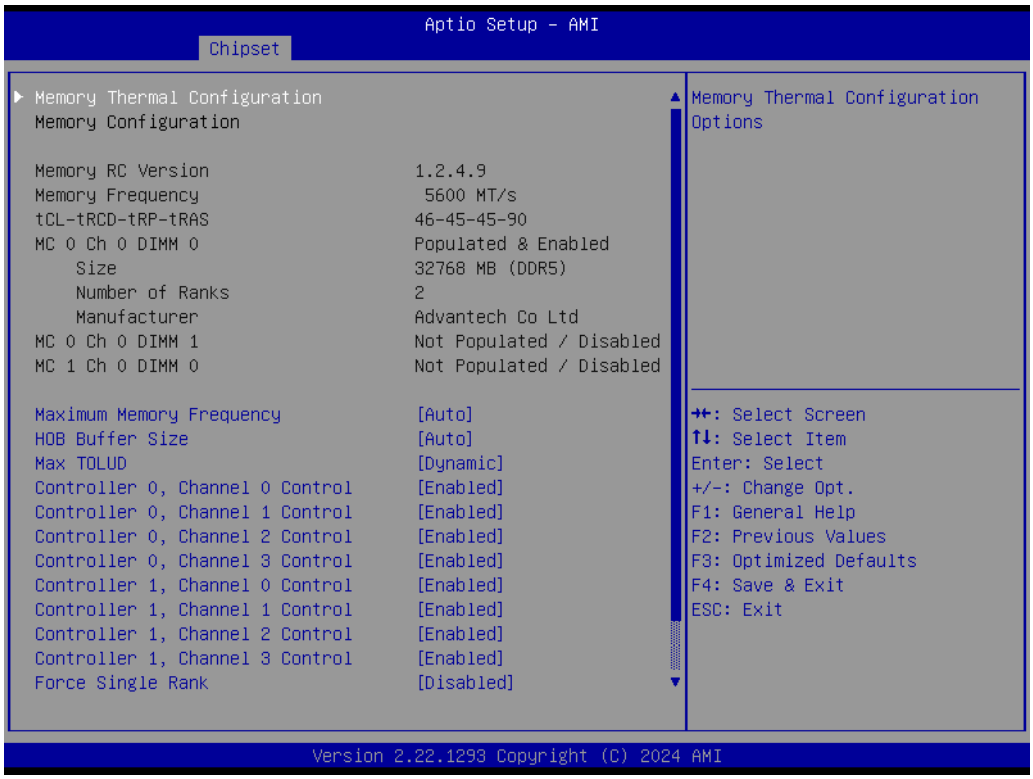


Figure 3.37 Memory Configuration

- **Maximum Memory Frequency**
  Maximum Memory Frequency Selections in Mhz.
- **HOB Buffer Size**
  Size to set HOB Buffer.
- **Max TOLUD**
  Maximum value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on the largest MMIO length of installed graphic controller.
- **Fast Boot**
  Enable/Disable fast path thru the MRC.

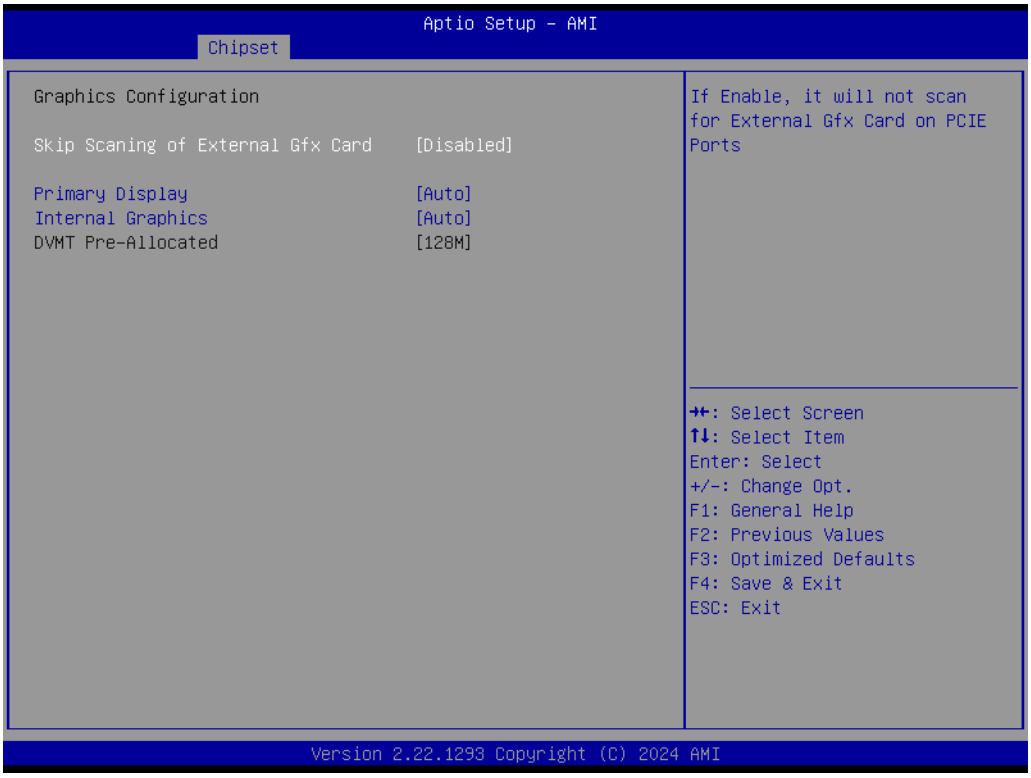


Figure 3.38 Graphics Configuration

- **Skip Scaning of External Gfx Card**
  If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports.
- **Primary Display**
  Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select HG for Hybrid Gfx.
- **Internal Graphics**
  Keep IGFX enabled base on the setup options.
- **DVMT Pre-Allocated**
  Select DVMT5.0 pre-allocated(fixed) Graphics Memory size is used by the internal graphics device.

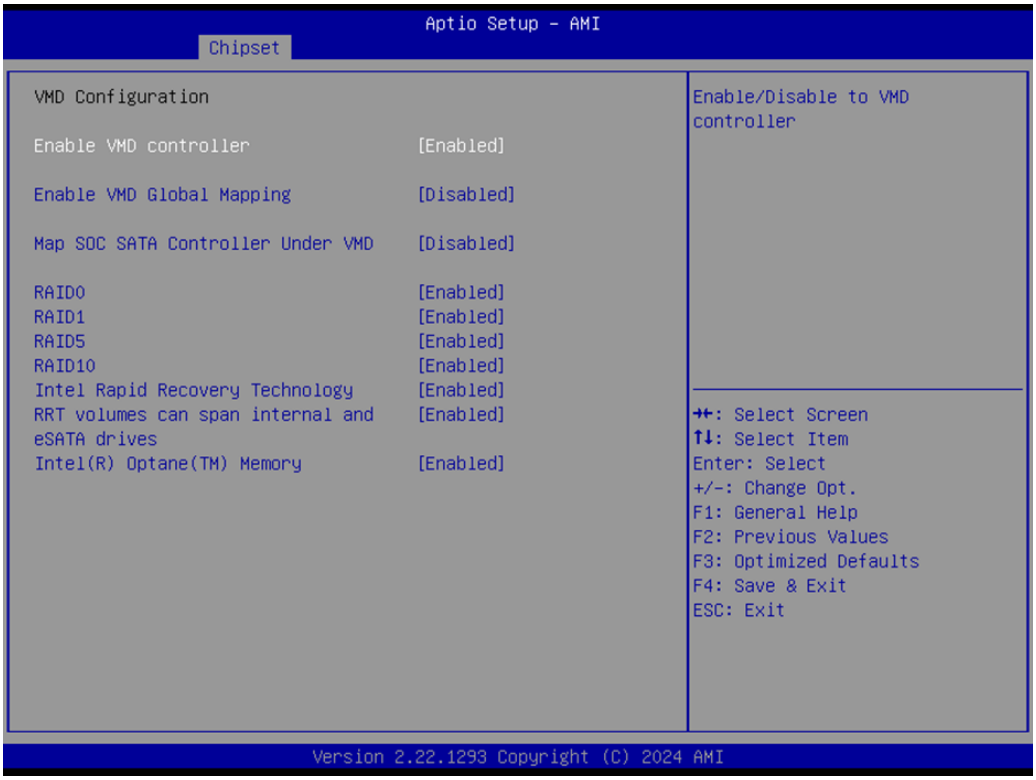


Figure 3.39 VMD Setup Menu

- **Enable VMD controller**
  Enable/Disable to VMD controller.
- **Enable VMD Global Mapping**
  Enable/Disable to VMD Global Mapping.
- **Map SOC SATA Controller Under VMD**
- **RAID0**
  Enable/Disable RAID0 feature.
- **RAID1**
  Enable/Disable RAID1 feature.
- **RAID5**
  Enable/Disable RAID5 feature.
- **RAID10**
  Enable/Disable RAID10 feature.
- **Intel Rapid Recovery Technology RRT volumes can span internal and eSATA drivers**
- **Intel(R) Optane(TM) Memory**
  Enable/Disable System Acceleration with Intel(R) Optane(TM) Memory feature.

3.5.2 PCI Express Configuration

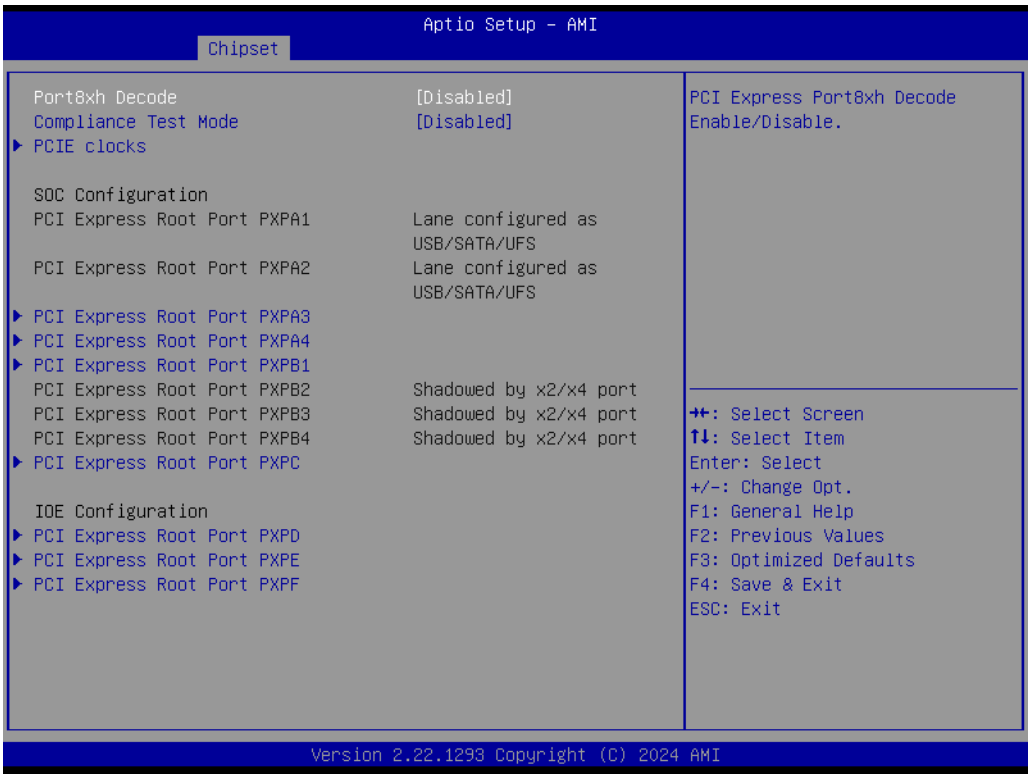


Figure 3.40 PCI Express Configuration

- **PCIE Power Gating**
  PCIe Express Power Gating Enable/Disable for all port.
- **PCI Express Root Port PXPA3**
- **PCI Express Root Port PXPA4**
- **PCI Express Root Port PXPB1**
- **PCI Express Root Port PXPC**
- **PCI Express Root Port PXPD**
- **PCI Express Root Port PXPE**
- **PCI Express Root Port PXPF**

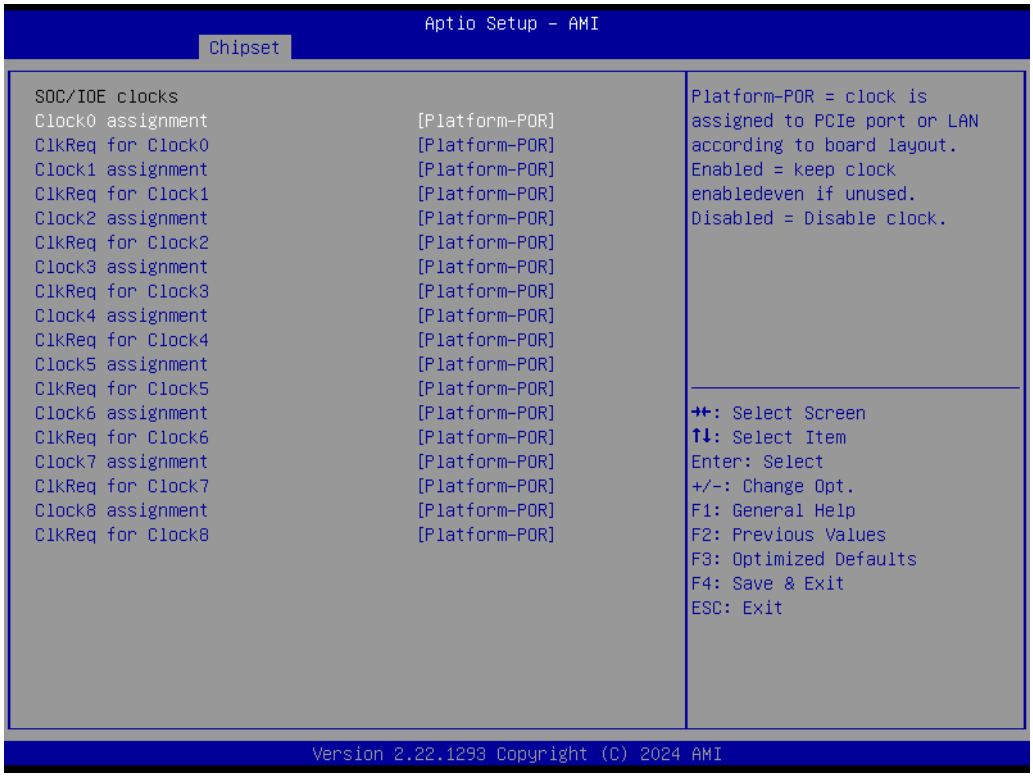


Figure 3.41 PCIE clocks

- **Clock0 assignment**
  Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled=keep clock enabled even if unused. Disabled=Disable clock.
- **ClkReq for Clock0**
  Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used
- **Clock1 assignment**
  Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled=keep clock enabled even if unused. Disabled=Disable clock.
- **ClkReq for Clock1**
  Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used
- **Clock2 assignment**
  Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled=keep clock enabled even if unused. Disabled=Disable clock.
- **ClkReq for Clock2**
  Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used
- **Clock3 assignment**
  Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled=keep clock enabled even if unused. Disabled=Disable clock.
- **ClkReq for Clock3**
  Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used
- **Clock4 assignment**

Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled=keep clock enabled even if unused. Disabled=Disable clock.

- **ClkReq for Clock4**

  Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used

- **Clock5 assignment**

  Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled=keep clock enabled even if unused. Disabled=Disable clock.

- **ClkReq for Clock5**

  Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used

- **Clock6 assignment**

  Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled=keep clock enabled even if unused. Disabled=Disable clock.

- **ClkReq for Clock6**

  Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used

- **Clock7 assignment**

  Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled=keep clock enabled even if unused. Disabled=Disable clock.

- **ClkReq for Clock7**

  Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used

- **Clock8 assignment**

  Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled=keep clock enabled even if unused. Disabled=Disable clock.

- **ClkReq for Clock8**

  Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.

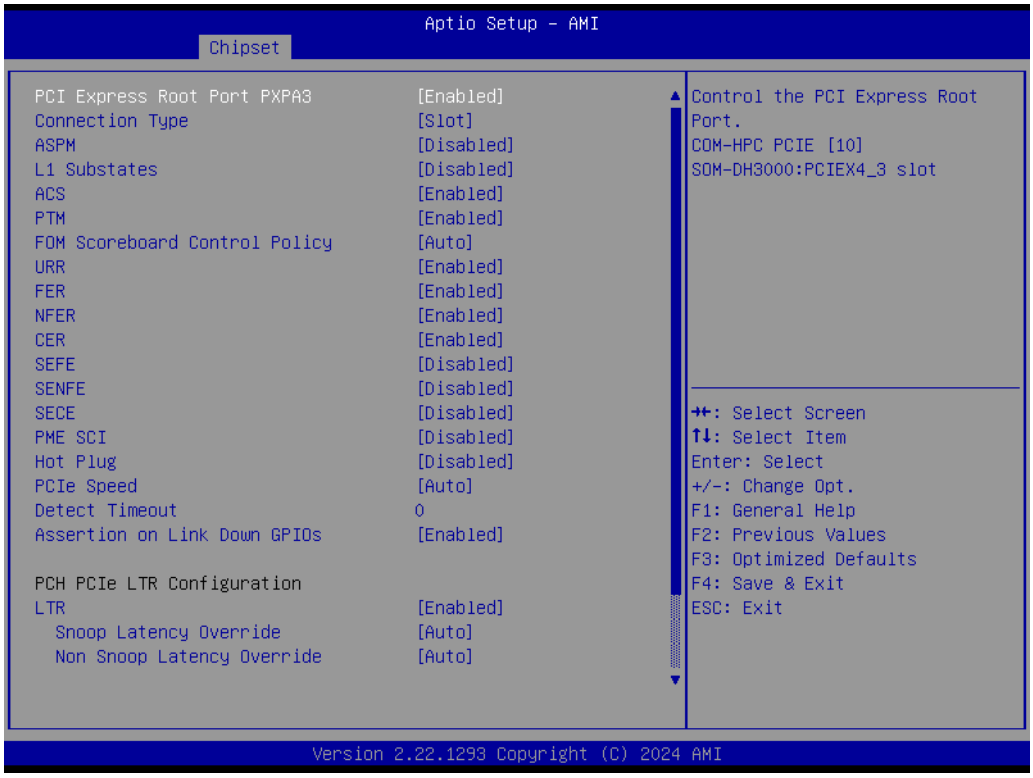
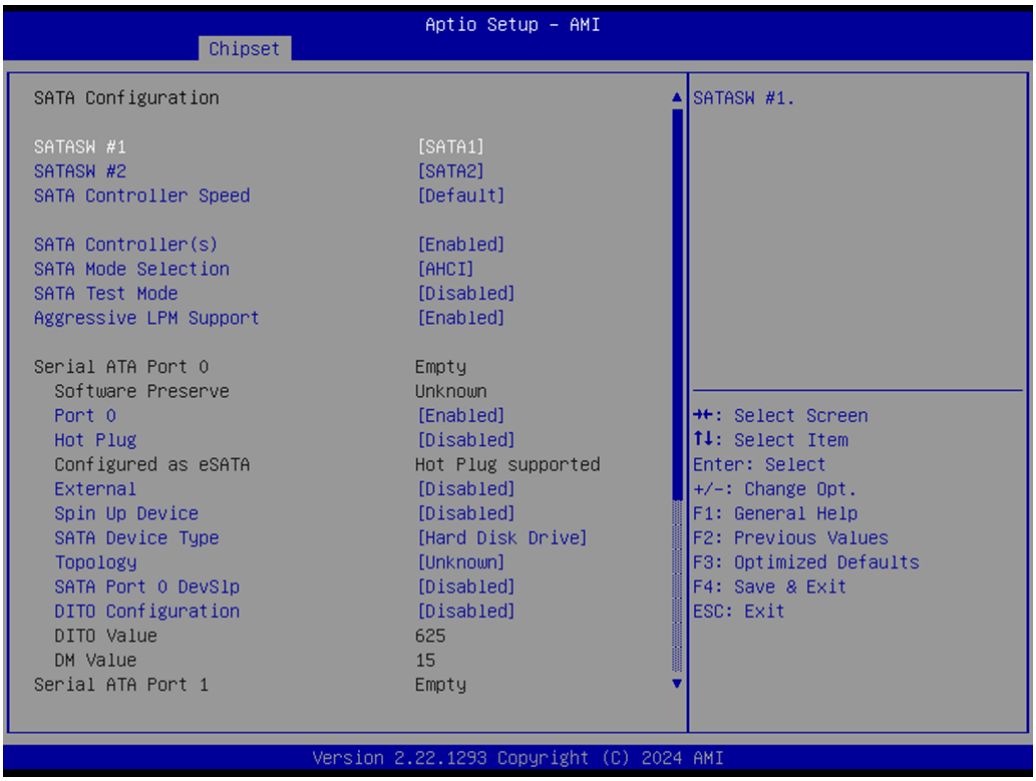


Figure 3.42 PCIE Root Port

- **PCI Express Root Port PXPA3**
  Control the PCI Express Root Port.

3.5.2.1 SATA Configuratioin



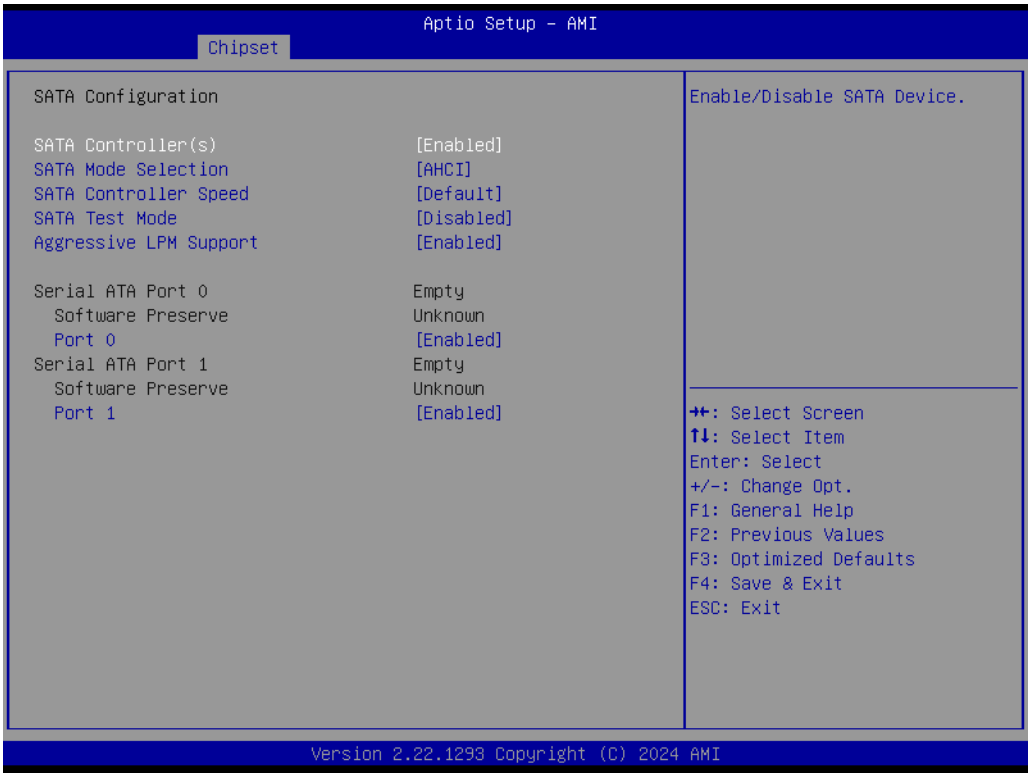


Figure 3.43 SATA Drives

- **SATA Controller(s)**
  Enable/Disable SATA Device.
- **SATA Mode Selection**
  Determines how SATA controller(s) operate.
- **SATA Test Mode**
  Test Mode Enable/Disable (Loop Back).
- **Aggressive LPM Support**
  Enable PCH to aggressively enter link power state.
- **SATA Controller Speed**
  Indicates the maximum speed the SATA controller can support.
- **Port 0**
  Enable or Disable SATA Port.
- **Port 1**
  Enable or Disable SATA Port.

3.5.2.2 USB Configuration

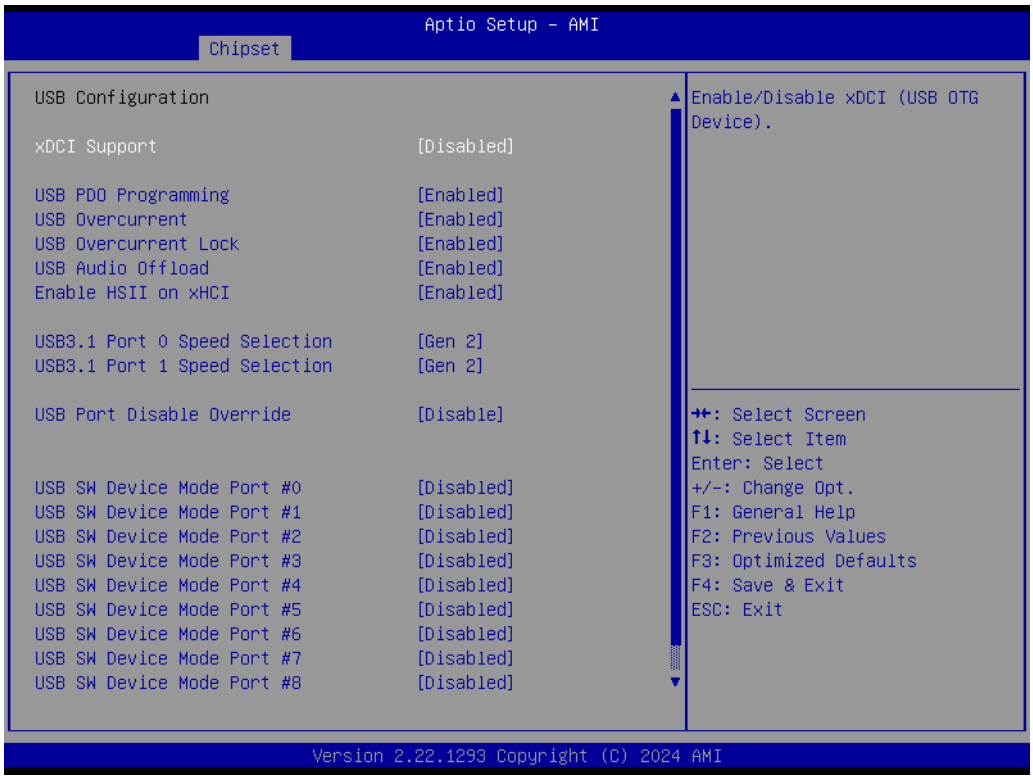


Figure 3.44 USB Configuration

- **xDCI Support**
  Enable/Disable xDCI (US OTG Device).
- **USB PD0 Programming**
  Select ‘Enable’ if Port Disable Override functionality is used.
- **USB Overcurrent**
  Select ‘Disabled’ for pin-based debug. If pin-based debug is enabled bit USB overcurrent is not disabled, USB Dbc does not work.
- **USB Overcurrent Lock**
  Select ‘Enabled’ if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping data.
- **USB Audio offload**
  Enable/Disable USB Audio Offlaid functionality.
- **Enable HSII on xHCI**
  Enable/Disable HSII feature. It may lead to increased power consumption.
- **USB3.1 Port 0 Speed Selection**
  USB3.1 Speed selection; Gen1 or Gen2.
- **USB3.1 Port 1 Speed Selection**
  USB3.1 Speed selection; Gen1 or Gen2.
- **USB Port Disable Override**
  Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller
- **USB SW Device Mode Port #0**
  Enable Connector Event for device subscription.
- **USB SW Device Mode Port #1**

Enable Connector Event for device subscription.

- **USB SW Device Mode Port #2**
  Enable Connector Event for device subscription.
- **USB SW Device Mode Port #3**
  Enable Connector Event for device subscription.
- **USB SW Device Mode Port #4**
  Enable Connector Event for device subscription.
- **USB SW Device Mode Port #5**
  Enable Connector Event for device subscription.
- **USB SW Device Mode Port #6**
  Enable Connector Event for device subscription.
- **USB SW Device Mode Port #7**
  Enable Connector Event for device subscription.
- **USB SW Device Mode Port #8**
  Enable Connector Event for device subscription.
- **USB SW Device Mode Port #9**
  Enable Connector Event for device subscription.

3.5.2.3 Security Configuration

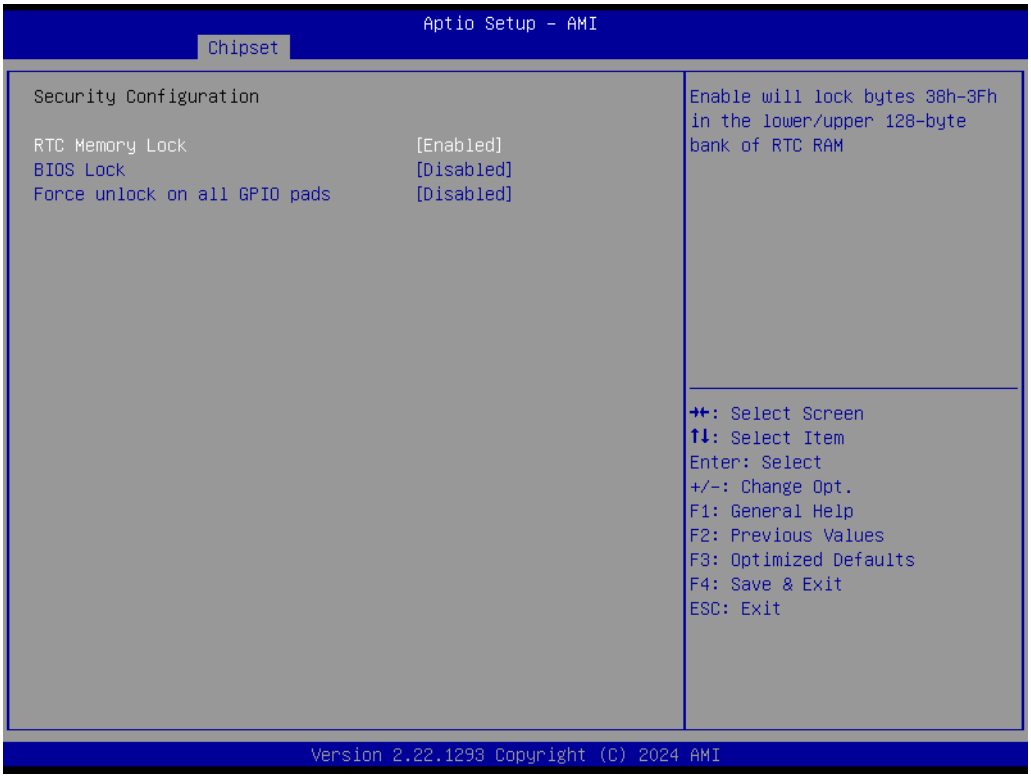


Figure 3.45 Security Configuration

- **RTC Memory Lock**
  Enable will lock bytes 38h-3Fh in the lower/upper 126 –byte bank of RTC RAM.
- **BIOS Lock**
  Enable/Disable the PCH BIOS lock enable feature. Required to be enabled to ensure SMM protection of flash.
- **Force unlock on all GPIO pads**

If Enabled BIOS will force all GPIO pads to be in unlocked state.

3.5.2.4 HD Audio Subsystem Configuration Settings

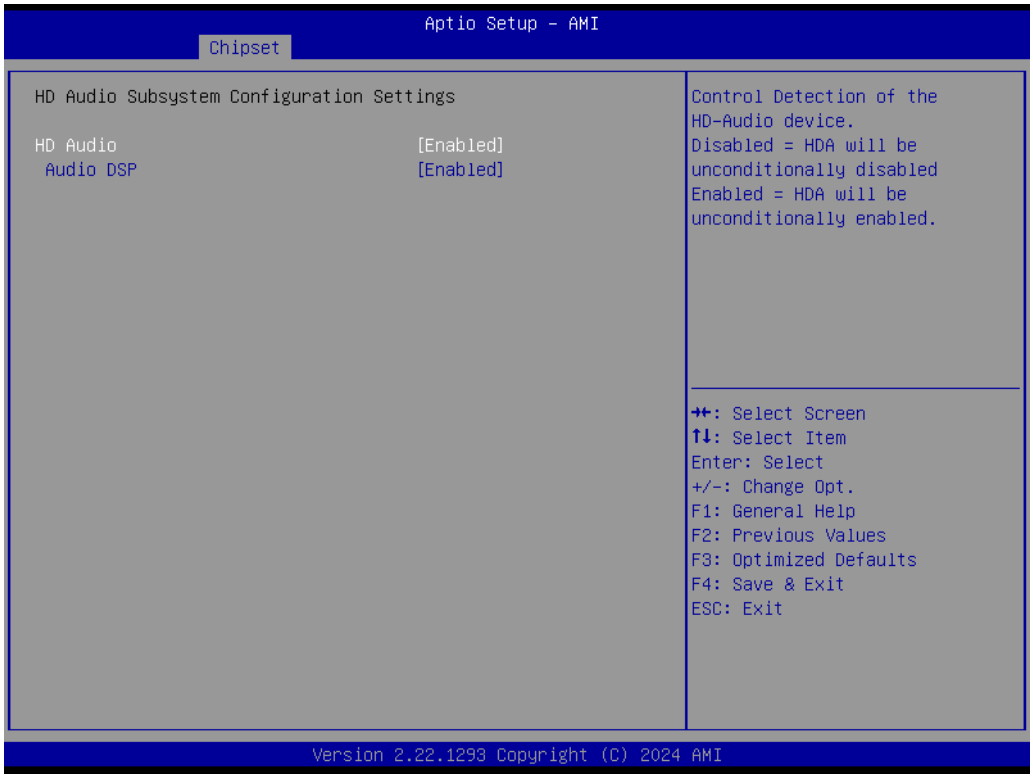


Figure 3.46 HD Audio Subsystem Configuration Settings

- **HD Audio**
  Control Detection of the HD-Audio device. Disabled=HDA will be unconditionally disabled. Enabled=HDA will be unconditionally enabled.
- **Audio DSP**
  Enable/Disable Audio DSP.

3.5.3 PCH-IO Configuration

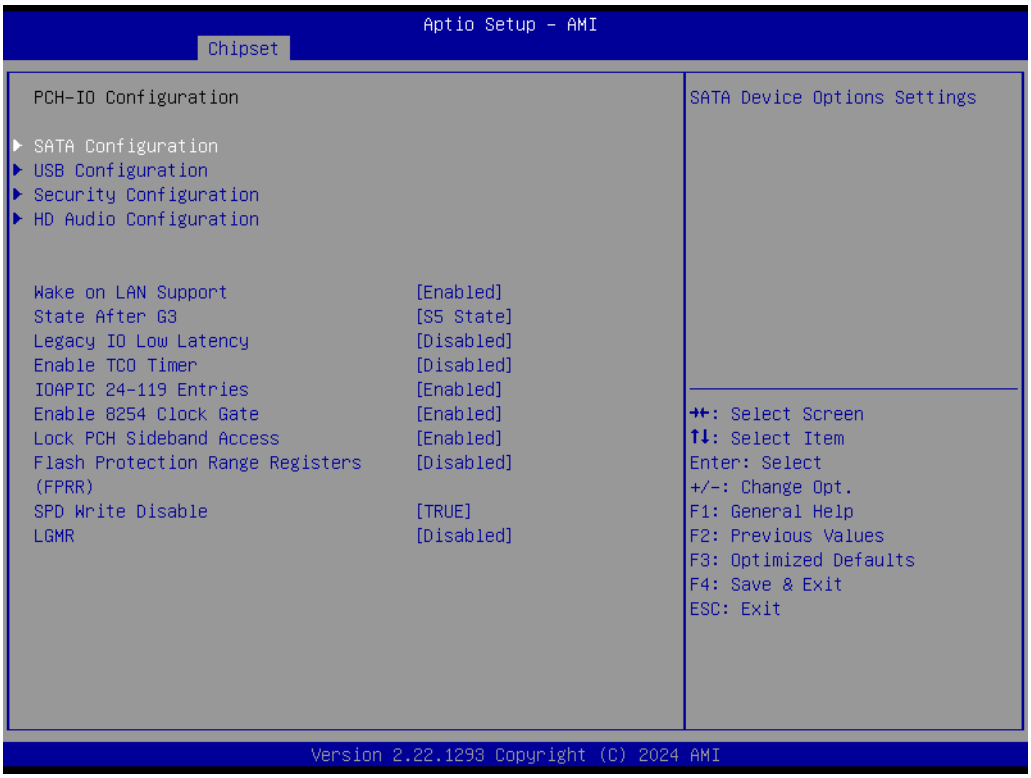


Figure 3.47 PCH-IO Configuration

- **SATA Configuration**
  SATA device option settings.
- **USB Configuration**
  USB Configuration settings.
- **Security Configuration**
  Security Configuration settings.
- **HD Audio Configuration**
  HD audio subsystem configuration settings.
- **Wake on LAN Support**
  Seriallo configuration settings.
- **State After G3**
  Specify what state to go to when power is re-applied after a power failure (G3 state).
- **Legacy IO Low Latency**
- **Enable TC0 Timer**
  PCIe Ref.5%.
- **I0APIC 24-119 Entries**
- **Enable 8254 Clock Gate**
- **Lock PCH Sideband Access**
- **Flash Protection Range Registers(FPRR)**
- **SPD Write Disable**
  Enable/Disable setting SPD Write Disable. For security recommendations, SPD write disable bit must be set.
- **LGMR**

3.6 Security Chipset

Figure 3.48 Security Chipset

- **Administrator Password**
  Set Setup Administrator Password.
- **User Password**
  Set User Password.
- **Secure Boot**
  Secure Boot Configuration.

3.6.1 Secure Boot

Figure 3.49 Secure Boot

- **Secure Boot**

  Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset.

- **Secure Boot Mode**

  Secure Boot mode options:

  Standard or Custom.

  In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.

3.6.2 Boot Setup

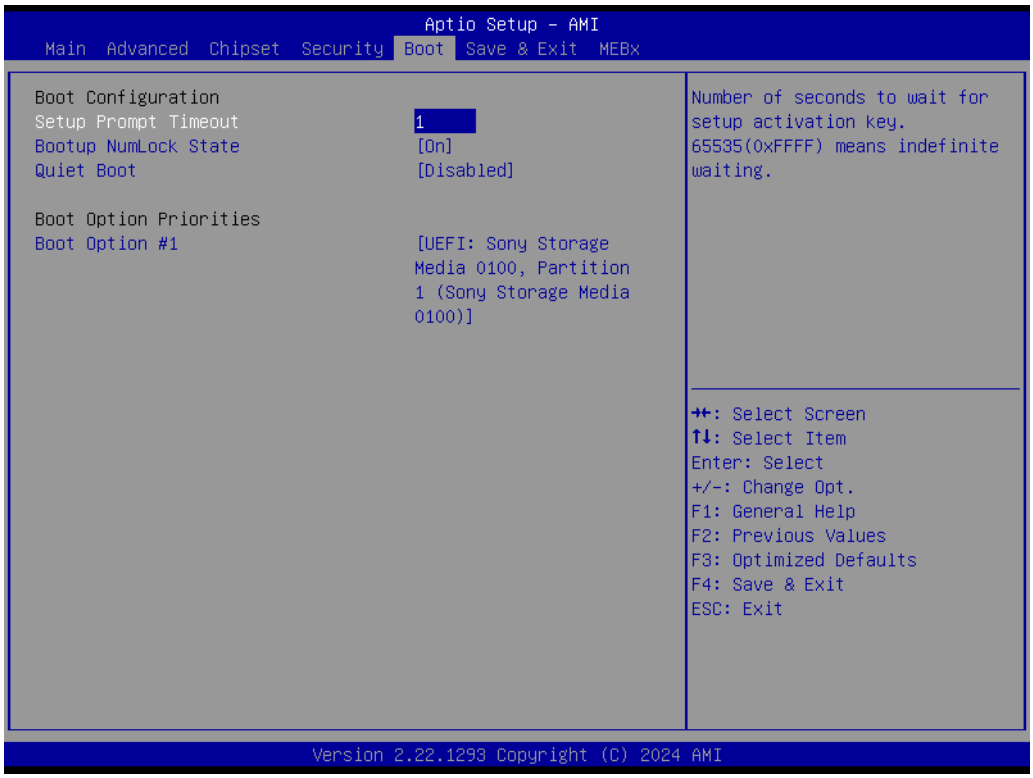


Figure 3.50 Boot Setup

- **Setup Prompt Timeout**
  Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
- **Bootup NumLock State**
  Select the keyboard NumLock state.
- **Quiet Boot**
  Enables or disables Quiet Boot option.
- **Boot Option #1**
  Sets the system boot order.

3.7 Save & Exit

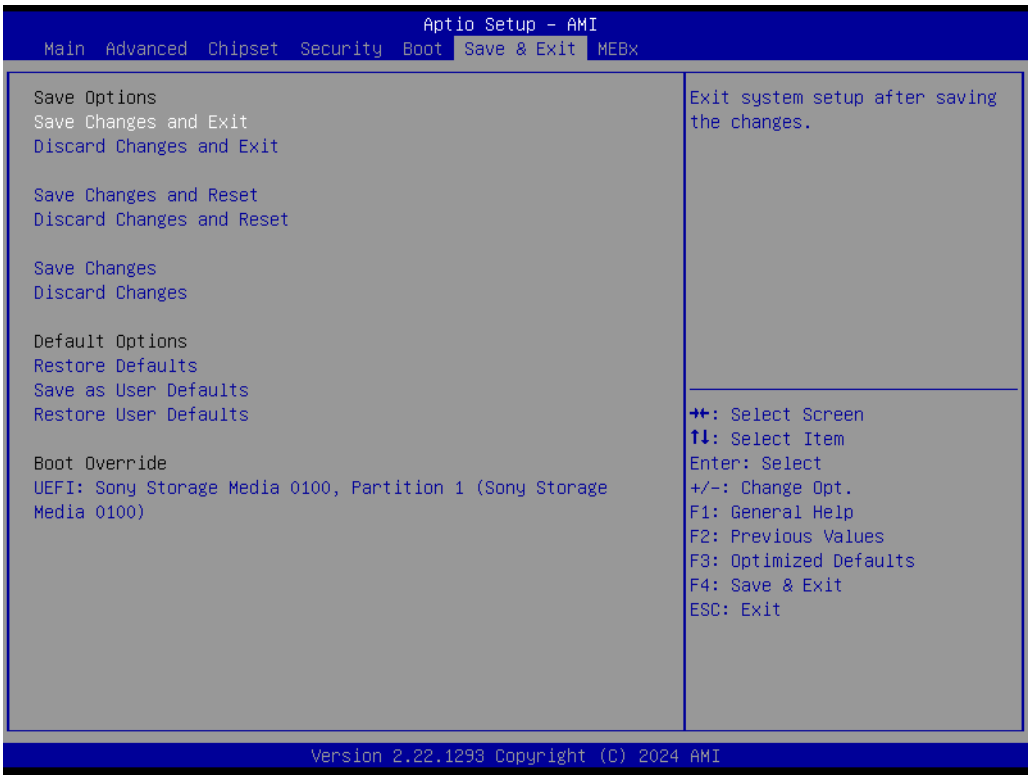


Figure 3.51 Save & Exit

- **Save Changes and Exit**
  Exit system setup after saving the changes.
- **Discard Changes and Exit**
  Exit system setup without saving any changes.
- **Save Changes and Reset**
  Reset the system after saving the changes.
- **Discard Changes and Reset**
  Reset system setup without saving any changes.
- **Save Changes**
  Save Changes done so far to any of the setup options.
- **Discard Changes**
  (005B) Discard Changes done so far to any of the setup options.
- **Restore Defaults**
  Restore/Load Default values for all the setup options.
- **Save as User Defaults**
  Save the changes done so far as User Defaults.
- **Restore User Defaults**
  Restore the User Defaults to all the setup options.
- **Boot Override**

3.8 MEBx

Figure 3.52 MEBx

Chapter 4

S/W Introduction & Installation

Sections include:

- S/W Introduction
- Driver Installation
- Advantech iManager

4.1 S/W Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft Windows embedded technology". We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (Hardware suppliers, System integrators, Embedded OS distributors) for projects. Our goal is to make Windows Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Driver Installation

The Intel Chipset Software Installation (CSI) utility installs the Windows INF files that explain how chipset components are configured to the operating system.

4.2.1 Windows Driver Setup

To install the drivers on a windows-based operation system, please connect to internet and browse the website http://support.advantech.com.tw. Next, download the drivers that you want to install. Then follow the Driver Setup instructions to complete the installation.

4.2.2 Other OS

Linux Ubuntu

4.3 Advantech iManager

Advantech's platforms come equipped with iManager, a micro controller that provides embedded features for system integrators. Embedded features have been moved from the OS/BIOS level to the board level, to increase reliability and simplify integration. iManager runs whether the operating system is running or not; it can count the boot times and running hours of the device, monitor device health, and provide an advanced watchdog to handle errors just as they happen. iManager also comes with a secure & encrypted EEPROM for storing important security key or other customer define information. All the embedded functions are configured through API and provide corresponding utilities to demonstrate. These APIs comply with PICMG EAPI (Embedded Application Programmable Interface) specification and unify in the same structures. It makes these embedded features easier to integrate, speed up developing schedule, and provide the customer's software continuity while upgrade hardware. More detail of how to use the APIs and utilities, please refer to Advantech iManager2.0 Software API User Manual.

4.3.1 Control

GPIO

General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off the device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

SMBus

SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface a embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

PC

PC is a bi-directional two wire bus that was developed by Phillips for use in their televisions in the 1980s.The PC API allows a developer to interface with an embedded system environment and transfer serial messages using the PC protocols, allowing multiple simultaneous device contol.

4.3.1.1 Display

Brightness Control

The Brightness Control API allows a developer to access embedded devices and easily control brightness.

Backlight

The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

4.3.1.2 Monitor

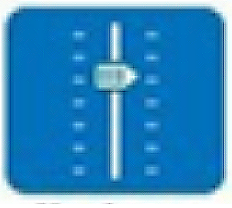
Watchdog

A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

Hardware Monitor

The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.

Hardware Control



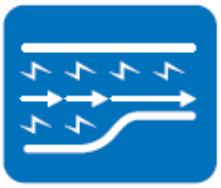
The Hardware Control API allows developers to set the PWM (Pulse Width Modulation) value to adjust fan speed or other devices. It can also be used to adjust the LCD brightness.

4.3.1.3 Power Saving

CPU Speed

Makes use of Intel SpeedStep technology to save power consumption. The system will automatically adjust the CPU speed depending on the system loading.

System Throttling



Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

Appendix A

Pin Assignment

This appendix gives you the information about the hardware pin assignment of the SOM-A350 CPU System on Module.
Sections include:

- SOM-A350 Type 6 Pin Assignment

A.1 SOM-A350 Pin Assignment

This section provides the pin assignment for SOM-A350 on the COM HPC connector, in accordance with the COM-HPC Revision 1.2 Client Type pin-out definitions. For comprehensive information on how to utilize these pins, and to access design guidance, checklists, reference schematics, and additional hardware/software support, please reach out to Advantech for more details.

Table A.1: J1 Connector Rows A and B

Pin#	Row A Description	SOM-A350 Difference	Pin#	Row B Description	SOM-A350 Difference
J1.A1	VCC		J1.B1	VCC	
J1.A2	VCC		J1.B2	PWRBTN#	
J1.A3	VCC		J1.B3	VCC	
J1.A4	VCC		J1.B4	THERMTRIP#	
J1.A5	VCC		J1.B5	VCC	
J1.A6	VCC		J1.B6	TAMPER#	
J1.A7	VCC		J1.B7	VCC	
J1.A8	VCC		J1.B8	SUS_S3#	
J1.A9	VCC		J1.B9	VCC	
J1.A10	GND		J1.B10	WD_STROBE#	
J1.A11	BATLOW#		J1.B11	WD_OUT	
J1.A12	PLTRST#		J1.B12	GND	
J1.A13	GND		J1.B13	USB5-	
J1.A14	USB7-		J1.B14	USB5+	
J1.A15	USB7+		J1.B15	GND	
J1.A16	GND		J1.B16	USB4-	
J1.A17	USB6-		J1.B17	USB4+	
J1.A18	USB6+		J1.B18	GND	
J1.A20	DDI1_SDA_AUX-		J1.B20	I2S_DOUT / SNDW_-DAT3 / HDA_SDO	
J1.A21	DDI1_SCL_AUX+		J1.B21	I2S_MCLK / HDA_RST	
J1.A22	GND		J1.B22	I2S_DIN / SNDW_-DAT2 / HDA_SDI	
J1.A23	DDI1_PAIR0-		J1.B23	I2S_CLK / SNDW_-CLK2 / HDA_BCLK	
J1.A24	DDI1_PAIR0+		J1.B24	VCC_5V_SBY	
J1.A25	GND		J1.B25	USB67_OC#	
J1.A26	DDI1_PAIR1-		J1.B26	USB45_OC#	
J1.A27	DDI1_PAIR1+		J1.B27	USB23_OC#	
J1.A28	GND		J1.B28	USB01_OC#	
J1.A29	DDI1_PAIR2-		J1.B29	SML1_CLK	
J1.A30	DDI1_PAIR2+		J1.B30	SML1_DAT	
J1.A31	GND		J1.B31	PMCALERT#	
J1.A32	DDI1_PAIR3-		J1.B32	SML0_CLK	
J1.A33	DDI1_PAIR3+		J1.B33	SML0_DAT	

Table A.2: J1 Connector Rows A and B					
Pin#	**Row A Description**	**SOM-A350 Difference**	**Pin#**	**Row B Description**	**SOM-A350 Difference**
J1.A34	GND		J1.B34	USB_PD_ALERT#	
J1.A35	eDP_AUX- / DSI_TX0-		J1.B35	USB_PD_I2C_CLK	
J1.A36	eDP_AUX+ / DSI_TX0+		J1.B36	USB_PD_I2C_DAT	
J1.A37	GND		J1.B37	USB_RT_ENA	
J1.A38	eDP_TX0- / DSI_TX1-		J1.B38	USB1_LSRX	NA
J1.A39	eDP_TX0+ / DSI_TX1+		J1.B39	USB1_LSTX	NA
J1.A40	GND		J1.B40	USB0_LSRX	NA
J1.A41	eDP_TX1- / DSI_TX2-		J1.B41	USB0_LSTX	NA
J1.A42	eDP_TX1+ / DSI_TX2+		J1.B42	GND	
J1.A43	GND		J1.B43	USB0_AUX-	NA
J1.A44	eDP_TX2- / DSI_CLK-		J1.B44	USB0_AUX+	NA
J1.A45	eDP_TX2+ / DSI_CLK+		J1.B45	LID#	
J1.A46	GND		J1.B46	SLEEP#	
J1.A47	eDP_TX3- / DSI_TX3-		J1.B47	VCC_BOOT_SPI	
J1.A48	eDP_TX3+ / DSI_TX3+		J1.B48	BOOT_SPI_CS#	
J1.A49	GND		J1.B49	BSEL0	
J1.A50	eSPI_IO0		J1.B50	BSEL1	
J1.A51	eSPI_IO1		J1.B51	BSEL2	
J1.A52	eSPI_IO2		J1.B52	eSPI_ALERT0#	
J1.A53	eSPI_IO3		J1.B53	eSPI_ALERT1#	
J1.A54	eSPI_CLK		J1.B54	eSPI_CS0#	
J1.A55	GND		J1.B55	eSPI_CS1#	
J1.A56	PCIe_CLKREQ0_LO#		J1.B56	eSPI_RST#	
J1.A57	PCIe_CLKREQ0_HI#		J1.B57	GND	
J1.A58	GND		J1.B58	PCIe_BMC_RX-	NA
J1.A59	PCIe_BMC_TX-	NA	J1.B59	PCIe_BMC_RX+	NA
J1.A60	PCIe_BMC_TX+	NA	J1.B60	GND	
J1.A61	GND		J1.B61	PCIe08_RX-	
J1.A62	PCIe08_TX-		J1.B62	PCIe08_RX+	
J1.A63	PCIe08_TX+		J1.B63	GND	
J1.A64	GND		J1.B64	PCIe09_RX-	
J1.A65	PCIe09_TX-		J1.B65	PCIe09_RX+	
J1.A66	PCIe09_TX+		J1.B66	GND	
J1.A67	GND		J1.B67	PCIe10_RX-	
J1.A68	PCIe010_TX-		J1.B68	PCIe10_RX+	
J1.A69	PCIe010_TX+		J1.B69	GND	
J1.A70	GND		J1.B70	PCIe11_RX-	

Table A.3: J1 Connector Rows A and B					
Pin#	**Row A Description**	**SOM-A350 Difference**	**Pin#**	**Row B Description**	**SOM-A350 Difference**
J1.A71	PCIe11_TX-		J1.B71	PCIe11_RX+	
J1.A72	PCIe11_TX+		J1.B72	GND	
J1.A73	GND		J1.B73	PCIe12_RX-	NA
J1.A74	PCIe12_TX-	NA	J1.B74	PCIe12_RX+	NA
J1.A75	PCIe12_TX+	NA	J1.B75	GND	
J1.A76	GND		J1.B76	PCIe13_RX-	NA
J1.A77	PCIe13_TX-	NA	J1.B77	PCIe13_RX+	NA
J1.A78	PCIe13_TX+	NA	J1.B78	GND	
J1.A79	GND		J1.B79	PCIe14_RX-	NA
J1.A80	PCIe14_TX-	NA	J1.B80	PCIe14_RX+	NA
J1.A81	PCIe14_TX+	NA	J1.B81	GND	
J1.A82	GND		J1.B82	PCIe15_RX-	NA
J1.A83	PCIe15_TX-	NA	J1.B83	PCIe15_RX+	NA
J1.A84	PCIe15_TX+	NA	J1.B84	GND	
J1.A85	GND		J1.B85	TEST#	PU 100k ohm
J1.A86	VCC_RTC		J1.B86	RSMRST_OUT#	
J1.A87	SUS_CLK		J1.B87	UART1_TX	
J1.A88	GPIO_00		J1.B88	UART1_RX	
J1.A89	GPIO_01		J1.B89	UART1_RTS#	
J1.A90	GPIO_02		J1.B90	UART1_CTS#	
J1.A91	GPIO_03		J1.B91	IPMB_CLK	NA
J1.A92	GPIO_04		J1.B92	IPMB_DAT	NA
J1.A93	GPIO_05		J1.B93	GP_SPI_MOSI	
J1.A94	GPIO_06		J1.B94	GP_SPI_MISO	
J1.A95	GPIO_07		J1.B95	GP_SPI_CS0#	
J1.A96	GPIO_08		J1.B96	GP_SPI_CS1#	NA
J1.A97	GPIO_09		J1.B97	GP_SPI_CS2#	NA
J1.A98	GPIO_10		J1.B98	GP_SPI_CS3#	NA
J1.A99	GPIO_11		J1.B99	GP_SPI_CLK	
J1.A100	TYPE0	NC	J1.B100	GP_SPI_ALERT#	

Table A.4: J1 Connector Rows C and D					
Pin#	**Row C Description**	**SOM-A350 Difference**	**Pin#**	**Row D Description**	**SOM-A350 Difference**
J1.C1	VCC		J1.D1	VCC	
J1.C2	RSTBTN#		J1.D2	VCC	
J1.C3	VCC		J1.D3	VCC	
J1.C4	CARRIER_HOT#		J1.D4	VCC	
J1.C5	VCC		J1.D5	VCC	
J1.C6	VIN_PWROK		J1.D6	VCC	
J1.C7	VCC		J1.D7	VCC	
J1.C8	SUS_S4_S5#		J1.D8	VCC	
J1.C9	VCC		J1.D9	VCC	
J1.C10	GND		J1.D10	WAKE0#	
J1.C11	FAN_PWMOUT		J1.D11	WAKE1#	
J1.C12	FAN_TACHIN		J1.D12	GND	
J1.C13	GND		J1.D13	USB1-	
J1.C14	USB3-		J1.D14	USB1+	
J1.C15	USB3+		J1.D15	GND	
J1.C16	GND		J1.D16	USB0-	
J1.C17	USB2-		J1.D17	USB0+	
J1.C18	USB2+		J1.D18	GND	
J1.C19	GND		J1.D19	DDI0_SDA_AUX-	
J1.C20	SNDW_DMIC_CLK1		J1.D20	DDI0_SCL_AUX+	
J1.C21	SNDW_DMIC_DAT1		J1.D21	GND	
J1.C22	GND		J1.D22	DDI0_PAIR0-	
J1.C23	SNDW_DMIC_CLK0		J1.D23	DDI0_PAIR0+	
J1.C24	SNDW_DMIC_DAT0		J1.D24	GND	
J1.C25	GND		J1.D25	DDI0_PAIR1-	
J1.C26	DDI0_DDC_AUX_SEL		J1.D26	DDI0_PAIR1+	
J1.C27	DDI1_DDC_AUX_SEL		J1.D27	GND	
J1.C28	DDI0_HPD		J1.D28	DDI0_PAIR2-	
J1.C29	DDI1_HPD		J1.D29	DDI0_PAIR2+	
J1.C30	eDP_HPD / DSI_HPD		J1.D30	GND	
J1.C31	eDP_VDD_EN / DSI_-VDD_EN		J1.D31	DDI0_PAIR3-	
J1.C32	eDP_BKLT_EN / DSI_BKLT_EN		J1.D32	DDI0_PAIR3+	
J1.C33	eDP_BKLT_CTL / DSI_BKLT_CTL		J1.D33	GND	
J1.C34	GND		J1.D34	AC_PRESENT	
J1.C35	USB1_AUX-	NA	J1.D35	RSVD	
J1.C36	USB1_AUX+	NA	J1.D36	GND	
J1.C37	GND		J1.D37	USB1_SSTX0-	
J1.C38	USB1_SSRX0-	?	J1.D38	USB1_SSTX0+	

Table A.5: J1 Connector Rows C and D					
Pin#	**Row C Description**	**SOM-A350 Difference**	**Pin#**	**Row D Description**	**SOM-A350 Difference**
J1.C39	USB1_SSRX0+		J1.D39	GND	
J1.C40	GND		J1.D40	USB1_SSTX1-	NA
J1.C41	USB1_SSRX1-	NA	J1.D41	USB1_SSTX1+	NA
J1.C42	USB1_SSRX1+	NA	J1.D42	GND	
J1.C43	GND		J1.D43	USB0_SSTX0-	
J1.C44	USB0_SSRX0-		J1.D44	USB0_SSTX0+	
J1.C45	USB0_SSRX0+		J1.D45	GND	
J1.C46	GND		J1.D46	USB0_SSTX1-	NA
J1.C47	USB0_SSRX1-	NA	J1.D47	USB0_SSTX1+	NA
J1.C48	USB0_SSRX1+	NA	J1.D48	GND	
J1.C49	GND		J1.D49	SATA0_RX-	
J1.C50	BOOT_SPI_IO0		J1.D50	SATA0_RX+	
J1.C51	BOOT_SPI_IO1		J1.D51	GND	
J1.C52	BOOT_SPI_IO2		J1.D52	SATA0_TX-	
J1.C53	BOOT_SPI_IO3		J1.D53	SATA0_TX+	
J1.C54	BOOT_SPI_CLK		J1.D54	GND	
J1.C55	GND		J1.D55	SATA1_RX-	
J1.C56	PCIe_REFCLK0_HI-		J1.D56	SATA1_RX+	
J1.C57	PCIe_REFCLK0_HI+		J1.D57	GND	
J1.C58	GND		J1.D58	SATA1_TX-	
J1.C59	PCIe_REFCLK0_LO-		J1.D59	SATA1_TX+	
J1.C60	PCIe_REFCLK0_LO+		J1.D60	GND	
J1.C61	GND		J1.D61	PCIe00_TX-	
J1.C62	PCIe00_RX-		J1.D62	PCIe00_TX+	
J1.C63	PCIe00_RX+		J1.D63	GND	
J1.C64	GND		J1.D64	PCIe01_TX-	
J1.C65	PCIe01_RX-		J1.D65	PCIe01_TX+	
J1.C66	PCIe01_RX+		J1.D66	GND	
J1.C67	GND		J1.D67	PCIe02_TX-	
J1.C68	PCIe02_RX-		J1.D68	PCIe02_TX+	
J1.C69	PCIe02_RX+		J1.D69	GND	
J1.C70	GND		J1.D70	PCIe03_TX-	
J1.C71	PCIe03_RX-		J1.D71	PCIe03_TX+	
J1.C72	PCIe03_RX+		J1.D72	GND	
J1.C73	GND		J1.D73	PCIe04_TX-	
J1.C74	PCIe04_RX-		J1.D74	PCIe04_TX+	
J1.C75	PCIe04_RX+		J1.D75	GND	

Table A.6: J1 Connector Rows C and D					
Pin#	**Row C Description**	**SOM-A350 Difference**	**Pin#**	**Row D Description**	**SOM-A350 Difference**
J1.C76	GND		J1.D76	PCIe05_TX-	
J1.C77	PCIe05_RX-		J1.D77	PCIe05_TX+	
J1.C78	PCIe05_RX+		J1.D78	GND	
J1.C79	GND		J1.D79	PCIe06_TX-	
J1.C80	PCIe06_RX-		J1.D80	PCIe06_TX+	
J1.C81	PCIe06_RX+		J1.D81	GND	
J1.C82	GND		J1.D82	PCIe07_TX-	
J1.C83	PCIe07_RX-		J1.D83	PCIe07_TX+	
J1.C84	PCIe07_RX+		J1.D84	GND	
J1.C85	GND		J1.D85	NBASET0_MDI0-	
J1.C86	SMB_CLK		J1.D86	NBASET0_MDI0+	
J1.C87	SMB_DAT		J1.D87	GND	
J1.C88	SMB_ALERT#		J1.D88	NBASET0_MDI1-	
J1.C89	UART0_TX		J1.D89	NBASET0_MDI1+	
J1.C90	UART0_RX		J1.D90	GND	
J1.C91	UART0_RTS#		J1.D91	NBASET0_MDI2-	
J1.C92	UART0_CTS#		J1.D92	NBASET0_MDI2+	
J1.C93	I2C0_CLK		J1.D93	GND	
J1.C94	I2C0_DAT		J1.D94	NBASET0_MDI3-	
J1.C95	I2C0_ALERT#		J1.D95	NBASET0_MDI3+	
J1.C96	I2C1_CLK		J1.D96	GND	
J1.C97	I2C1_DAT		J1.D97	NBASET0_LINK_-MAX#	
J1.C98	NBASET0_SDP		J1.D98	NBA-SET0_LINK_MID#	
J1.C99	NBASET0_CTREF	NC	J1.D99	NBA-SET0_LINK_ACT#	
J1.C100	TYPE1	GND	J1.D100	TYPE2	GND

Table A.7: J2 Connector Rows E and F					
Pin#	**Row E Description**	**SOM-A350 Difference**	**Pin#**	**Row F Description**	**SOM-A350 Difference**
J2.E1	RAPID_SHUTDOWN		J2.F1	FUSA_STATUS0	NA
J2.E2	GND		J2.F2	FUSA_STATUS1	NA
J2.E3	DDI2_SDA_AUX-		J2.F3	FUSA_ALERT#	NA
J2.E4	DDI2_SCL_AUX+		J2.F4	FUSA_SPI_CS#	NA
J2.E5	GND		J2.F5	FUSA_SPI_CLK	NA
J2.E6	DDI2_PAIR0-		J2.F6	FUSA_SPI_MISO	NA
J2.E7	DDI2_PAIR0+		J2.F7	FUSA_SPI_MOSI	NA
J2.E8	GND		J2.F8	FUSA_SPI_ALERT	NA
J2.E9	DDI2_PAIR1-		J2.F9	FUSA_VOLT-AGE_ERR#	NA
J2.E10	DDI2_PAIR1+		J2.F10	PROCHOT#	NA
J2.E11	GND		J2.F11	CATERR#	NA
J2.E12	DDI2_PAIR2-		J2.F12	RSVD	
J2.E13	DDI2_PAIR2+		J2.F13	RSVD	
J2.E14	GND		J2.F14	RSVD	
J2.E15	DDI2_PAIR3-		J2.F15	RSVD	
J2.E16	DDI2_PAIR3+		J2.F16	RSVD	
J2.E17	GND		J2.F17	RSVD	
J2.E18	DDI2_DDC_AUX_SEL		J2.F18	RSVD	
J2.E19	DDI2_HPD		J2.F19	GND	
J2.E20	GND		J2.F20	PCIe32_RX-	NA
J2.E21	PCIe32_TX-	NA	J2.F21	PCIe32_RX+	NA
J2.E22	PCIe32_TX+	NA	J2.F22	GND	
J2.E23	GND		J2.F23	PCIe33_RX-	NA
J2.E24	PCIe33_TX-	NA	J2.F24	PCIe33_RX+	NA
J2.E25	PCIe33_TX+	NA	J2.F25	GND	
J2.E26	GND		J2.F26	PCIe34_RX-	NA
J2.E27	PCIe34_TX-	NA	J2.F27	PCIe34_RX+	NA
J2.E28	PCIe34_TX+	NA	J2.F28	GND	
J2.E29	GND		J2.F29	PCIe35_RX-	NA
J2.E30	PCIe35_TX-	NA	J2.F30	PCIe35_RX+	NA
J2.E31	PCIe35_TX+	NA	J2.F31	GND	
J2.E32	GND		J2.F32	PCIe36_RX-	NA
J2.E33	PCIe36_TX-	NA	J2.F33	PCIe36_RX+	NA
J2.E34	PCIe36_TX+	NA	J2.F34	GND	
J2.E35	GND		J2.F35	PCIe37_RX-	NA
J2.E36	PCIe37_TX-	NA	J2.F36	PCIe37_RX+	NA
J2.E37	PCIe37_TX+	NA	J2.F37	GND	
J2.E38	GND		J2.F38	PCIe38_RX-	NA

Table A.8: J2 Connector Rows E and F					
Pin#	**Row E Description**	**SOM-A350 Difference**	**Pin#**	**Row F Description**	**SOM-A350 Difference**
J2.E39	PCIe38_TX-	NA	J2.F39	PCIe38_RX+	NA
J2.E40	PCIe38_TX+	NA	J2.F40	GND	
J2.E41	GND		J2.F41	PCIe39_RX-	NA
J2.E42	PCIe39_TX-	NA	J2.F42	PCIe39_RX+	NA
J2.E43	PCIe39_TX+	NA	J2.F43	GND	
J2.E44	GND		J2.F44	PCIe16_RX-	
J2.E45	PCIe16_TX-		J2.F45	PCIe16_RX+	
J2.E46	PCIe16_TX+		J2.F46	GND	
J2.E47	GND		J2.F47	PCIe17_RX-	
J2.E48	PCIe17_TX-		J2.F48	PCIe17_RX+	
J2.E49	PCIe17_TX+		J2.F49	GND	
J2.E50	GND		J2.F50	PCIe18_RX-	
J2.E51	PCIe18_TX-		J2.F51	PCIe18_RX+	
J2.E52	PCIe18_TX+		J2.F52	GND	
J2.E53	GND		J2.F53	PCIe19_RX-	
J2.E54	PCIe19_TX-		J2.F54	PCIe19_RX+	
J2.E55	PCIe19_TX+		J2.F55	GND	
J2.E56	GND		J2.F56	PCIe20_RX-	
J2.E57	PCIe20_TX-		J2.F57	PCIe20_RX+	
J2.E58	PCIe20_TX+		J2.F58	GND	
J2.E59	GND		J2.F59	PCIe21_RX-	
J2.E60	PCIe21_TX-		J2.F60	PCIe21_RX+	
J2.E61	PCIe21_TX+		J2.F61	GND	
J2.E62	GND		J2.F62	PCIe22_RX-	
J2.E63	PCIe22_TX-		J2.F63	PCIe22_RX+	
J2.E64	PCIe22_TX+		J2.F64	GND	
J2.E65	GND		J2.F65	PCIe23_RX-	
J2.E66	PCIe23_TX-		J2.F66	PCIe23_RX+	
J2.E67	PCIe23_TX+		J2.F67	GND	
J2.E68	GND		J2.F68	RSVD	
J2.E69	RSVD		J2.F69	RSVD	
J2.E70	RSVD		J2.F70	GND	
J2.E71	RSVD		J2.F71	NBASET1_MDI0-	
J2.E72	RSVD		J2.F72	NBASET1_MDI0+	
J2.E73	RSVD		J2.F73	GND	
J2.E74	RSVD		J2.F74	NBASET1_MDI1-	
J2.E75	RSVD		J2.F75	NBASET1_MDI1+	

Table A.9: J2 Connector Rows E and F					
Pin#	**Row E Description**	**SOM-A350 Difference**	**Pin#**	**Row F Description**	**SOM-A350 Difference**
J2.E76	RSVD		J2.F76	GND	
J2.E77	RSVD		J2.F77	NBASET1_MDI2-	
J2.E78	NBASET1_CTREF	NC	J2.F78	NBASET1_MDI2+	
J2.E79	NBASET1_SDP		J2.F79	GND	
J2.E80	NBASET1_LINK_MID#		J2.F80	NBASET1_MDI3-	
J2.E81	NBASET1_LINK_ACT#		J2.F81	NBASET1_MDI3+	
J2.E82	NBASET1_LINK_MAX#		J2.F82	GND	
J2.E83	GND		J2.F83	RSVD	
J2.E84	RSVD		J2.F84	RSVD	
J2.E85	RSVD		J2.F85	GND	
J2.E86	GND		J2.F86	ETH0_TX-	NA
J2.E87	ETH0_RX-	NA	J2.F87	ETH0_TX+	NA
J2.E88	ETH0_RX+	NA	J2.F88	GND	
J2.E89	GND		J2.F89	ETH1_TX-	NA
J2.E90	ETH1_RX-	NA	J2.F90	ETH1_TX+	NA
J2.E91	ETH1_RX+	NA	J2.F91	GND	
J2.E92	GND		J2.F92	PCIe_REFCLK2-	NA
J2.E93	PCIe_REFCLK1-		J2.F93	PCIe_REFCLK2+	NA
J2.E94	PCIe_REFCLK1+		J2.F94	GND	
J2.E95	GND		J2.F95	RSVD	
J2.E96	PCIe_CLKREQ1#		J2.F96	ETH0-1_PRSNT#	NA
J2.E97	PCIe_CLKREQ2#	NA	J2.F97	ETH0-1_PHY_RST#	NA
J2.E98	PCIe_CLKREQ_OUT0#	NA	J2.F98	ETH0_SDP	NA
J2.E99	PCIe_CLKREQ_OUT1#	NA	J2.F99	ETH1_SDP	NA
J2.E100	PCIe_PERST_IN0#		J2.F100	PCIe_PERST_IN1#	

Table A.10: J2 Connector Rows G and H					
Pin#	**Row G Description**	**SOM-A350 Difference**	**Pin#**	**Row H Description**	**SOM-A350 Difference**
J2.G1	VCC_5V_SBY		J2.H1	GND	
J2.G2	GND		J2.H2	USB2_SSTX0-	
J2.G3	USB2_SSRX0-		J2.H3	USB2_SSTX0+	
J2.G4	USB2_SSRX0+		J2.H4	GND	
J2.G5	GND		J2.H5	USB2_SSTX1-	
J2.G6	USB2_SSRX1-		J2.H6	USB2_SSTX1+	
J2.G7	USB2_SSRX1+		J2.H7	GND	
J2.G8	GND		J2.H8	USB3_SSTX0-	
J2.G9	USB3_SSRX0-		J2.H9	USB3_SSTX0+	
J2.G10	USB3_SSRX0+		J2.H10	GND	
J2.G11	GND		J2.H11	USB3_SSTX1-	
J2.G12	USB3_SSRX1-		J2.H12	USB3_SSTX1+	
J2.G13	USB3_SSRX1+		J2.H13	GND	
J2.G14	GND		J2.H14	USB2_AUX-	
J2.G15	USB3_LSRX		J2.H15	USB2_AUX+	
J2.G16	USB3_LSTX		J2.H16	GND	
J2.G17	USB2_LSRX		J2.H17	USB3_AUX-	
J2.G18	USB2_LSTX		J2.H18	USB3_AUX+	
J2.G19	PEG_LANE_REV#		J2.H19	GND	
J2.G20	GND		J2.H20	PCIe40_TX-	NA
J2.G21	PCIe40_RX-	NA	J2.H21	PCIe40_TX+	NA
J2.G22	PCIe40_RX+	NA	J2.H22	GND	
J2.G23	GND		J2.H23	PCIe41_TX-	NA
J2.G24	PCIe41_RX-	NA	J2.H24	PCIe41_TX+	NA
J2.G25	PCIe41_RX+	NA	J2.H25	GND	
J2.G26	GND		J2.H26	PCIe42_TX-	NA
J2.G27	PCIe42_RX-	NA	J2.H27	PCIe42_TX+	NA
J2.G28	PCIe42_RX+	NA	J2.H28	GND	
J2.G29	GND		J2.H29	PCIe43_TX-	NA
J2.G30	PCIe43_RX-	NA	J2.H30	PCIe43_TX+	NA
J2.G31	PCIe43_RX+	NA	J2.H31	GND	
J2.G32	GND		J2.H32	PCIe44_TX-	NA
J2.G33	PCIe44_RX-	NA	J2.H33	PCIe44_TX+	NA
J2.G34	PCIe44_RX+	NA	J2.H34	GND	
J2.G35	GND		J2.H35	PCIe45_TX-	NA
J2.G36	PCIe45_RX-	NA	J2.H36	PCIe45_TX+	NA
J2.G37	PCIe45_RX+	NA	J2.H37	GND	
J2.G38	GND		J2.H38	PCIe46_TX-	NA

Table A.11: J2 Connector Rows G and H					
Pin#	**Row G Description**	**SOM-A350 Difference**	**Pin#**	**Row H Description**	**SOM-A350 Difference**
J2.G39	PCIe46_RX-	NA	J2.H39	PCIe46_TX+	NA
J2.G40	PCIe46_RX+	NA	J2.H40	GND	
J2.G41	GND		J2.H41	PCIe47_TX-	NA
J2.G42	PCIe47_RX-	NA	J2.H42	PCIe47_TX+	NA
J2.G43	PCIe47_RX+	NA	J2.H43	GND	
J2.G44	GND		J2.H44	PCIe24_TX-	
J2.G45	PCIe24_RX-		J2.H45	PCIe24_TX+	
J2.G46	PCIe24_RX+		J2.H46	GND	
J2.G47	GND		J2.H47	PCIe25_TX-	
J2.G48	PCIe25_RX-		J2.H48	PCIe25_TX+	
J2.G49	PCIe25_RX+		J2.H49	GND	
J2.G50	GND		J2.H50	PCIe26_TX-	
J2.G51	PCIe26_RX-		J2.H51	PCIe26_TX+	
J2.G52	PCIe26_RX+		J2.H52	GND	
J2.G53	GND		J2.H53	PCIe27_TX-	
J2.G54	PCIe27_RX-		J2.H54	PCIe27_TX+	
J2.G55	PCIe27_RX+		J2.H55	GND	
J2.G56	GND		J2.H56	PCIe28_TX-	
J2.G57	PCIe28_RX-		J2.H57	PCIe28_TX+	
J2.G58	PCIe28_RX+		J2.H58	GND	
J2.G59	GND		J2.H59	PCIe29_TX-	
J2.G60	PCIe29_RX-		J2.H60	PCIe29_TX+	
J2.G61	PCIe29_RX+		J2.H61	GND	
J2.G62	GND		J2.H62	PCIe30_TX-	
J2.G63	PCIe30_RX-		J2.H63	PCIe30_TX+	
J2.G64	PCIe30_RX+		J2.H64	GND	
J2.G65	GND		J2.H65	PCIe31_TX-	
J2.G66	PCIe31_RX-		J2.H66	PCIe31_TX+	
J2.G67	PCIe31_RX+		J2.H67	GND	
J2.G68	GND		J2.H68	RSVD	
J2.G69	RSVD		J2.H69	RSVD	
J2.G70	RSVD		J2.H70	GND	
J2.G71	GND		J2.H71	CSI1_RX0-	NA
J2.G72	CSI0_RX0-	NA	J2.H72	CSI1_RX0+	NA
J2.G73	CSI0_RX0+	NA	J2.H73	GND	
J2.G74	GND		J2.H74	CSI1_RX1-	NA
J2.G75	CSI0_RX1-	NA	J2.H75	CSI1_RX1+	NA

Table A.12: J2 Connector Rows G and H					
Pin#	**Row G Description**	**SOM-A350 Difference**	**Pin#**	**Row H Description**	**SOM-A350 Difference**
J2.G76	CSI0_RX1+	NA	J2.H76	GND	
J2.G77	GND		J2.H77	CSI1_RX2-	NA
J2.G78	CSI0_RX2-	NA	J2.H78	CSI1_RX2+	NA
J2.G79	CSI0_RX2+	NA	J2.H79	GND	
J2.G80	GND		J2.H80	CSI1_RX3-	NA
J2.G81	CSI0_RX3-	NA	J2.H81	CSI1_RX3+	NA
J2.G82	CSI0_RX3+	NA	J2.H82	GND	
J2.G83	GND		J2.H83	CSI1_CLK-	NA
J2.G84	CSI0_CLK-	NA	J2.H84	CSI1_CLK+	NA
J2.G85	CSI0_CLK+	NA	J2.H85	GND	
J2.G86	GND		J2.H86	CSI1_I2C_CLK	NA
J2.G87	CSI0_I2C_CLK	NA	J2.H87	CSI1_I2C_DAT	NA
J2.G88	CSI0_I2C_DAT	NA	J2.H88	CSI1_MCLK	NA
J2.G89	CSI0_MCLK	NA	J2.H89	CSI1_RST#	NA
J2.G90	CSI0_RST#	NA	J2.H90	CSI1_ENA	NA
J2.G91	CSI0_ENA	NA	J2.H91	GND	
J2.G92	GND		J2.H92	PCIe_REFCLKIN0-	NA
J2.G93	RSVD		J2.H93	PCIe_REFCLKIN0+	NA
J2.G94	RSVD		J2.H94	GND	
J2.G95	GND		J2.H95	PCIe_REFCLKIN1-	NA
J2.G96	ETH0-1_I2C_CLK	NA	J2.H96	PCIe_REFCLKIN1+	NA
J2.G97	ETH0-1_I2C_DAT	NA	J2.H97	GND	
J2.G98	ETH0-1_PHY_INT#	NA	J2.H98	ETH0-1_MDIO_CLK	NA
J2.G99	ETH0-1_INT#	NA	J2.H99	ETH0-1_MDIO_DAT	NA
J2.G100	PCIe_WAKE_OUT0#	NA	J2.H100	PCIe_WAKE_OUT1#	NA

Appendix B

Watchdog Timer

This appendix details information about the watchdog timer programming on the SOM-A350 CPU System on Module.

Sections include:

- Watchdog Timer Programming

B.1 Programming the Watchdog Timer

Table B.1: Programming the Watchdog Timer

Trigger Event	Note
IRQ	(BIOS setting default disable)**
NMI	N/A
SCI	Support
Power Off	Support
H/W Restart	Support
WDT Pin Activate	Support

** WDT new driver support automatically selects available IRQ number from BIOS, and then sets it to EC. Only Win10 supports this.

In other OS, it will still use IRQ number from BIOS setting as usual. For more details, please refer to iManager & Software API User Manual.

Appendix C

Programming GPIO

This Appendix illustrates the General Purpose Input and Output pin settings.

Sections include:

- **GPIO Register**

C.1 GPIO Register

Table C.1: GPIO Register	
GPIO Byte Mapping	**H/W Pin Name**
BIT0	GPI0
BIT1	GPI1
BIT2	GPI2
BIT3	GPI3
BIT4	GPO0
BIT5	GPO1
BIT6	GPO2
BIT7	GPO3

For details, please refer to iManager & Software API User Manual.

Appendix D

System Assignments

This appendix gives you the information about the system resource allocation on the SOM-A350 CPU System on Module.

Sections include:

- System I/O Ports
- DMA Channel Assignments
- Interrupt Assignments
- 1st MB Memory Map

D.1 System I/O Ports

Table D.1: System I/O Ports	
Addr. Range (Hex)	**Device**
0x0000EFA0-0x0000EFBF	Intel(R) SMBus - 7E22
0x00000299-0x0000029A	Motherboard resources
0x000002C0-0x000002DF	Motherboard resources
0x000002A0-0x000002BF	Motherboard resources
0x000002A0-0x000002BF	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x0000029E-0x000002AD	Motherboard resources
0x00000060-0x0000006F	Motherboard resources
0x00000200-0x0000027F	Motherboard resources
0x00000300-0x0000037F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x000002F0-0x000002F7	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x00001854-0x00001857	Motherboard resources
0x00000062-0x00000062	Microsoft ACPI-Compliant Embedded Controller
0x00000066-0x00000066	Microsoft ACPI-Compliant Embedded Controller
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller

Table D.1: System I/O Ports	
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x00003050-0x00003057	Standard SATA AHCI Controller
0x00003040-0x00003043	Standard SATA AHCI Controller
0x00003020-0x0000303F	Standard SATA AHCI Controller
0x00000000-0x00000CF7	PCI Express Root Complex
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x0000FFF8-0x0000FFFF	Intel(R) Active Management Technology - SOL (COM3)
0x00002000-0x000020FE	Motherboard resources
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer

D.2 Interrupt Assignments

Table D.2: Interrupt Assignments	
Addr. Range (Hex)	**Device**
IRQ 4294967294	PCI Express Root Port
IRQ 4294967271 - IRQ 4294967287	Intel(R) Ethernet Controller I226-LMvP
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 4294967292	Standard SATA AHCI Controller
IRQ 6	Motherboard resources
IRQ 4294967288	Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 34	Intel(R) Serial IO I2C Host Controller - 7E7A
IRQ 111	Trusted Platform Module 2.0
IRQ55 - IRQ 204	Microsoft ACPI-Compliant System
IRQ 256 - IRQ 511	Microsoft ACPI-Compliant System
IRQ 4294967290	Intel(R) Arc(TM) Graphics
IRQ 4294967290	Intel(R) Arc(TM) Graphics
IRQ 19	Intel(R) Active Management Technology - SOL (COM3)
IRQ 4294967289	Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967291	Intel(R) Management Engine Interface #1
IRQ 0	System timer
IRQ 32	Intel(R) Serial IO I2C Host Controller - 7E78
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INTC1083
IRQ 4294967293	PCI Express Root Port

D.3 1st MB Memory Map

Table D.3: 1st MB Memory Map	
Addr. Range (Hex)	**Device**
0x11268000-0x112680FF	Intel(R) SMBus - 7E22
0xFEDC0000-0xFEDC7FFF	Motherboard resources
0x0000-0x0FFF	Motherboard resources
0x0000-0x0FFF	Motherboard resources
0xC0000000-0xCFFFFFFF	Motherboard resources
0xFED20000-0xFED7FFFF	Motherboard resources
0xFC800000-0xFC81FFFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0xBFFC0000-0xBFFFFFFF	Intel(R) Platform Monitoring Technology (PMT) Driver
0x80000000-0x802FFFFF	PCI Express Root Port
0x80000000-0x802FFFFF	PCI Express Root Complex
0x80100000-0x801FFFFF	Intel(R) Ethernet Controller I226-LMvP
0x80200000-0x80203FFF	Intel(R) Ethernet Controller I226-LMvP
0xFED00000-0xFED003FF	High precision event timer
0x80400000-0x80401FFF	Standard SATA AHCI Controller
0x80403000-0x804030FF	Standard SATA AHCI Controller
0x80402000-0x804027FF	Standard SATA AHCI Controller
0x11240000-0x1124FFFF	Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
0xA0000-0xBFFFF	PCI Express Root Complex
0x1126A000-0x1126AFFF	Intel(R) Serial IO I2C Host Controller - 7E7A
0x10000000-0x10FFFFFF	Intel(R) Arc(TM) Graphics
0x0000-0xFFFFFFF	Intel(R) Arc(TM) Graphics
0xFED40000-0xFED44FFF	Trusted Platform Module 2.0
0xFE010000-0xFE010FFF	Intel(R) SPI - 7E23
0x80300000-0x8037FFFF	PCI Express Upstream Switch Port
0x80300000-0x8037FFFF	PCI Express Root Port
0xBFFFF000-0xBFFFFFFF	Intel(R) Active Management Technology - SOL (COM3)
0x11250000-0x1125FFFF	Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
0x11269000-0x11269FFF	Intel(R) Management Engine Interface #1
0x1126B000-0x1126BFFF	Intel(R) Serial IO I2C Host Controller - 7E78
0xE0D10000-0xE0D1FFFF	Intel(R) Serial IO GPIO Host Controller - INTC1083
0xE0D20000-0xE0D2FFFF	Intel(R) Serial IO GPIO Host Controller - INTC1083
0xE0D30000-0xE0D3FFFF	Intel(R) Serial IO GPIO Host Controller - INTC1083
0xE0D40000-0xE0D4FFFF	Intel(R) Serial IO GPIO Host Controller - INTC1083
0xE0D50000-0xE0D5FFFF	Intel(R) Serial IO GPIO Host Controller - INTC1083
0xBFFBC000-0xBFFBFFFF	Intel® Smart Sound Technology BUS
0xBFC00000-0xBFDFFFFF	Intel® Smart Sound Technology BUS

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Please verify specifications before quoting. This guide is intended for reference purposes only.

All product specifications are subject to change without notice.