

ET980 Series

**Intel® 12th Gen. Core™
COM Express Type 6 Module**

User's Manual

Version 1.0
(June 2023)

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Compliance



This product has passed CE tests for environmental specifications and limits. This product is in accordance with the directives of the European Union (EU). In a domestic environment, this product may cause radio interference in which case users may be required to take adequate measures.



This product has been tested and found to comply with the limits for a Class B device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer's instructions, may cause harmful interference to radio communications.

WEEE



This product must not be disposed of as normal household waste, in accordance with the EU directive of for waste electrical and electronic equipment (WEEE - 2012/19/EU). Instead, it should be disposed of by returning it to a municipal recycling collection point. Check local regulations for disposal of electronic products.

Green IBASE



This product is compliant with the current RoHS restrictions and prohibits use of the following substances in concentrations exceeding 0.1% by weight (1000 ppm) except for cadmium, limited to 0.01% by weight (100 ppm).

- Lead (Pb)
- Mercury (Hg)
- Cadmium (Cd)
- Hexavalent chromium (Cr6+)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ether (PBDE)

Important Safety Information

Carefully read the precautions before using the board.

Environmental conditions:

- Use this product in environments with ambient temperatures between 0°C and 60°C.
- Do not leave this product in an environment where the storage temperature may be below -20° C or above 80° C. To prevent from damages, the product must be used in a controlled environment.

Care for your IBASE products:

- Before cleaning the PCB, unplug all cables and remove the battery.
- Clean the PCB with a circuit board cleaner or degreaser, or use cotton swabs and alcohol.
- Vacuum the dust with a computer vacuum cleaner to prevent the fan from being clogged.



WARNING

Attention during use:

- Do not use this product near water.
- Do not spill water or any other liquids on this product.
- Do not place heavy objects on the top of this product.

Anti-static precautions

- Wear an anti-static wrist strap to avoid electrostatic discharge.
- Place the PCB on an anti-static kit or mat.
- Hold the edges of PCB when handling.
- Touch the edges of non-metallic components of the product instead of the surface of the PCB.
- Ground yourself by touching a grounded conductor or a grounded bit of metal frequently to discharge any static.



CAUTION

Danger of explosion if the internal lithium-ion battery is replaced by an incorrect type. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions or recycle them at a local recycling facility or battery collection point.

Warranty Policy

- **IBASE standard products:**

24-month (2-year) warranty from the date of shipment. If the date of shipment cannot be ascertained, the product serial numbers can be used to determine the approximate shipping date.

- **3rd-party parts:**

12-month (1-year) warranty from delivery for the 3rd-party parts that are not manufactured by IBASE, such as CPU, CPU cooler, memory, storage devices, power adapter, panel and touchscreen.

- * PRODUCTS, HOWEVER, THAT FAIL DUE TO MISUSE, ACCIDENT, IMPROPER INSTALLATION OR UNAUTHORIZED REPAIR SHALL BE TREATED AS OUT OF WARRANTY AND CUSTOMERS SHALL BE BILLED FOR REPAIR AND SHIPPING CHARGES.

Technical Support & Services

1. Visit the IBASE website at www.ibase.com.tw to find the latest information about the product.
2. If you need any further assistance from your distributor or sales representative, prepare the following information of your product and elaborate upon the problem.
 - Product model name
 - Product serial number
 - Detailed description of the problem
 - The error messages in text or in screenshots if there is any
 - The arrangement of the peripherals
 - Software in use (such as OS and application software, including the version numbers)
3. If repair service is required, please log in the RMA system of the website or and contact your distributor or sales representative for assistance.

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Chapter 1

General Information

The information provided in this chapter includes:

- Features
- Packing List
- Optional Accessories
- Specifications
- Block Diagram
- Board View
- Board Dimensions

1.1 Introduction

Designed for computing embedded applications in industrial, gaming, medical and various IoT applications, ET980 is a COM Express module based on the platform of Intel 12th Gen. Core i7/i5/i3 processors. It supports COM Express carrier boards that can be upgraded to newer or backward-compatible versions. The ET980 features two DDR4-3200 memory slots, 2.5GbE connectivity, triple independent displays, and a comprehensive set of I/O including 4x USB 3.2, 8x USB 2.0, 2x SATA III, 2x COM, as well expansion slots for 1x PCI-E(x16), 1x PCI-E(x4), 4x PCI-E(x1) via the carrier board.

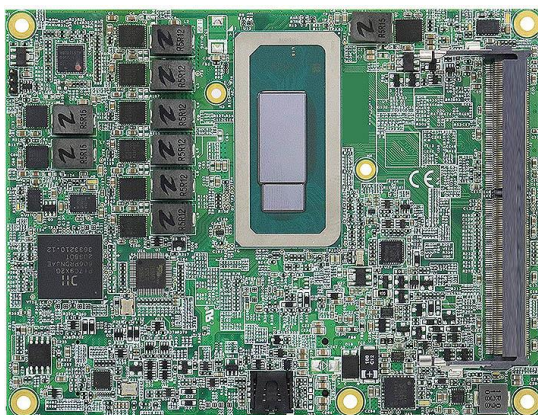


Photo of ET980

1.2 Features

- Onboard 12th Gen Intel® Core™ i7/i5/i3 processors
- 2x DDR4-3200 SO-DIMM sockets, Max. 64GB
- Onboard 2.5 GbE
- Supports 3x independent displays - HDMI / DP / VGA / LVDS or eDP
- 4x USB 3.2, 8x USB 2.0, 2x SATA III, 2x COM
- 1x PCI-E(x8) [2x PCI-E(4x) signal**], 1x PCI-e(x4), 4x PCI-E(x1) to carrier board
- **Only one PCI-E (x8) signal from Alder Lake-P 28W/15W CPU skus**
- *Digital I/O, TPM (2.0), Watchdog timer

1.3 Packing List

Your ET980 package should include the items listed below. If any of the items below is missing, contact the distributor or dealer from whom you purchased the product.

- ET980 COM Express Module x 1

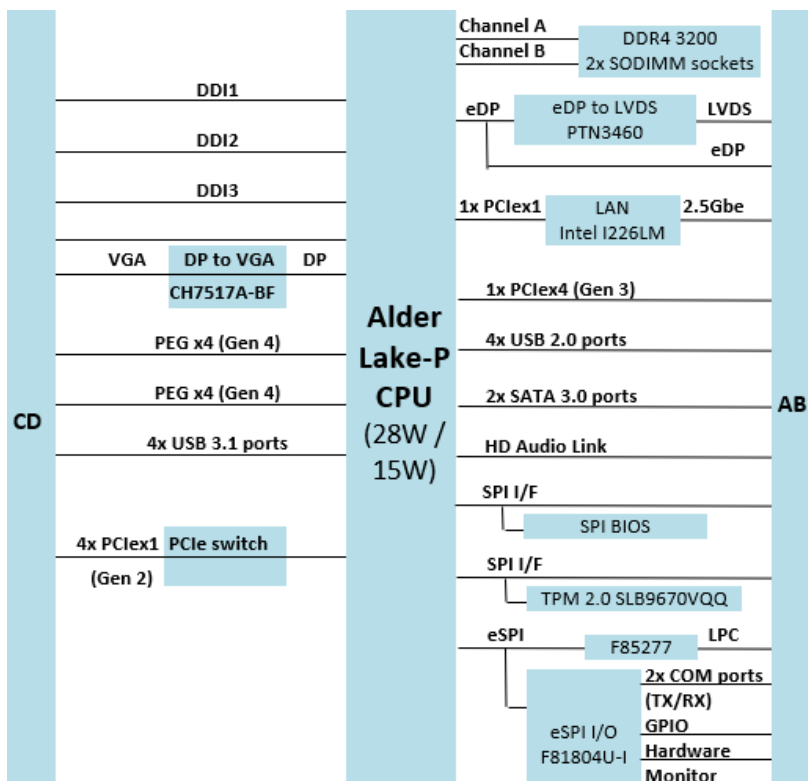
1.4 Specifications

Product Models	
ET980LV-I7U - Intel® Core™ i7-1265UE with LVDS support ET980LV-I7P - Intel® Core™ i7-1270PE with LVDS support ET980LV-I5U - Intel® Core™ i5-1245UE with LVDS support ET980-I5U - Intel® Core™ i5-1245UE with eDP support ET980LV-I5P - Intel® Core™ i5-1250PE with LVDS support ET980LV-I3P - Intel® Core™ i3-1220PE with LVDS support	
System	
Operating System	Windows 10 (64-bit)
Memory	2x DDR4-3200 SO-DIMM sockets, Max. 64GB, ECC compatible
Graphics	12th Gen Intel® Core™ P-series processor integrated graphics
Video Output	HDMI, DisplayPort, VGA, LVDS or eDP on carrier board
Ethernet	Intel® I226LM 2.5 GbE RJ45 on carrier board
Super I/O	Fintek F81804U-I
USB 2.0	8x USB 2.0 via carrier board
USB 3.X	4x USB 3.1 (Gen 2) via carrier board
Serial ATA	2x SATA III via carrier board
Audio	Built-in HD Audio controller
Expansion Slot	1x PCI-E(x8) [(Gen. 4) (PCIe(4x)+ PCIe(4x)), 1xPCI-E(x4) (Gen. 3), 4x PCI-E(x1) (Gen. 2) to carrier board
Power	+12V and +5VSB for ATX, +12V for AT

Watchdog Timer	Yes (256 segments, 0, 1, 2...255 sec / min)
BIOS	AMI BIOS
H/W Monitor	Yes
TPM	TPM (2.0)
Dimensions	125 x 95 mm (4.92" x 3.74")
Certification	CE, FCC Class B, LVD
RoHS	Yes
Environment	
Temperature	<ul style="list-style-type: none">• Operation: 0 ~ 60 °C (32 ~ 140 °F)• Storage: -20 ~ 80 °C (-4 ~ 176 °F)
Relative Humidity	10 ~ 95 %, non-condensing

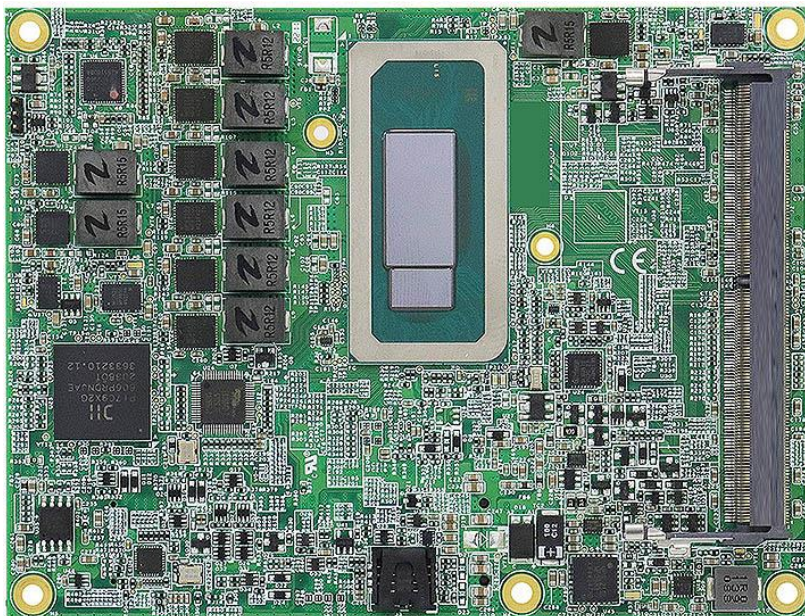
All specifications are subject to change without prior notice.

1.5 Block Diagram

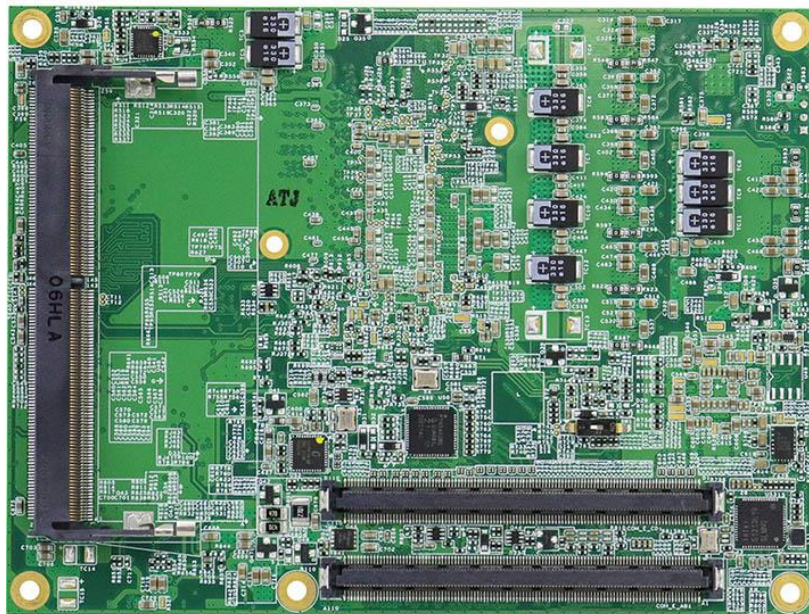


1.6 Board View

Top View



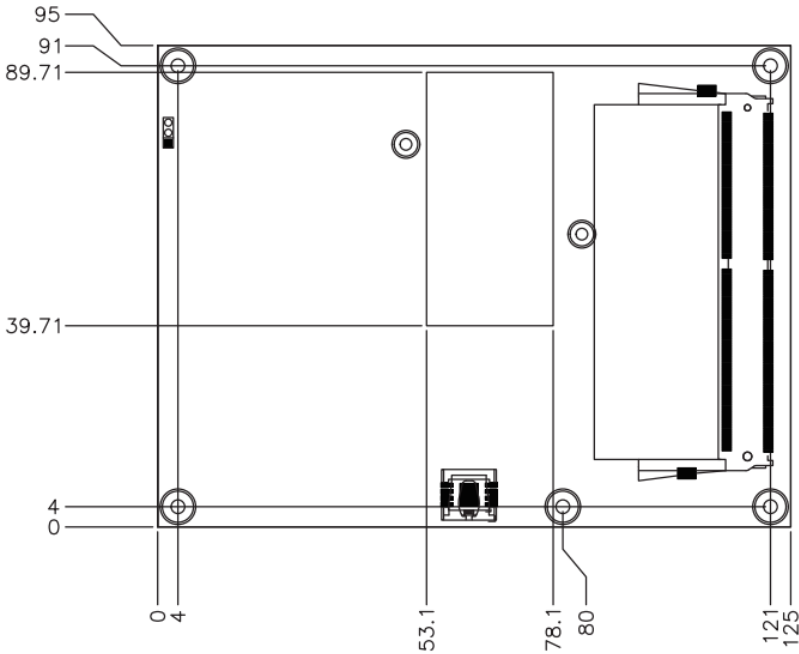
Bottom View



* The pictures are for reference only. Some minor components may differ.

1.7 Dimensions

Unit: mm



Chapter 2

Hardware Configuration

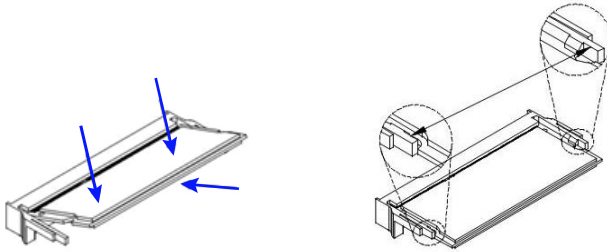
This section provides information on jumper settings and connectors on the ET980 in order to set up a workable system. On top of that, you will also need to install crucial pieces such as the CPU and the memory before using the product. The topics covered are:

- Installations
- Switch and connector locations and information

2.1 Installations

2.1.1 Installing the Memory

To replace or install a memory module, locate the memory slot (J2, J4) on the board and perform the following steps:

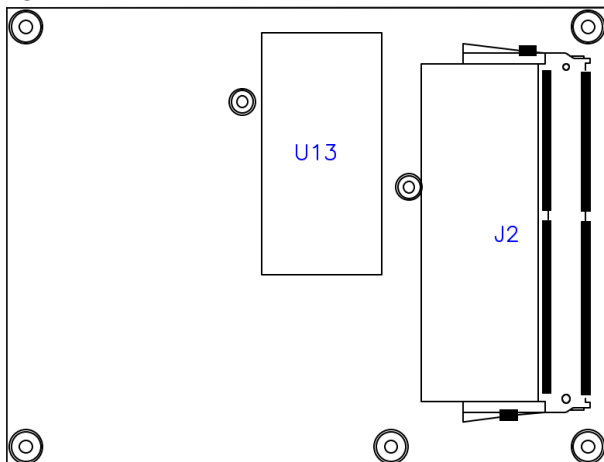


1. Align the key of the memory module with that on the memory slot and insert the module slantwise.
2. Gently push the module in an upright position until the clips of the slot close to hold the module in place when the module touches the bottom of the slot.

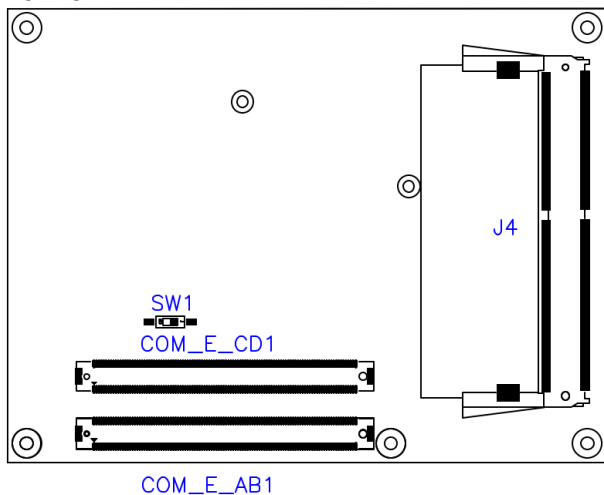
To remove the module, press the clips outwards with both hands, and the module will pop-up.

2.2 Switch & Connector Locations

TOP VIEW



BOTTOM VIEW



Remarks:

SW1: ATX / AT Mode



J2, J4: SO-DIMM Sockets

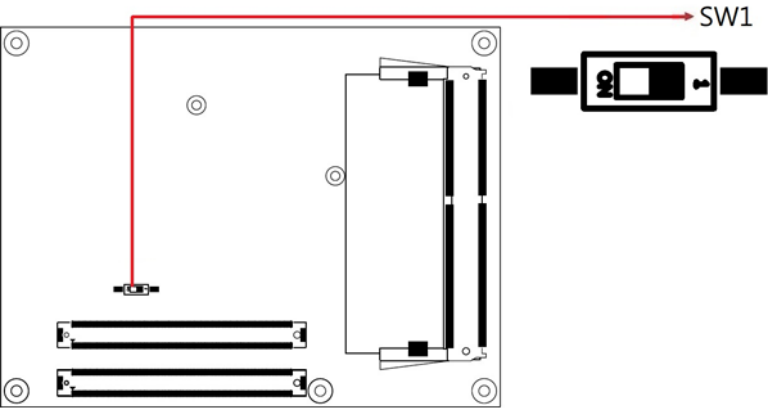
COM_E_AB1, COM_E_CD1: COM Express Module Type 6 Connector

2.3 Switch & Connector Quick Reference

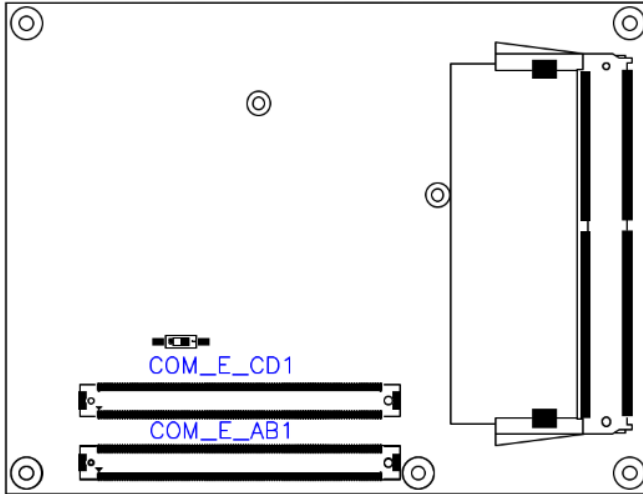
Function	Jumper	Page
ATX / AT Mode	SW1	12
COM Express Module Type 6 Connector	(COM_E_AB1, COM_E_CD1)	13

2.3.1 ATX / AT Mode (SW1)

Function	Pin closed	Illustration
ATX (default)	P1-OFF	
AT	P1-ON	



2.3.2 COM Express Module Type 6 Connector



Row A		Row B		Row C		Row D	
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	GND	D2	GND
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	USB_SSRX0-	D3	USB_SSTX0-
A4	GBE0_LINK100#	B4	LPC_AD0	C4	USB_SSRX0+	D4	USB_SSTX0+
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	GND	D5	GND
A6	GBE0_MDI2-	B6	LPC_AD2	C6	USB_SSRX1-	D6	USB_SSTX1-
A7	GBE0_MDI2+	B7	LPC_AD3	C7	USB_SSRX1+	D7	USB_SSTX1+
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	GND	D8	GND
A9	GBE0_MDI1-	B9	NC	C9	USB_SSRX2-	D9	USB_SSTX2-
A10	GBE0_MDI1+	B10	LPC_CLK	C10	USB_SSRX2+	D10	USB_SSTX2+
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	USB_SSRX3-	D12	USB_SSTX3-
A13	GBE0_MDI0+	B13	SMB_CK	C13	USB_SSRX3+	D13	USB_SSTX3+
A14	GBE0_CTREF	B14	SMB_DAT	C14	GND	D14	GND
A15	SUS_S3#	B15	SMB_ALERT#	C15	NC	D15	DDI1_CTRLCLK_AUX+
A16	SATA0_TX+	B16	SATA1_TX+	C16	NC	D16	DDI1_CTRLCLK_AUX-
A17	SATA0_TX-	B17	SATA1_TX-	C17	RSVD	D17	RSVD
A18	SUS_S4#	B18	NC	C18	RSVD	D18	RSVD
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCIE_RX6+	D19	PCIE_TX6+
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCIE_RX6-	D20	PCIE_TX6-
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	NC	B22	NC	C22	PCIE_RX7+	D22	PCIE_TX7+
A23	NC	B23	NC	C23	PCIE_RX7-	D23	PCIE_TX7-
A24	SUS_S5#	B24	PWR_OK	C24	DDI1_HPD	D24	RSVD
A25	NC	B25	NC	C25	NC	D25	RSVD
A26	NC	B26	NC	C26	NC	D26	DDI1_PAIR0+
A27	BATLOW#	B27	WDT	C27	RSVD	D27	DDI1_PAIR0-
A28	SATA_ACT#	B28	NC	C28	RSVD	D28	RSVD
A29	HDA_SYNC	B29	NC	C29	NC	D29	DDI1_PAIR1+
A30	HDA_RST#	B30	HDA_SDIN0	C30	NC	D30	DDI1_PAIR1-

Row A		Row B		Row C		Row D	
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	HDA_BITCLK	B32	NC	C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
A33	HDA_SDOUT	B33	I2C_CK	C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
A34	BIOS_DIS0#	B34	I2C_DAT	C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
A35	THRMTRIP#	B35	THRM#	C35	RSVD	D35	RSVD
A36	USB6-	B36	USB7-	C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+
A37	USB6+	B37	USB7+	C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	DDI3_DDC_AUX_SEL	D38	RSVD
A39	USB4-	B39	USB5-	C39	DDI3_PAIR0+	D39	DDI2_PAIR0+
A40	USB4+	B40	USB5+	C40	DDI3_PAIR0-	D40	DDI2_PAIR0-
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	DDI3_PAIR1+	D42	DDI2_PAIR1+
A43	USB2+	B43	USB3+	C43	DDI3_PAIR1-	D43	DDI2_PAIR1-
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	DDI2_HPD	D44	DDI2_HPD
A45	USB0-	B45	USB1-	C45	RSVD	D45	RSVD
A46	USB0+	B46	USB1+	C46	DDI3_PAIR2+	D46	DDI2_PAIR2+
A47	VCC_RTC	B47	NC	C47	DDI3_PAIR2-	D47	DDI2_PAIR2-
A48	RSVD	B48	NC	C48	RSVD	D48	RSVD
A49	GBE0_SDP	B49	SYS_RESET#	C49	DDI3_PAIR3+	D49	DDI2_PAIR3+
A50	LPC_SERIRQ	B50	CB_RESET#	C50	DDI3_PAIR3-	D50	DDI2_PAIR3-
A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+	C52	RSVD	D52	RSVD
A53	PCIE_TX5-	B53	PCIE_RX5-	C53	RSVD	D53	RSVD
A54	GPIO	B54	GPO1	C54	NC	D54	NC
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	RSVD	D55	RSVD
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	RSVD	D56	RSVD
A57	GND	B57	GPO2	C57	NC	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	RSVD	D58	RSVD
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	RSVD	D59	RSVD
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	RSVD	D61	RSVD
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	RSVD	D62	RSVD
A63	GPI1	B63	GPO3	C63	RSVD	D63	RSVD
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	RSVD	D64	RSVD
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	RSVD	D65	RSVD
A66	GND	B66	WAKE0#	C66	RSVD	D66	RSVD
A67	GPIO2	B67	WAKE1#	C67	NC	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	RSVD	D68	RSVD
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	RSVD	D69	RSVD
A70	GND (FIXED)	B70	GND (FIXED)	C70	GND (FIXED)	D70	GND (FIXED)
A71	LVDS_A0+/ eDP_TX2+	B71	LVDS_B0+	C71	RSVD	D71	RSVD
A72	LVDS_A0-/ eDP_TX2-	B72	LVDS_B0-	C72	RSVD	D72	RSVD
A73	LVDS_A1+/ eDP_TX1+	B73	LVDS_B1+	C73	GND	D73	GND
A74	LVDS_A1-/ eDP_TX1-	B74	LVDS_B1-	C74	RSVD	D74	RSVD
A75	LVDS_A2+/ eDP_TX0+	B75	LVDS_B2+	C75	RSVD	D75	RSVD

Row A		Row B		Row C		Row D	
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A76	LVDS_A2-/eDP_TX0-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN/eDP_VDD_EN	B77	LVDS_B3+	C77	RSVD	D77	RSVD
A78	LVDS_A3+	B78	LVDS_B3-	C78	PEG_RX8+	D78	PEG_TX8+
A79	LVDS_A3-	B79	LVDS_BKLT_EN/eDP_BKLT_EN	C79	PEG_RX8-	D79	PEG_TX8-
A80	GND (FIXED)	B80	GND (FIXED)	C80	GND (FIXED)	D80	GND (FIXED)
A81	LVDS_A_CK+/eDP_TX3+	B81	LVDS_B_CK+	C81	PEG_RX9+	D81	PEG_TX9+
A82	LVDS_A_CK-/eDP_TX3-	B82	LVDS_B_CK-	C82	PEG_RX9-	D82	PEG_TX9-
A83	LVDS_I2C_CK/eDP_AUX+	B83	LVDS_BKLT_CTRL	C83	RSVD	D83	RSVD
A84	LVDS_I2C_DAT/eDP_AUX-	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PEG_RX10+	D85	PEG_TX10+
A86	RSVD	B86	VCC_5V_SBY	C86	PEG_RX10-	D86	PEG_TX10-
A87	eDP_HPD	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE_CLK_REF+	B88	BIOS_DIS1#	C88	PEG_RX11+	D88	PEG_TX11+
A89	PCIE_CLK_REF-	B89	VGA_RED	C89	PEG_RX11-	D89	PEG_TX11-
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN	C91	PEG_RX12+	D91	PEG_TX12+
A92	SPI_MISO	B92	VGA_BLU	C92	PEG_RX12-	D92	PEG_TX12-
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	SPI_CLK	B94	VGA_VSYNC	C94	PEG_RX13+	D94	PEG_TX13+
A95	SPI_MOSI	B95	VGA_I2C_CK	C95	PEG_RX13-	D95	PEG_TX13-
A96	TPM_PP	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97	NC	B97	SPI_CS#	C97	RSVD	D97	RSVD
A98	SER0_TX	B98	RSVD	C98	PEG_RX14+	D98	PEG_TX14+
A99	SER0_RX	B99	RSVD	C99	PEG_RX14-	D99	PEG_TX14-
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWMOUT	C101	PEG_RX15+	D101	PEG_TX15+
A102	SER1_RX	B102	FAN_TACHIN	C102	PEG_RX15-	D102	PEG_TX15--
A103	NC	B103	NC	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

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Chapter 3

Drivers Installation

This chapter introduces installation of the following drivers:

- Intel® Chipset Software Installation Utility
- Graphics Driver
- HD Audio Driver
- LAN Driver
- Intel® Management Engine Drivers
- Intel® Serial IO Drivers

3.1 Introduction

This section describes the installation procedures for software and drivers. The contents of this section include the following:

Note: After installing your Windows operating system, you must install the Intel® Chipset Software Installation Utility first before proceeding with the drivers installation.

3.2 Intel® Chipset Software Installation Utility

The Intel® Chipset drivers should be installed first before the software drivers to install INF files for Plug & Play function for Intel chipset components. Follow the instructions below to complete the installation.

1. Go to the download page of the product. Copy the compressed drivers file to your computer. Double click the file to decompress it. Run “CDGuide” to go to the main drivers page as shown. Click **Intel** on the left pane and then **Intel(R) AlderLake-P Chipset Drivers** on the right pane.



2. Click **Intel(R) Chipset Software Installation Utility**.



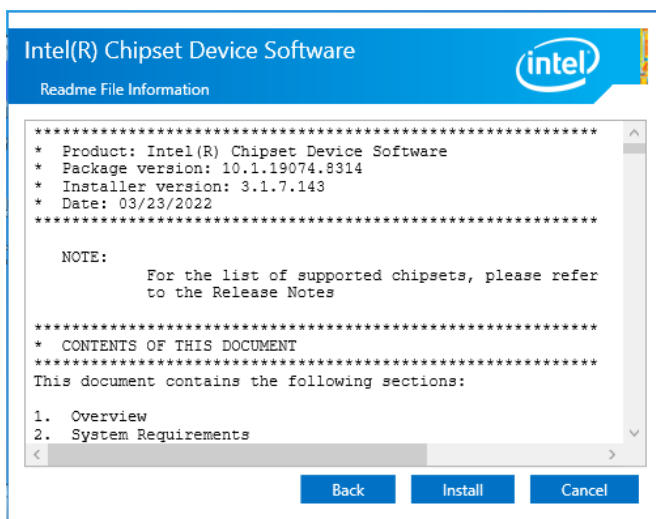
3. When the *Welcome* screen to the Intel® Chipset Device Software appears, click **Next**.



4. Accept the software license agreement.



5. On the *Readme File Information* screen, click **Install**.



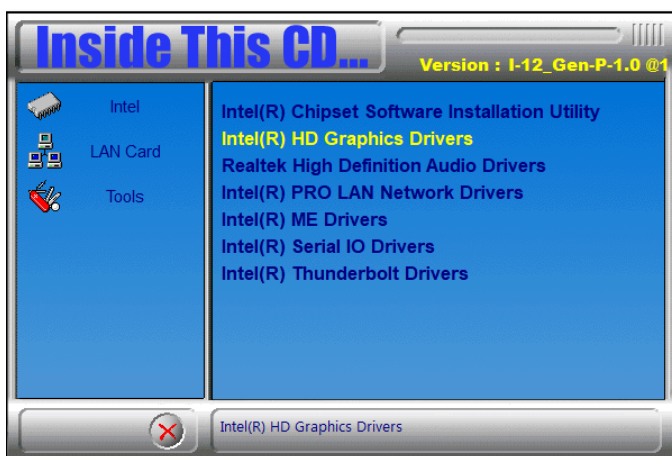
6. The driver has been completely installed. Click **Finish**.

3.3 Graphics Driver Installation

1. Click **Intel** on the left pane and then **Intel(R) AlderLake-P Chipset Drivers** on the right pane.



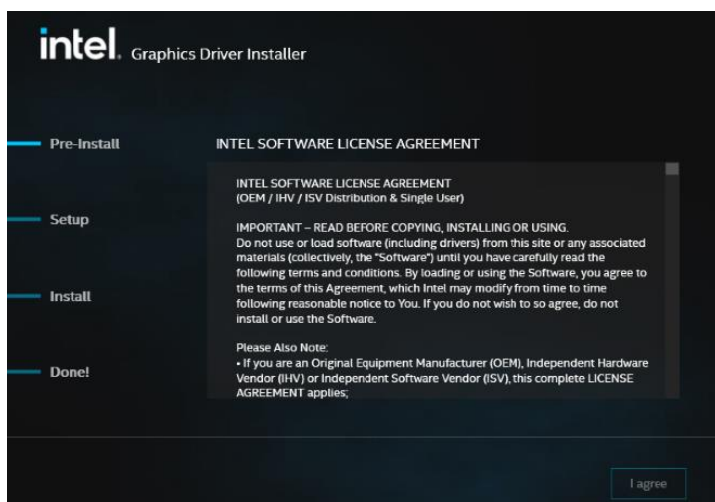
2. Click **Intel(R) HD Graphics Driver**.



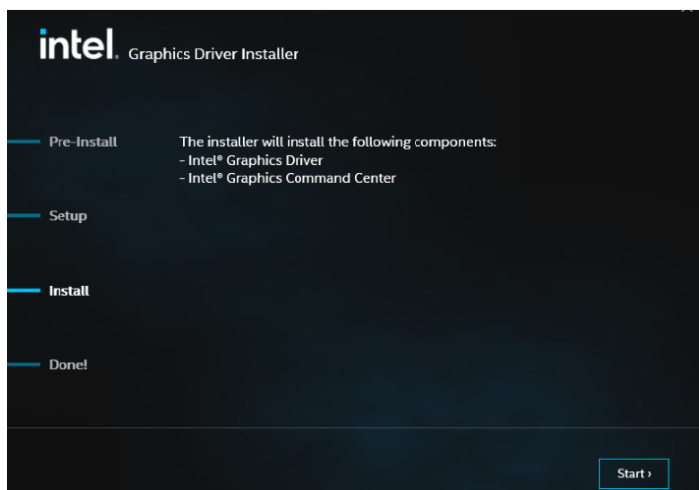
- On the next screen shown below, click **Begin installation**.



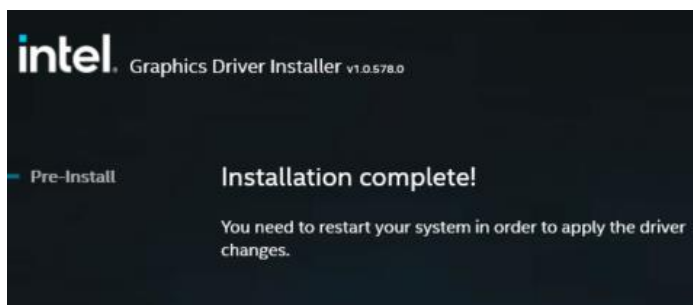
- Click **I agree**.



5. Click **Start**.



6. When installation is complete, restart your system in order to apply the driver changes.

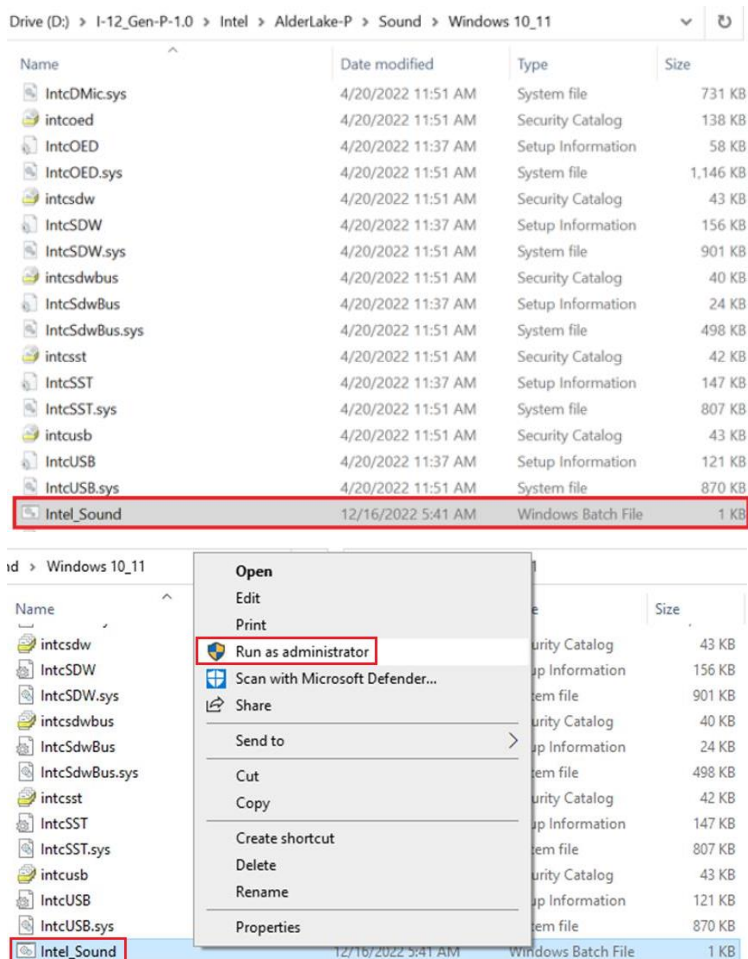


3.4 HD Audio Driver Installation

- Before installing the audio drivers in the disk provided, run the batch file - **Intel_Sound.bat** in the directory shown in the picture below:

I-12_Gen-P-1.0\Intel\AlderLake-P\Sound\Windows 10_11

Right-click **Intel_Sound.bat** and **run the batch file as administrator**.

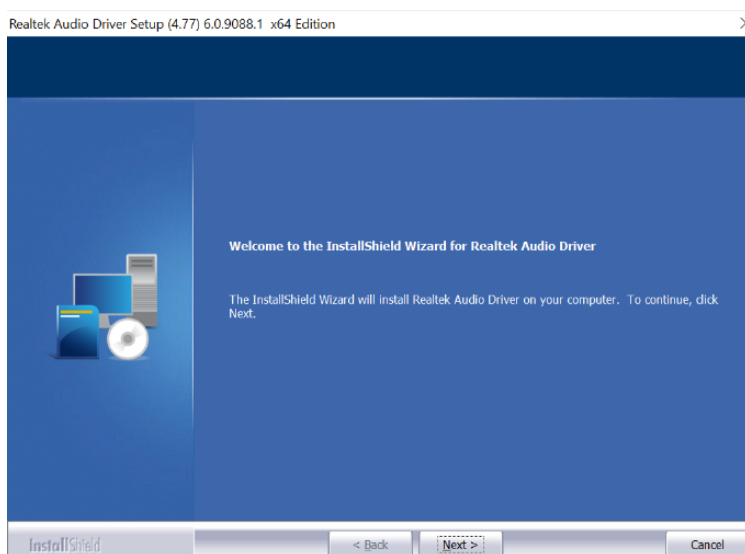


- After running the batch file, install the audio drivers. Click **Intel** on the left pane and then **Intel(R) AlderLake-P Chipset Drivers** on the right.

- Click **Realtek High Definition Audio Drivers**.



- On the *Welcome* screen of the InstallShield Wizard, click **Next**.



- When the InstallShield Wizard has completed the installation, restart your computer to be able to use the program.

3.5 LAN Driver Installation

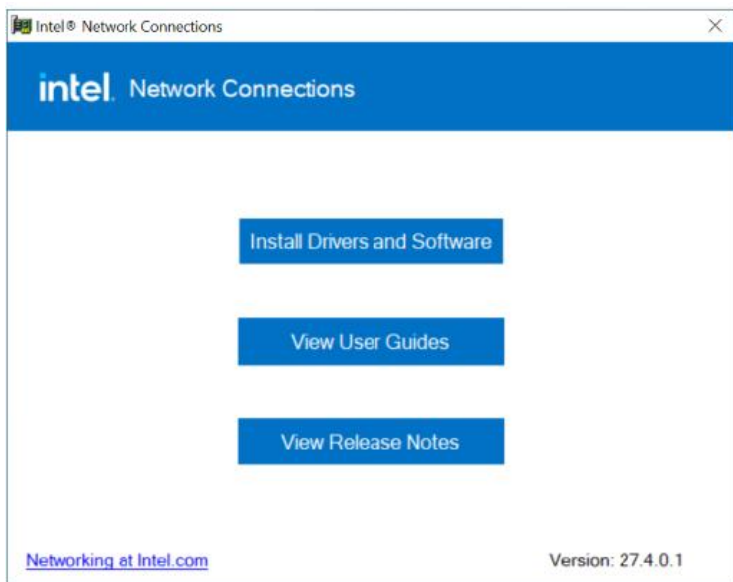
1. Click **Intel** on the left pane and then **Intel(R) AlderLake-P Chipset Drivers** on the right pane.



2. Click **Intel(R) PRO LAN Network Drivers..**



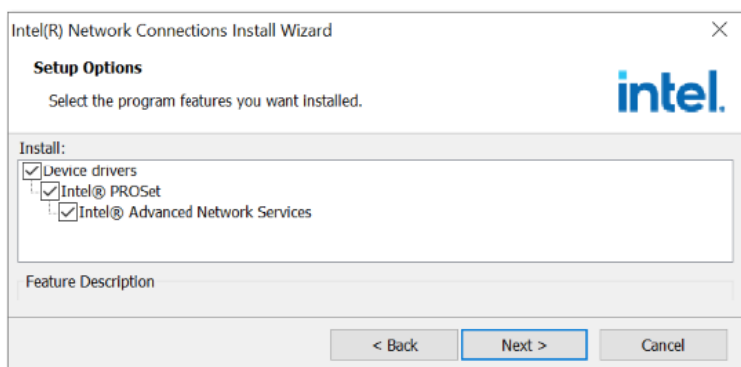
3. Click **Install Drivers and Software**.



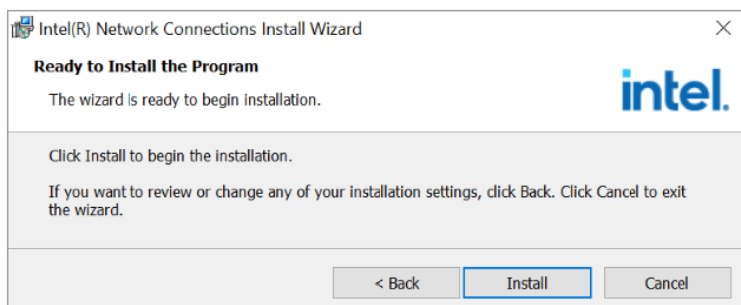
4. On the *Welcome* screen appears, click **Next**.
5. Accept the license agreement and click **Next**.



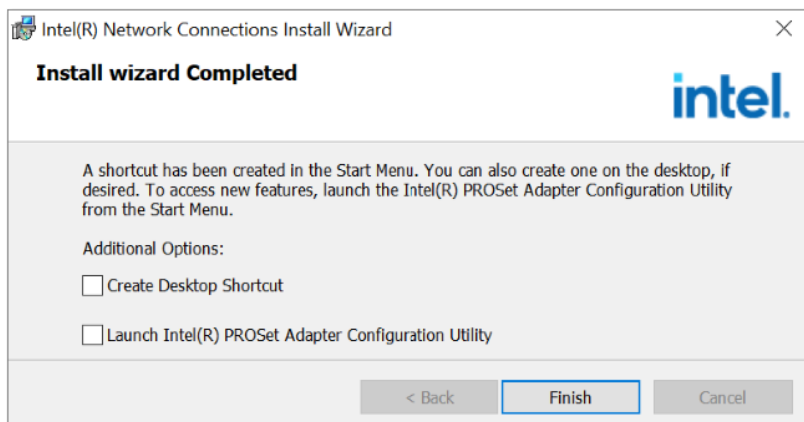
6. In the *Setup Options*, click **Next**.



7. Click **Install**.



8. Install wizard has completed the installation. Click **Finish**.



3.6 Intel® Management Engine Drivers Installation

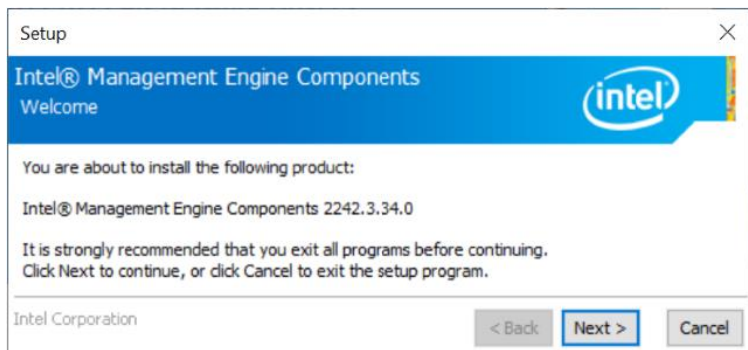
1. Click **Intel** on the left pane and then **Intel(R) AlderLake-P Chipset Drivers** on the right pane.



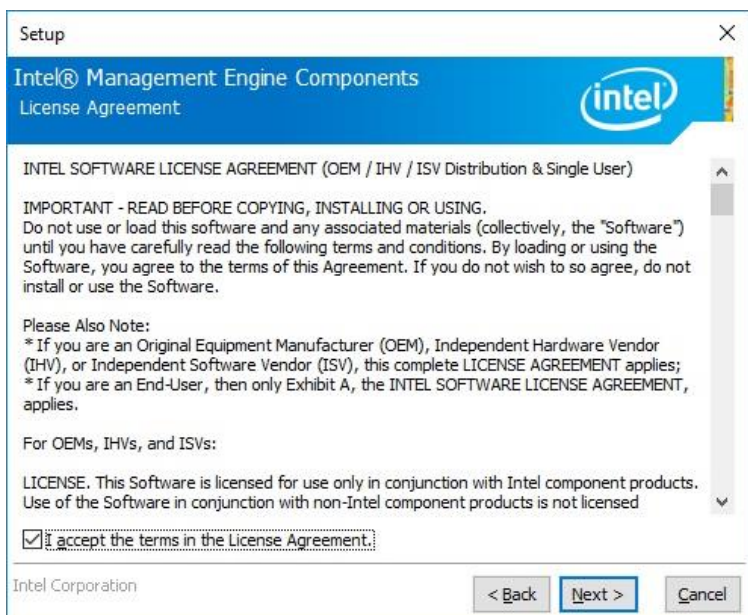
2. Click **Intel(R) ME Drivers**.



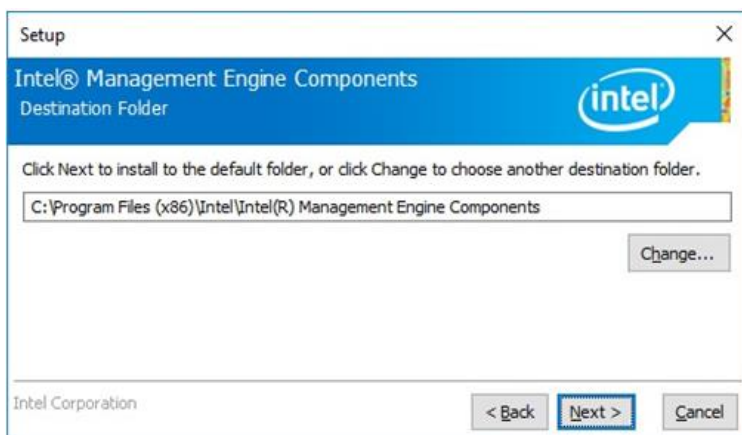
3. When the *Welcome* screen appears, click **Next**.



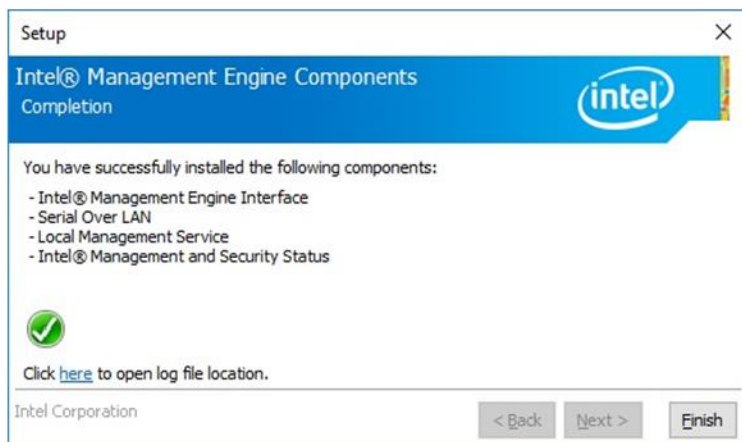
4. Accept the license agreement and click **Next** until the installation starts.



5. Click **Next** to install to the default folder or click **Change** to choose another destination folder.



6. When installation has been completed, click **Finish**.



3.7 Intel® Serial IO Drivers Installation

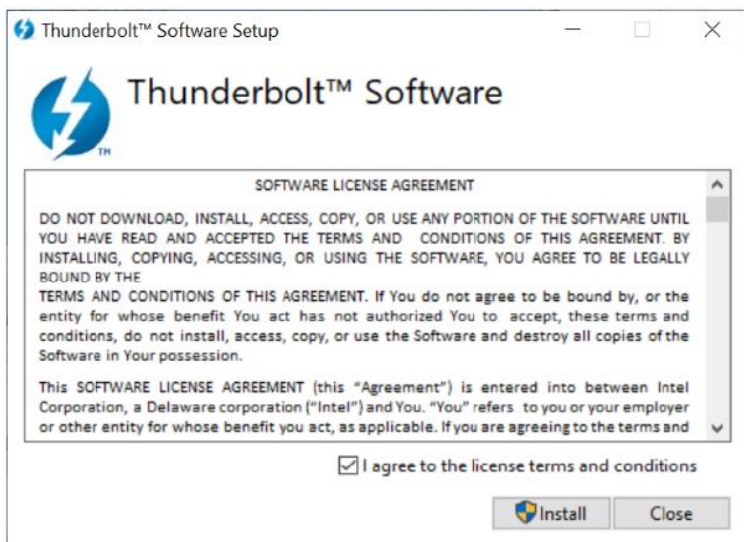
1. Click **Intel** on the left pane and then **Intel(R) AlderLake-P Chipset Drivers** on the right pane.



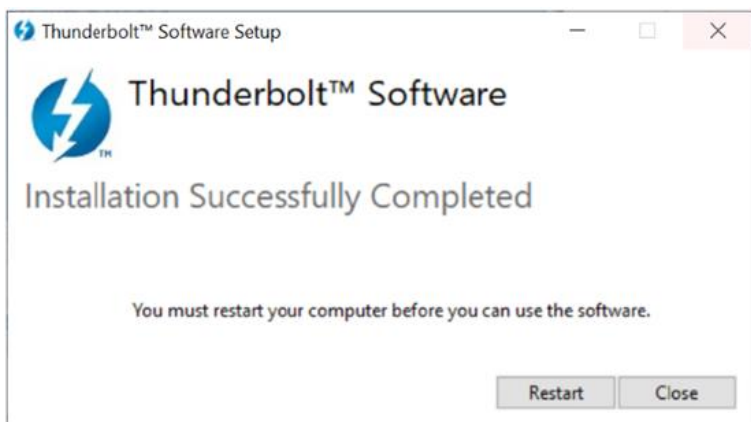
2. Click **Intel(R) Serial IO Drivers**.



3. Agree with the license terms and conditions and click **Install**.



4. Installation has been successfully completed. Click **Restart**.



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Chapter 4

BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

- Main Settings
- Advanced Settings
- Chipset Settings
- Security Settings
- Boot Settings
- Save & Exit

4.1 Introduction

The BIOS (Basic Input/Output System) installed in the ROM of your computer system supports Intel® processors. The BIOS provides critical low-level support for standard devices such as disk drives, serial ports and parallel ports. It also provides password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

4.2 BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Press the key immediately allows you to enter the Setup utility. If you are a little bit late pressing the key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup.

If you still need to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again.

The following message will appear on the screen:

```
Press <DEL> to Enter Setup
```

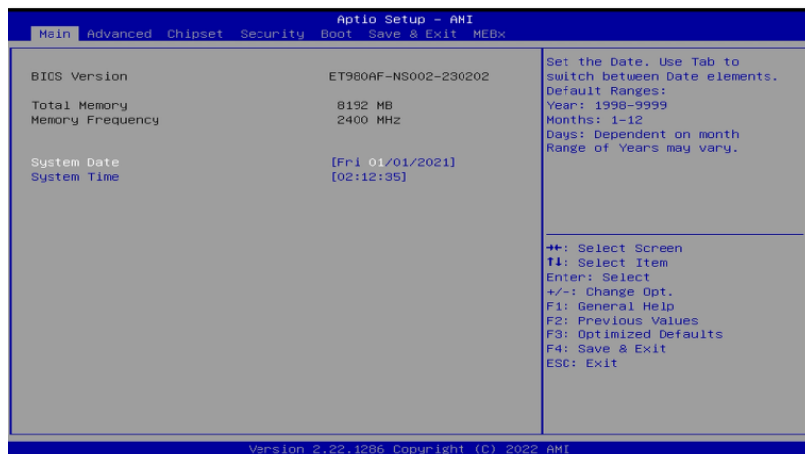
In general, press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help, and <Esc> to quit.

When you enter the BIOS Setup utility, the *Main Menu* screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: It is strongly recommended that you avoid making any changes to the chipset defaults.

These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could make the system unstable and crash in some cases.

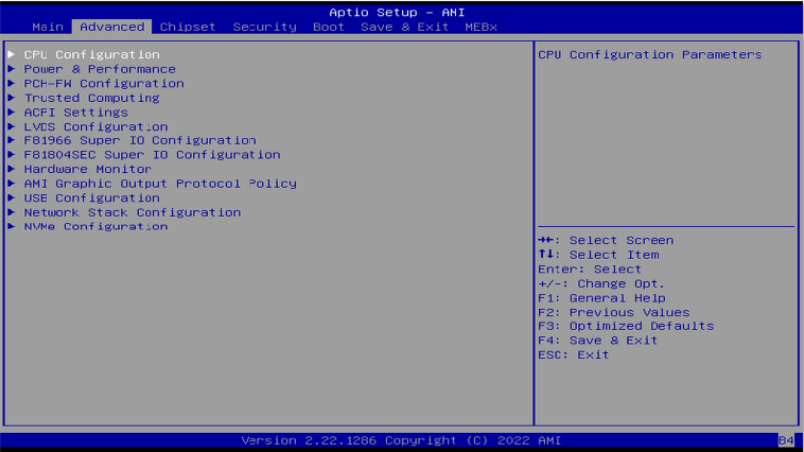
4.3 Main Settings



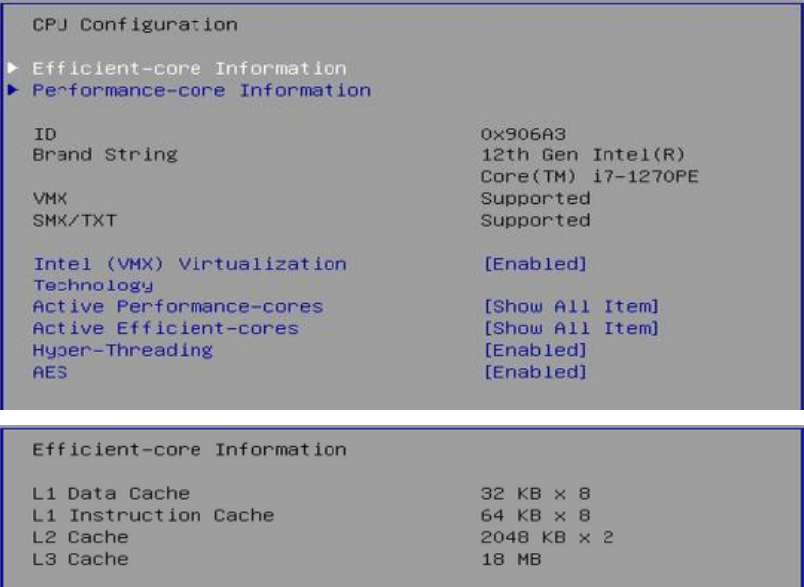
BIOS Setting	Description
System Language	Choose the system default language.
System Date	Sets the date. Use the <Tab> key to switch between the date elements.
System Time	Set the time. Use the <Tab> key to switch between the time elements.

4.4 Advanced Settings

This section allows you to configure, improve your system and allows you to set up some system features according to your preference.



4.4.1 CPU Configuration



Performance-core Information	
L1 Data Cache	48 KB × 4
L1 Instruction Cache	32 KB × 4
L2 Cache	1280 KB × 4
L3 Cache	18 MB

CPU Configuration		Number of P-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together. When both are {0,0}, Pcode will enable all cores.
▶ Efficient-core Information		
▶ Performance-core Information		
ID	0x906A3	
Brand String	12th Gen Intel(R) Core(TM) i7-1270PE Supported	
VMX		
SMX/TXT		
Intel (VMX) Virtualization Technology		
Active Performance-cores		
Active Efficient-cores		

Active Performance-cores

Show All Item

3

2

1

: Select Screen

Active Performance-cores	
Show All Item	
3	
2	
1	

CPU Configuration		Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together. When both are [0,0], Pcode will enable all cores.
▶ Efficient-core Information		
▶ Performance-core Information		
ID	0x906A3	
Brand String	12th Gen Intel(R)	
	Active Efficient-cores	
VMX	Show All Item	
SMX/TXT	7	
	6	
	5	
	4	
	3	
	2	
	1	
	0	
Intel (VMX) Virtualization Technology		
Active Performance-cores		
Active Efficient-cores		
Hyper-Threading		
AES		

⌘: Select Screen
⌘: Select Item
Enter: Select
/=: Change Opt.
F1: Command Help

Active Efficient-cores	
Show All Item	
7	
6	
5	
4	
3	
2	
1	
0	

BIOS Setting	Description
Efficient-core Information	Displays the E-core Information
Performance-core Information	Displays the P-core Information
Intel (VMX) Virtualization Technology	Enables / Disables a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
Intel (VMX) Virtualization Technology	Enables / Disables a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
Active Performance-Cores	Number of cores to enable in each processor package. Options: 3, 2, 1
Active Efficient-cores	Number of cores to enable in each processor package. Options: 7, 6, 5, 4, 3, 2, 1
Hyper-Threading	Enables / Disables Hyperthreading Technology.
AES	Enables / Disables AES (Advanced Encryption Standard).

4.4.2 Power & Performance

Advanced

Aptio Setup - AMI

Power & Performance

▶ CPU - Power Management Control

CPU - Power Management Control Options

⬆⬆: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.22.1286 Copyright (C) 2022 AMI

CPU - Power Management Control

Intel(R) SpeedStep(tm) [Enabled]
Intel(R) Speed Shift Technology [Enabled]
▶ Config TDP Configurations

Allows more than two frequency ranges to be supported.

CPU - Power Management Control

Intel(R) SpeedStep(tm) [Enabled]
Intel(R) Speed Shift Technology [Enabled]
▶ Config TDP Configurations

Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.

CPU - Power Management Control

Intel(R) SpeedStep(tm) [Enabled]
Intel(R) Speed Shift Technology [Enabled]
▶ Config TDP Configurations

Configurable Processor Base Power (cTDP) Configurations

Config TDP Configurations

Configurable TDP Boot Mode [Nominal]
Power Limit 1 28.0W (MSR:28.0)
Power Limit 2 64.0W (MSR:64.0)

Configurable Processor Base Power (cTDP) Mode as Nominal/Level1/Level2/Deactivate TDP selection. Deactivate option will set MSR to Nominal and MPIO to Zero.

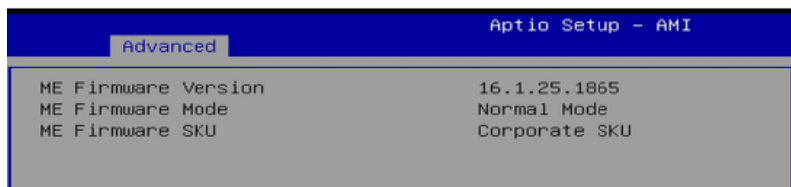
Configurable TDP Boot Mode

Nominal
Down
Up

Select Screen
Select Item

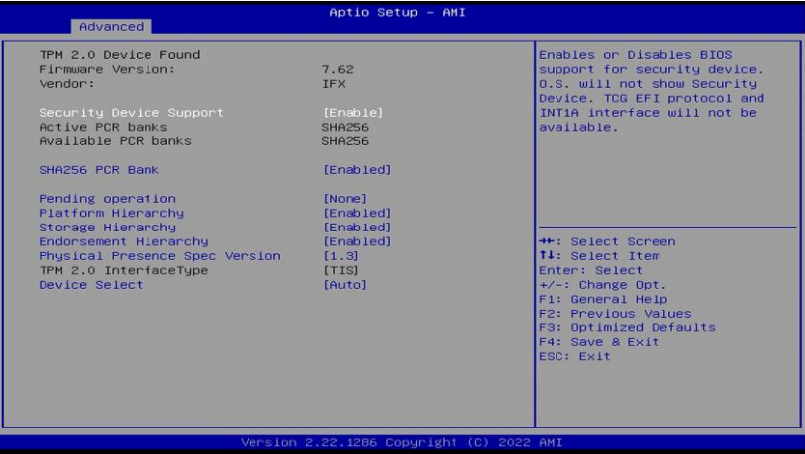
BIOS Setting	Description
Intel(R) SpeedStep(tm)	Allows more than two frequency ranges to be supported.
Intel(R) Speed Shift Technology	Enables / Disables Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.
Config TDP Configurations	Configurable Processor Base Power (cTDP) Configurations
Configurable TDP Boot Mode	Configurable Processor Base Power (cTDP) Mode as Nominal/Level/Level2/Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero.

4.4.3 PCH-FW Configuration



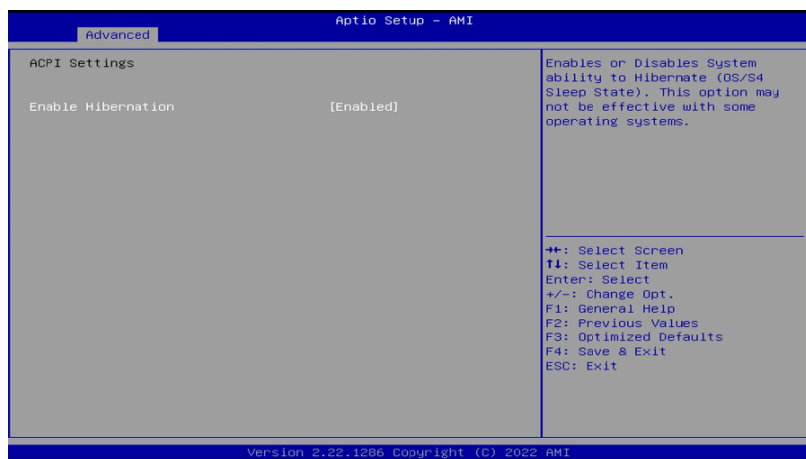
Displays the information of PCH firmware, such as the firmware version, mode, and SKU.

4.4.3.1. Trusted Computing



BIOS Setting	Description
Security Device Support	Enables / Disables BIOS support for security device. OS will not show security device. TCG EFI protocol and INT1A interface will not be available.
SHA256 PCR Bank	Enables / Disables SHA256 PCR Bank.
Pending operation	Schedule an operation for the security device. Note: Your computer will reboot during restart in order to change state of security device.
Platform Hierarchy	Enables / Disables platform hierarchy.
Storage Hierarchy	Enables / Disables storage hierarchy.
Endorsement Hierarchy	Enables / Disables endorsement hierarchy.
Physical Presence Spec Version	Selects to show the PPI Spec Version (1.2 or 1.3) that the OS supports. Note: Some HCK tests might not support 1.3.
Device Select	<ul style="list-style-type: none"> TPM 1.2 will restrict support to TPM 1.2 devices only. TPM 2.0 will restrict support to TPM 2.0 devices only. Auto will support both with the default being set to TPM 2.0 deices if not found, and TPM 1.2 device will be enumerated.

4.4.4 ACPI Settings



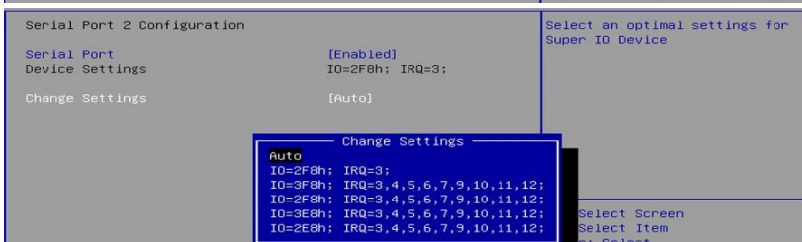
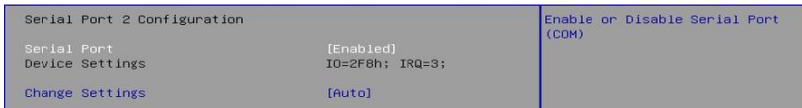
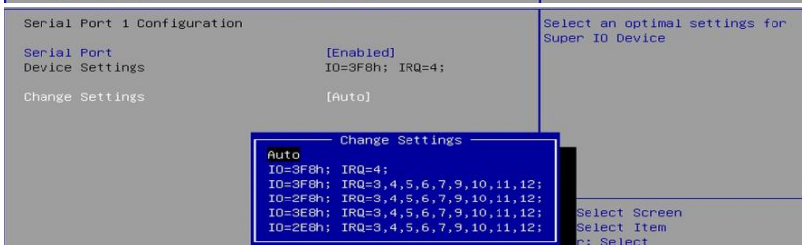
BIOS Setting	Description
Enable Hibernation	Enables / Disables the system ability to hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

4.4.5 LVDS Configuration



BIOS Setting	Description
LVDS Control	Enabled / Disabled
Panel Color Depth	18 BIT / 24 BIT
LVDS Channel Type	Single / Dual
Panel Type	Options: 800 x 480 / 800 x 600 / 1024 x 768 / 1280 x 768 / 1280 x 960 / 1280 x 1024 / 1366 x 768 / 1440 x 900 / 1600 x 900 / 1600 x 1200 / 1680 x 1050 / 1920 x 1080 / 1920 x 1200
LVDS Backlight Control	Options: 0 (Min) ~ 7 (Max)

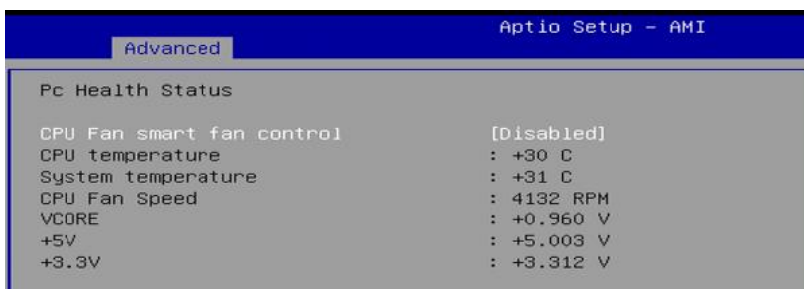
4.4.6 F81966 Super IO Configuration



4.4.7 F81804SEC Super IO Configuration

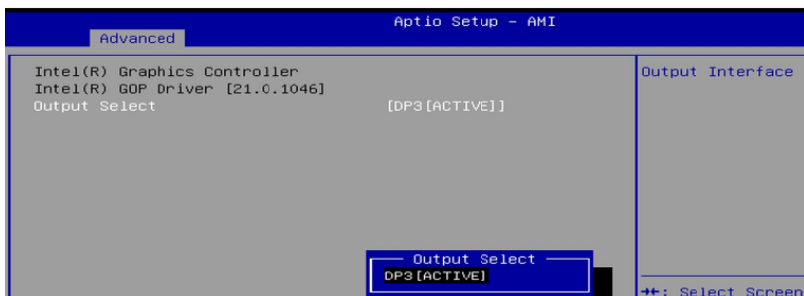
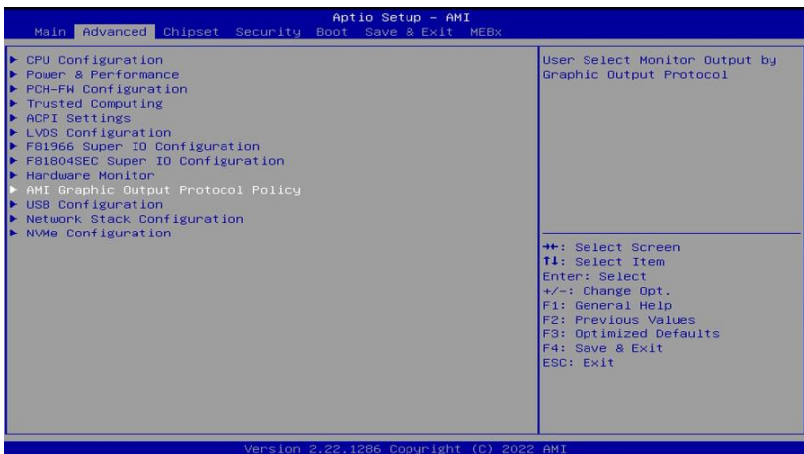
Aptio Setup - AMI	
<div>Advanced</div> <div>F81804SEC Super IO Configuration</div> <div> Super IO Chip F81804SEC ▶ Serial Port 1 Configuration ▶ Serial Port 2 Configuration </div> <div>Set Parameters of Serial Port 1 (COMA)</div>	
<div>Serial Port 1 Configuration</div> <div> Serial Port [Enabled] Device Settings IO=240h; IRQ=10; Change Settings [Auto] </div>	<div>Enable or Disable Serial Port (COM)</div>
<div>Serial Port 1 Configuration</div> <div> Serial Port [Enabled] Device Settings IO=240h; IRQ=10; Change Settings [Auto] </div>	<div>Select an optimal settings for Super IO Device</div>
<div>Change Settings</div> <div> Auto IO=240h; IRQ=10; IO=240h; IRQ=3,4,5,6,7,10,11,12; IO=248h; IRQ=3,4,5,6,7,10,11,12; </div>	<div>Select Screen Select Item</div>
<div>Serial Port 2 Configuration</div> <div> Serial Port [Enabled] Device Settings IO=248h; IRQ=11; Change Settings [Auto] Change Settings [Disable IR1 function] </div>	<div>Enable or Disable Serial Port (COM)</div>
<div>Serial Port 2 Configuration</div> <div> Serial Port [Enabled] Device Settings IO=248h; IRQ=11; Change Settings [Auto] Change Settings [Disable IR1 function] </div>	<div>Select an optimal settings for Super IO Device</div>
<div>Change Settings</div> <div> Auto IO=248h; IRQ=10; IO=240h; IRQ=3,4,5,6,7,10,11,12; IO=248h; IRQ=3,4,5,6,7,10,11,12; </div>	<div>Select Screen Select Item</div>
<div>Serial Port 2 Configuration</div> <div> Serial Port [Enabled] Device Settings IO=248h; IRQ=11; Change Settings [Auto] Change Settings [Disable IR1 function] </div>	<div>Select an optimal settings for Super IO Device</div>
<div>Change Settings</div> <div> Disable IR1 function Enable IR1 function, active pulse 1.6uS Enable IR1 function, active pulse 3/16 bit time </div>	<div>Screen</div>

4.4.8 Hardware Monitor



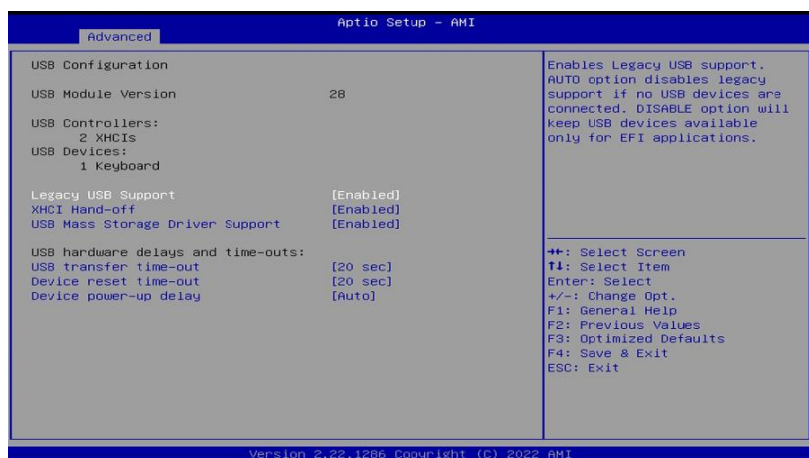
Displays the information of the computer health status.

4.4.9 AMI Graphic Output Protocol Policy



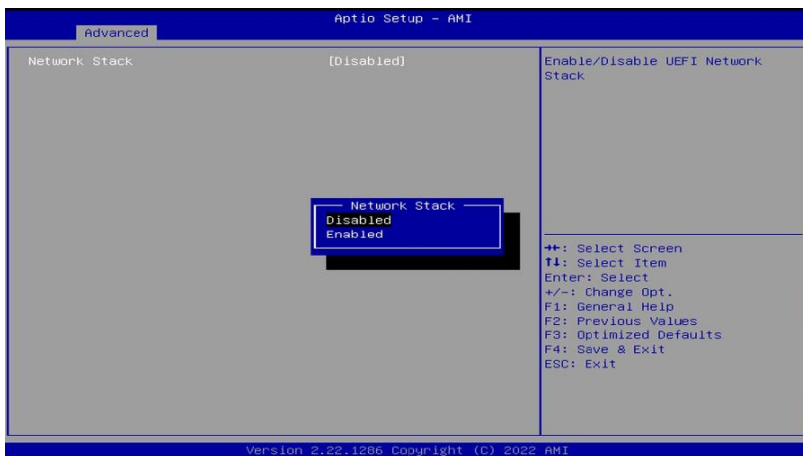
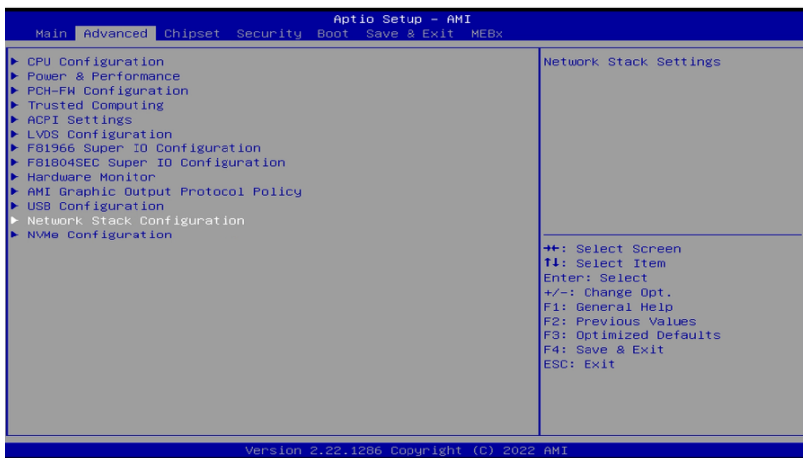
User Select Monitor Output by Graphic Output Protocol.

4.4.10 USB Configuration

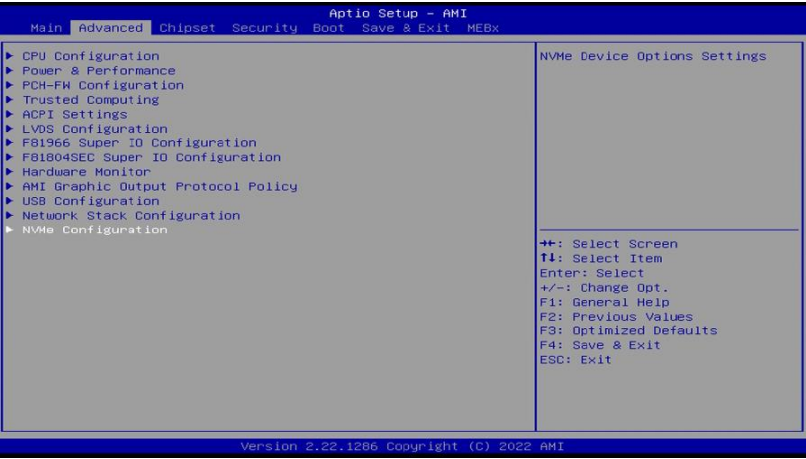


BIOS Setting	Description
Legacy USB Support	<ul style="list-style-type: none"> • Enabled enables Legacy USB support. • Auto disables legacy support if there is no USB device connected. • Disabled keeps USB devices available only for EFI applications.
XHCI Hand-off	This is a workaround for OSeS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enables / Disables the support for USB mass storage driver.
USB Transfer time-out	The time-out value (1 / 5 10 / 20 secs) for Control, Bulk, and Interrupt transfers.
Device reset time-out	Gives seconds (10 / 20 / 30 / 40 secs) to delay execution of Start Unit command to USB mass storage device.
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. "Auto" uses default value: for a root port it is 100 ms, for a hub port, the delay is taken from hub descriptor.

4.4.11 Network Stack Configuration



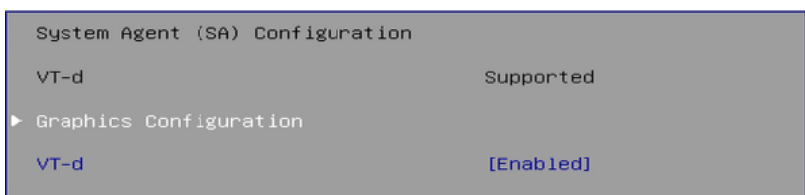
4.4.12 NVMe Configuration



4.5 Chipset Settings

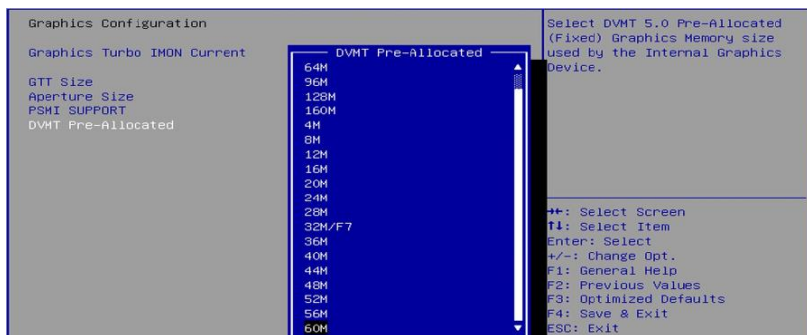
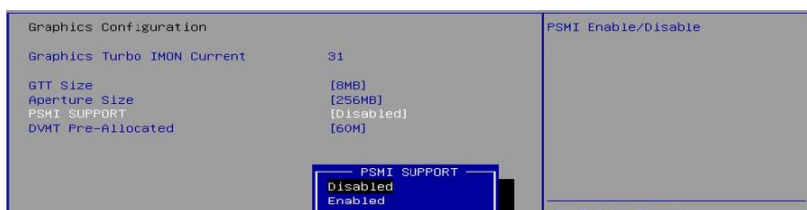
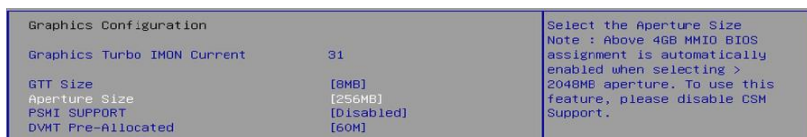
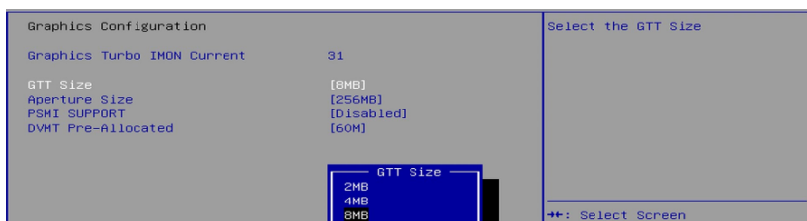


4.5.1 System Agent (SA) Configuration



BIOS Setting	Description
Memory Configuration	Memory Configuration Parameters
VT-d	Enables / Disables VT-d capability.

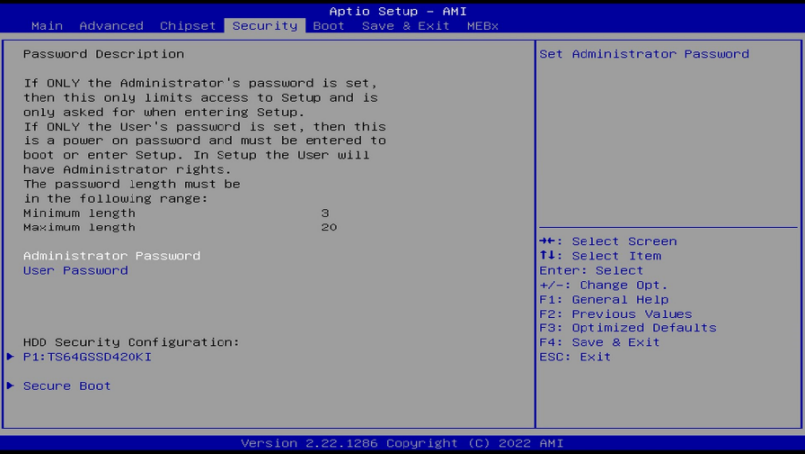
Graphics Configuration	Graphics turbo IMON current values supported (14-31)
Graphics Turbo IMON Current	31
GTT Size	[9MB]
Aperture Size	[256MB]
PSH1 SUPPORT	[Disabled]
DVMT Pre-Allocated	[60M]



PCH-IO Configuration

Aptio Setup - AMI		
Main	Advanced	Chipset
Security	Boot	Save & Exit
MEBx		
▶ System Agent (SA) Configuration ▶ PCH-IO Configuration		PCH Parameters
PCH-IO Configuration ▶ SATA Configuration PCH LAN Controller No GbE Region State After G3 [S0 State]		SATA Device Options Settings
SATA Configuration SATA Controller(s) [Enabled] Serial ATA Port 0 Empty Software Preserve Unknown Hot Plug [Disabled] Serial ATA Port 1 TS64GSSD420KI (64.0GB) Software Preserve SUPPORTED Hot Plug [Disabled] Serial ATA Port 2 Empty Software Preserve Unknown Hot Plug [Disabled]		Enable/Disable SATA Device.
PCH-IO Configuration ▶ SATA Configuration PCH LAN Controller No GbE Region State After G3 [S0 State]		Specify what state to go to when power is re-applied after a power failure (G3 state).
State After G3 S0 State S5 State		** Select Screen

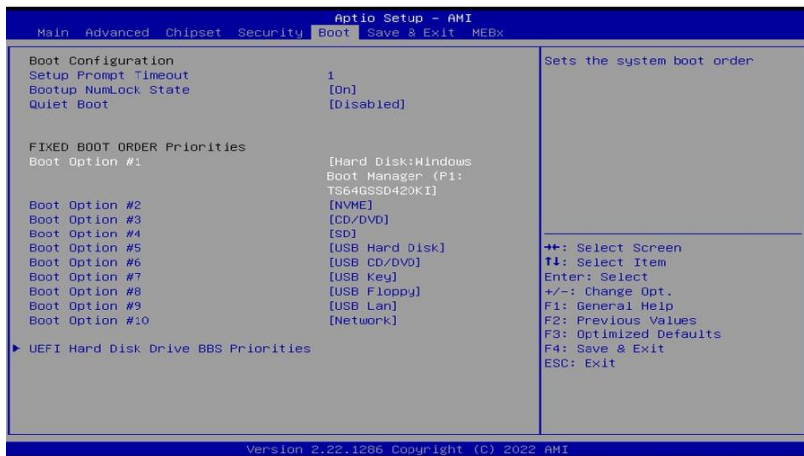
4.6 Security Settings



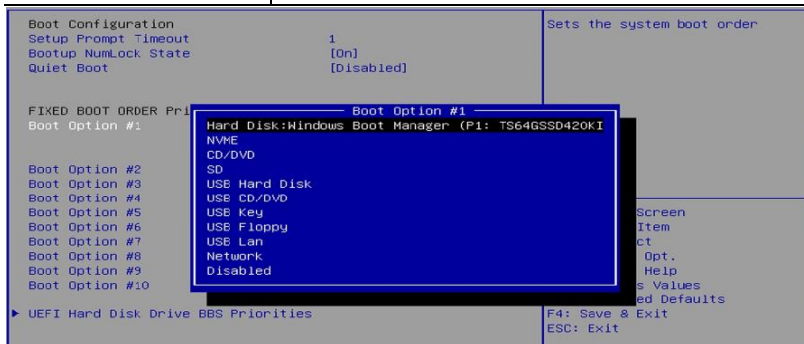
BIOS Setting	Description
Administrator Password	Sets an administrator password for the setup utility.
User Password	Sets a user password.
Secure Boot	Secure boot feature is Active if Secure Boot is enabled. Platform Key(PK) is enrolled and the system is in user mode. The mode change requires platform reset.



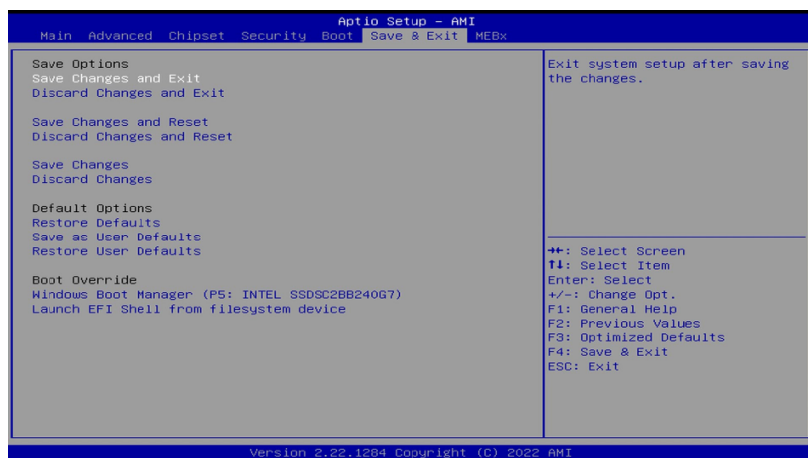
4.7 Boot Settings



BIOS Setting	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	Selects the keyboard NumLock state.
Quiet Boot	Enables / Disables Quiet Boot option.
Boot mode select	Selects a Boot mode, Legacy / UEFI.
Boot Option Priorities	Sets the system boot order priorities.



4.8 Save & Exit Settings



BIOS Setting	Description
Save Changes and Exit	Exits system setup after saving the changes.
Discard Changes and Exit	Exits system setup without saving any changes.
Save Changes and Reset	Resets the system after saving the changes.
Discard Changes and Reset	Resets system setup without saving any changes.
Save Changes	Saves changes done so far to any of the setup options.
Discard Changes	Discards changes done so far to any of the setup options.
Restore Defaults	Restores / Loads defaults values for all the setup options.
Save as User Defaults	Saves the changes done so far as User Defaults.
Restore User Defaults	Restores the user defaults to all the setup options.

Appendix

This section covers the following topics:

- A. I/O Port Address Map
- B. Interrupt Request Lines (IRQ)
- C. Watchdog Timer Configuration

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x00000A00-0x00000A0F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000A20-0x00000A2F	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x0000FFF8-0x0000FFFF	Intel(R) Active Management Technology - SOL (COM5)
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller

Address	Device Description
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x00003000-0x0000303F	Intel(R) UHD Graphics
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000240-0x00000247	Communications Port (COM3)
0x00000248-0x0000024F	Communications Port (COM4)
0x00000000-0x00000CF7	PCI Express Root Complex
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x0000EFA0-0x0000EFBF	Intel(R) SMBus - 51A3
0x00002000-0x000020FE	Motherboard resources
0x00003090-0x00003097	Standard SATA AHCI Controller
0x00003080-0x00003083	Standard SATA AHCI Controller
0x00003060-0x0000307F	Standard SATA AHCI Controller
0x00001854-0x00001857	Motherboard resources

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 4294967294	Intel(R) PCI Express Root Port #9 - 51B0
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INTC1055
IRQ 4294967271~83	Intel(R) Ethernet Controller I226-LM
IRQ 19	Intel(R) Active Management Technology - SOL (COM5)
IRQ 4294967289~91	PCI Express Downstream Switch Port
IRQ 4294967287	Intel(R) UHD Graphics
IRQ 4294967284	Intel(R) Management Engine Interface #1
IRQ 4294967292	PCI Express Downstream Switch Port
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 10	Communications Port (COM3)
IRQ 11	Communications Port (COM4)
IRQ 4294967286	Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967270	Intel® Smart Sound Technology BUS
IRQ 0	System timer
IRQ 55 ~ IRQ 204	Microsoft ACPI-Compliant System
IRQ 256 ~ IRQ511	Microsoft ACPI-Compliant System
IRQ 41	Trusted Platform Module 2.0
IRQ 4294967293	Intel(R) PCI Express Root Port #10 - 51B1
IRQ 4294967288	Standard SATA AHCI Controller
IRQ 4294967285	Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)

C. Watchdog Timer Configuration

The Watchdog Timer (WDT) is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven.

Under normal circumstance, you will need to restart the WDT at regular intervals before the timer counts to zero.

1. Sample Code:

```
//-----
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81804.H"
//-----
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//-----
int main (int argc, char *argv[])
{
    unsigned char bBuf;
    unsigned char bTime;
    char **endptr;

    char SIO;

    printf("Fintek 81804 watch dog program\n");
    SIO = Init_F81804();
    if (SIO == 0)
    {
        printf("Can not detect Fintek 81804, program abort.\n");
        return(1);
    }
    if (SIO == 0)

    if (argc != 2)
    {
        printf("Parameter incorrect!!\n");
        return (1);
    }
}
```

```

bTime = strtol(argv[1], endptr, 10);
printf("System will reset after %d seconds\n", bTime);

if (bTime)
{
    EnableWDT(bTime);
}
else
{
    DisableWDT();
}
return 0;
}

//-----
void EnableWDT(int interval)
{
    unsigned char bBuf;

    bBuf = Get_F81804_Reg(0x2B);
    bBuf &= (~0x20);
    Set_F81804_Reg(0x2B, bBuf);           //Enable WDTO

    Set_F81804_LD(0x07);                  //switch to logic device 7
    Set_F81804_Reg(0x30, 0x01);           //enable timer

    bBuf = Get_F81804_Reg(0xF5);
    bBuf &= (~0x0F);
    bBuf |= 0x52;
    Set_F81804_Reg(0xF5, bBuf);           //count mode is second

    Set_F81804_Reg(0xF6, interval);        //set timer

    bBuf = Get_F81804_Reg(0xFA);
    bBuf |= 0x01;
    Set_F81804_Reg(0xFA, bBuf);           //enable WDTO output

    bBuf = Get_F81804_Reg(0xF5);
    bBuf |= 0x20;
    Set_F81804_Reg(0xF5, bBuf);           //start counting
}

//-----
void DisableWDT(void)
{
    unsigned char bBuf;

    Set_F81804_LD(0x07);                  //switch to logic device 7

    bBuf = Get_F81804_Reg(0xFA);
    bBuf &= ~0x01;
    Set_F81804_Reg(0xFA, bBuf);           //disable WDTO output

    bBuf = Get_F81804_Reg(0xF5);
    bBuf &= ~0x20;
    bBuf |= 0x40;
    Set_F81804_Reg(0xF5, bBuf);           //disable WDT
}

//-----

//-----
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY

```

```

// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----
#include "F81804.H"
#include <dos.h>
//-----
unsigned int F81804_BASE;
void Unlock_F81804 (void);
void Lock_F81804 (void);
//-----
unsigned int Init_F81804(void)
{
    unsigned int result;
    unsigned char ucDid;

    F81804_BASE = 0x4E;
    result = F81804_BASE;

    ucDid = Get_F81804_Reg(0x20);
    if (ucDid == 0x07) //Fintek 81804
    {
        goto Init_Finish;
    }

    F81804_BASE = 0x2E;
    result = F81804_BASE;

    ucDid = Get_F81804_Reg(0x20);
    if (ucDid == 0x07) //Fintek 81804
    {
        goto Init_Finish;
    }

    F81804_BASE = 0x00;
    result = F81804_BASE;

Init_Finish:
    return (result);
}
//-----
void Unlock_F81804 (void)
{
    outputb(F81804_INDEX_PORT, F81804_UNLOCK);
    outputb(F81804_INDEX_PORT, F81804_UNLOCK);
}
//-----
void Lock_F81804 (void)
{
    outputb(F81804_INDEX_PORT, F81804_LOCK);
}
//-----
void Set_F81804_LD( unsigned char LD)
{
    Unlock_F81804();
    outputb(F81804_INDEX_PORT, F81804_REG_LD);
    outputb(F81804_DATA_PORT, LD);
    Lock_F81804();
}
//-----

```

```
void Set_F81804_Reg( unsigned char REG, unsigned char DATA)
```

```
{
    Unlock_F81804();
    outportb(F81804_INDEX_PORT, REG);
    outportb(F81804_DATA_PORT, DATA);
    Lock_F81804();
}
//-----
unsigned char Get_F81804_Reg(unsigned char REG)
{
    unsigned char Result;
    Unlock_F81804();
    outportb(F81804_INDEX_PORT, REG);
    Result = inportb(F81804_DATA_PORT);
    Lock_F81804();
    return Result;
}
//-----
```

```
//-----
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----
#ifndef F81804_H
#define F81804_H 1
//-----
#define F81804_INDEX_PORT (F81804_BASE)
#define F81804_DATA_PORT (F81804_BASE+1)
//-----
#define F81804_REG_LD 0x07
//-----
#define F81804_UNLOCK 0x87
#define F81804_LOCK 0xAA
//-----
unsigned int Init_F81804(void);
void Set_F81804_LD( unsigned char);
void Set_F81804_Reg( unsigned char,
unsigned char); unsigned char
Get_F81804_Reg( unsigned char);
//-----
#endif // F81804_H
```