innodisk

Total Solution For
Industrial Flash Storage

M.2 (P80)

InnoOSR 3TO8

Customer: _____

Customer Part Number: _____

Innodisk Part Number: _____

Innodisk Model Name: _____

Date: _____

Innodisk Approver	Customer Approver

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Features:

- PCIe Gen 3x4, NVMe SSD
- Kioxia 3D TLC NAND
- M.2 2280-D2-M
- iPower Guard
- iData Guard
- Thermal Throttling Management
- Support End-to-End Data Path Protection (ETEP)

Performance:

- Sequential Read up to 3,550 MB/s
- Sequential Write up to 2,700 MB/s

Power Requirements:

Input Voltage:	3.3V±5%
Max Operating Wattage (R/W):	5.8W
Idle Wattage:	0.9W

Reliability:

Capacity	TBW (Client)	DWPD
128GB	86	0.7
256GB	192	0.8
512GB	389	0.8
1TB	905	0.9
2TB	2304	1.2

Data Retention	1 Year
Warranty	3 Years

1 year data retention is at NAND life end.

For warranty details, please refer to:

https://www.innodisk.com/en/support_and_service/warranty

Revision History

Revision	Description	Date
V1.0	First Release	Feb., 2025
V1.1	Update InnoOSR pin define table	Jun., 2025

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1. Product Overview

1.1 Introduction of Innodisk M.2 (P80) 3TO8

Innodisk M.2 (P80) 3TO8 provides high capacity flash memory Solid State Drive (SSD) that electrically complies with PCIe interface and industrial 3D TLC NAND Flash. M.2 (P80) 3TO8 supports PCIe Gen 3 x4 and it is compliant with NVMe 1.4 providing excellent top and also sustained performance. It is designed with AES engine, which is a built in controller. When controller receives the data package from host, AES engine encrypts the data package and saves the encrypted data into NAND flash. Thus, unauthorized personal has no access to decrypt the data in NAND flash.

Besides outstanding balance of performance, rich form factors, capacity and customization flexibility, the key feature of InnoOSR family is the single-device, Firmware LBA level OS & Data back-up capability which enables on-site recovery of operating system by simple procedure such as GPIO triggering or application commands.

*Please note that both NVMe format and Sanitize will erase all disk data, including the backup area.

*Please note that no external storage devices are attached during back up/recovery until power off.

***CAUTION** TRIM must be enabled.*

TRIM enables SSD's controller to skip invalid data instead of moving. It can free up significant amount of resources, extends the lifespan of SSD by reducing erase, and write cycles on the SSD. Innodisk's handling of garbage collection along with TRIM command improves write performance on SSDs.

1.2 Product View and Models

Innodisk M.2 (P80) 3TO8 is available in following capacities with 3D TLC flash ICs.

M.2 (P80) 3TO8 128GB M.2 (P80) 3TO8 256GB M.2 (P80) 3TO8 512GB

M.2 (P80) 3TO8 1TB M.2 (P80) 3TO8 2TB

Figure 1: Innodisk M.2 (P80) 3TO8 (type 2280) with Vertical Pin Headers (PCB version: B)

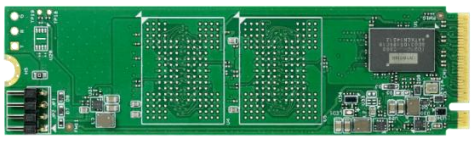


Figure 2: Innodisk M.2 (P80) 3TO8 (type 2280) with Horizontal Pin Headers (PCB version: A)

1.3 PCIe Interface

Innodisk M.2 (P80) 3TO8 supports PCIe Gen 3 interface and compliant with NVMe 1.4. M.2 (P80) 3TO8 can work under PCIe Gen 1, Gen 2 and Gen 3.

Most of operating system includes NVMe in-box driver now. For more information about the driver support in each OS, please visit https://nvmexpress.org/drivers/.

2. Product Specifications

2.1 Capacity and Device Parameters

M.2 (P80) 3TO8 device parameters are shown in Table 1.

Table 1: Device parameters

Note: User capacities vary depend on size of hidden OS back-up area

Capacity	OS back-up capacity (GB)	LBA	User Capacity(GB)
128GB	10	213470128	101.8
	20	192498608	91.8
	30	171527088	81.8
	60	108612528	51.8
256GB	30	405947568	193.5
	60	343033008	163.5
	90	280118448	133.5
512GB	30	874788528	417.1
	60	811873968	387.1
	90	748959408	357.1
1TB	30	1812467888	864.2
	60	1749555888	834.2
	90	1686641328	804.2
2TB	30	3687834288	1758.4
	60	3624919728	1728.4
	90	3562005168	1698.4

2.2 Performance

Burst Transfer Rate: 4 GB/s

Table 2: Performance- 112 Layers 3D TLC

Capacity	Unit	128GB	256GB	512GB	1TB	2TB
Sequential* Read (max.)	MB/s	1,450	3,000	3,550	3,550	3,250
Sequential* Write (max.)		560	1,100	2,250	2,700	2,350
Sustained Sequential Read (Avg.)***		680	990	1,150	1,150	1,100
Sustained Sequential Write (Avg.)***		220	390	660	790	730
4KB Random** Read (Q32T1)	IOPS	52,000	103,000	383,000	494,000	495,000
4KB Random** Write (Q32T1)		122,000	234,000	312,000	323,000	236,000

Note:

* Performance results are measured in Room Temperature with Out-of-Box devices and may vary depending on overall system setup.

** Performance results are based on CrystalDiskMark 8.0.1 with typical tolerances for range from 1% to 10%. Unit of 4KB items is I.O.P.S.

2.3 Electrical Specifications

2.3.1 Power Requirement

Table 3: Innodisk M.2 (P80) 3TO8 Power Requirement

Item	Symbol	Rating	Unit
Input voltage	V_{IN}	+3.3 DC +- 5%	V

2.3.2 Power Consumption

Table 4: Power Consumption

Mode	Power Consumption (W)
Read	5.8
Write	4.7
Idle	0.9
Power on peak	8.2

* Target: M.2 (P80) 3TO8 2TB

Note: Current results may vary depending on system components and power circuit design.

Please refer to the test report for other capacities.

2.4 Environmental Specifications

2.4.1 Temperature Ranges

Table 5: Temperature range for M.2 (P80) 3TO8

Temperature	Range
Operating	Standard Grade: 0°C to +70°C
Storage	-40°C to +85°C

2.4.2 Humidity

Relative Humidity: 10-95%, non-condensing

2.4.3 Shock and Vibration

Table 6: Shock/Vibration Testing for M.2 (P80) 3TO8

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2K Hz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500 G, 3 axes	IEC 68-2-27

2.4.4 Mean Time between Failures (MTBF)

Table 7 summarizes the MTBF prediction results for various M.2 (P80) 3TO8 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 7: M.2 (P80) 3TO8 MTBF

Product	Condition	MTBF (Hours)
Innodisk M.2 (P80) 3TO8	Telcordia SR-332 GB, 25°C	>3,000,000

2.5 CE and FCC Compatibility

M.2 (P80) 3TO8 conforms to CE and FCC requirements.

2.6 RoHS Compliance

M.2 (P80) 3TO8 is fully compliant with RoHS directive.

2.7 Reliability

Table 8: M.2 (P80) 3TO8 TBW

Parameter	Value
Read Cycles	Unlimited Read Cycles
Flash endurance	3,000 P/E cycles
Error Correct Code	Support(LDPC)
Data Retention	Under 40°C: 1 Year at NAND Life End

TBW* (Total Bytes Written) Unit: TB

Capacity	Sequential workload	Client workload
128GB	337	86
256GB	674	192
512GB	1348	389
1TB	2697	905
2TB	5395	2304

* Note:

1. Sequential: Mainly sequential write are estimated by PassMark Burnin Test v8.1 pro.
2. Client: Follow JESD218 Test method and JESD219A Workload, tested by ULINK. (The capacity lower than 64GB client workload is not specified in JEDEC219A, the values are estimated.)
3. Based on out-of-box performance.

2.8 Transfer Mode

M.2 (P80) 3TO8 support following transfer mode:

PCIe Gen 3: 4 GB/s

PCIe Gen 2: 2 MB/s

PCIe Gen 1: 1 MB/s

2.9 Pin Assignment

Innodisk M.2 (P80) 3TO8 follows standard M.2 spec, socket 3 key M PCIe-based SSD pinout. See Table 9 for M.2 (P80) 3TO8 pin assignment.

Table 9: Innodisk M.2 (P80) 3TO8 Pin Assignment

Signal Name	Pin #	Pin #	Signal Name
		75	GND
3.3V	74	73	GND
3.3V	72	71	GND
3.3V	70	69	NC
NC	68	67	NC
Notch	66	65	Notch
Notch	64	63	Notch
Notch	62	61	Notch
Notch	60	59	Notch
NC	58	57	GND
NC	56	55	REFCLKp
NC	54	53	REFCLKn
CLKREQ# (I/O)(0/3.3V)	52	51	GND
PERST# (I)(0/3.3V)	50	49	PERp0
NC (reserved for Input 3.3V for recovery trigger (low active) (GPIO 31))	48	47	PERn0
NC (reserved for Output 3.3V for LED (GPIO 30))	46	45	GND
NC (reserved for ALERT#)	44	43	PETp0
NC (reserved for SMB_DATA)	42	41	PETn0
NC (reserved for SMB_CLK)	40	39	GND
NC	38	37	PERp1
NC	36	35	PERn1
NC	34	33	GND
NC	32	31	PETp1
NC	30	29	PETn1
NC	28	27	GND
NC	26	25	PERp2
NC	24	23	PERn2
NC	22	21	GND
NC	20	19	PETp2
3.3V	18	17	PETn2

3.3V	16	15	GND
3.3V	14	13	PERp3
3.3V	12	11	PERn3
LED1# (O) (OD)	10	9	GND
NC	8	7	PETp3
NC	6	5	PETn3
3.3V	4	3	GND
3.3V	2	1	GND

2.10 Mechanical Dimensions

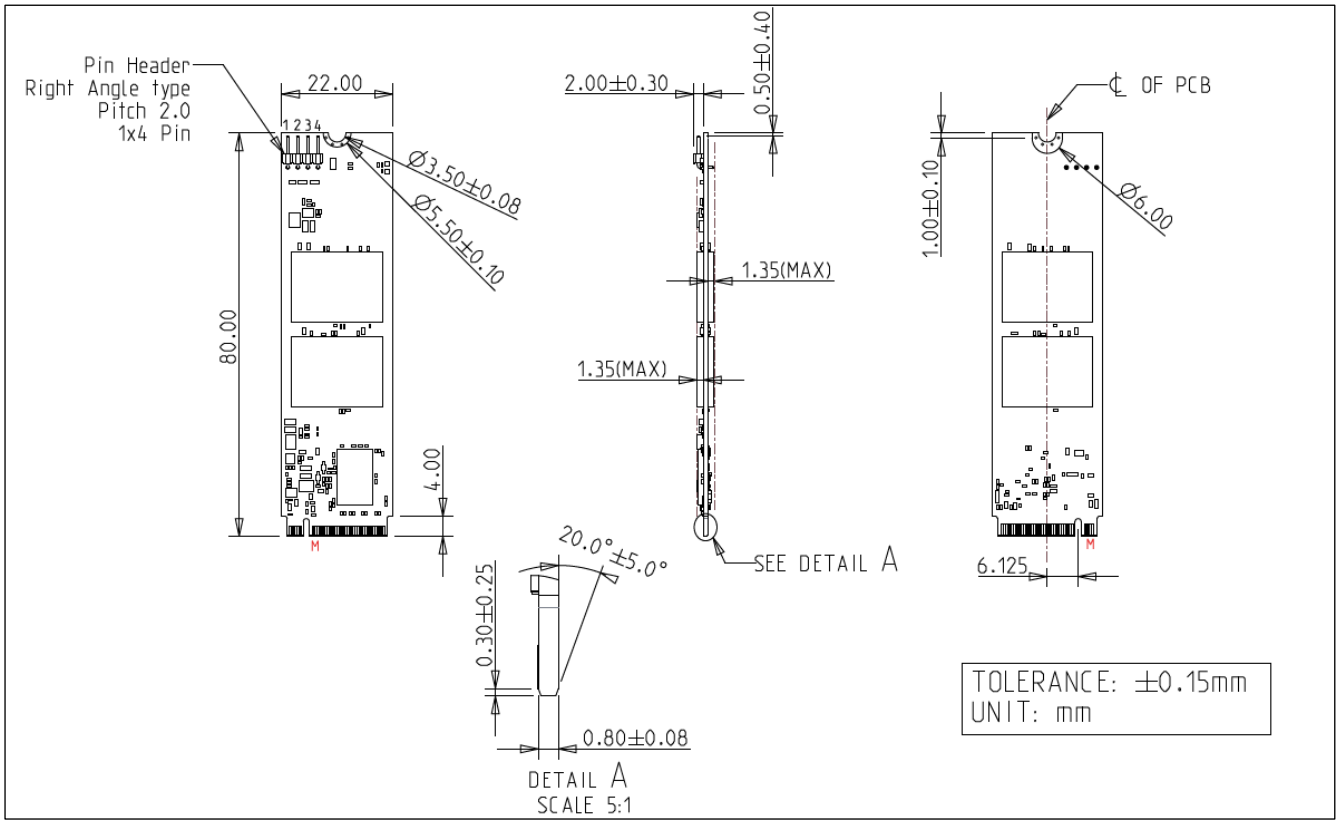


Figure 3: Innodisk M.2 (P80) 3TO8 diagram with Horizontal Pin Headers

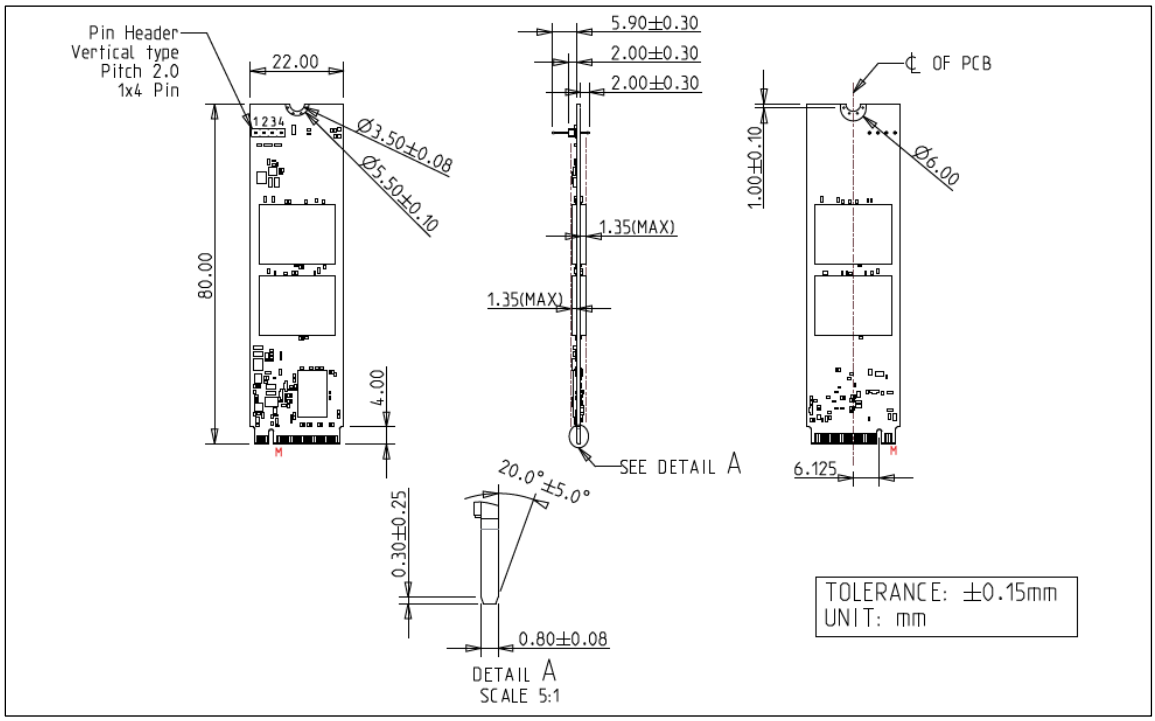


Figure 4: Innodisk M.2 (P80) 3TO8 diagram with Vertical Pin Headers

2.11 Assembly Weight

An Innodisk M.2 (P80) 3TO8 within flash ICs, 128GB's weight is 8 grams approximately.

2.12 Seek Time

Innodisk M.2 (P80) 3TO8 is not a magnetic rotating design. There is no seek or rotational latency required.

3. Theory of Operation

3.1 Overview

Figure 5 shows the operation of Innodisk M.2 (P80) 3TO8 from the system level, including the major hardware blocks.

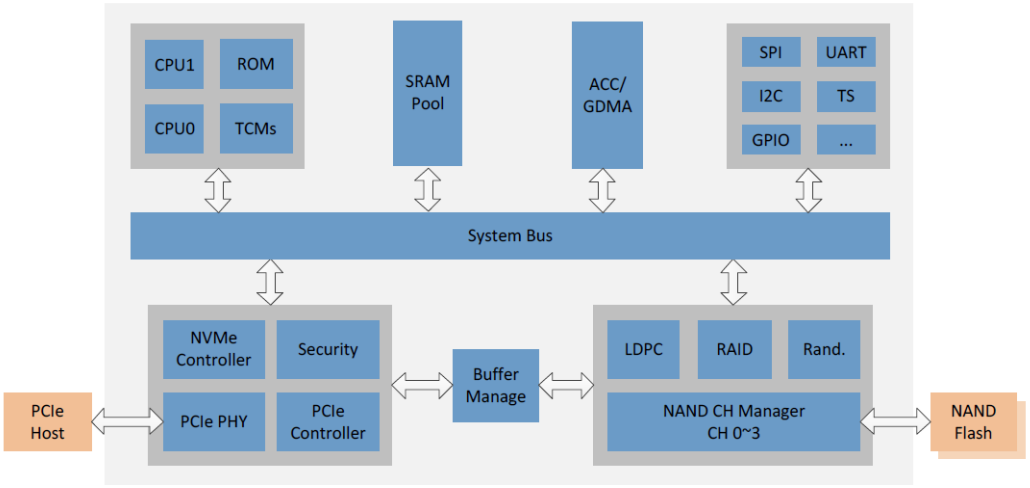


Figure 5: Innodisk M.2 (P80) 3TO8 Block Diagram

Innodisk M.2 (P80) 3TO8 integrates a PCIe Gen 3 x4 controller and NAND flash memories. Communication with the host occurs through the host interface, using the standard NVM protocol. Communication with the flash device(s) occurs through the flash interface.

3.2 PCIe Gen 3 x4 Controller

Innodisk M.2 (P80) 3TO8 is designed with innodisk ID310, a PCIe Gen 3 x4 controller which is compliant with NVMe 1.4, up to 32.0Gbps transfer speed. In addition, it is compliant with PCIe Gen 1, Gen 2 and Gen 3 specification. The controller supports up to four channels for flash interface.

3.3 Error Detection and Correction

Innodisk M.2 (P80) 3TO8 is designed with hardware LDPC ECC engine with hard-decision and soft-decision decoding. Low-density parity-check (LDPC) codes have excellent error correcting performance close to the Shannon limit when decoded with the belief-propagation (BP) algorithm using soft-decision information.

3.4 Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

Innodisk M.2 (P80) 3TO8 uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

3.5 Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SSD is shipped, or may develop during the life time of the SSD. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management, Bad Blocks replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

3.6 iData Guard

Innodisk's iData Guard is a comprehensive data protection mechanism that functions before and after a sudden power outage to SSD. Low-power detection terminates data writing before an abnormal power-off, while table-remapping after power-on deletes corrupt data and maintains data integrity. Innodisk's iData Guard provides effective power cycling management, preventing data stored in flash from degrading with use.

3.7 iPower Guard

iPower Guard technology is a set of preventive measures that protect the SSD in an unstable power supply environment. This comprehensive package comprises safeguards for startup and shutdown to maintain device performance and ensure data integrity.

3.8 Garbage Collection

Garbage collection is used to maintain data consistency and perform continual data cleansing on SSDs. It runs as a background process, freeing up valuable controller resources while sorting good data into available blocks, and deleting bad blocks. It also significantly reduces write operations to the drive, thereby increasing the SSD's speed and lifespan.

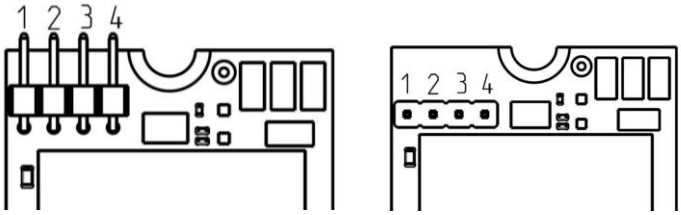
3.9 Trim

The Trim command is designed to enable the operating system to notify the SSD which pages no longer contain valid data due to erases either by the user or operating system itself. During a delete operation, the OS will mark the sectors as free for new data and send a Trim command to the SSD to mark them as not containing valid data. After that the SSD knows not to preserve the contents of the block when writing a page, resulting in less write amplification with fewer writes to the flash, higher write speed, and increased drive life.

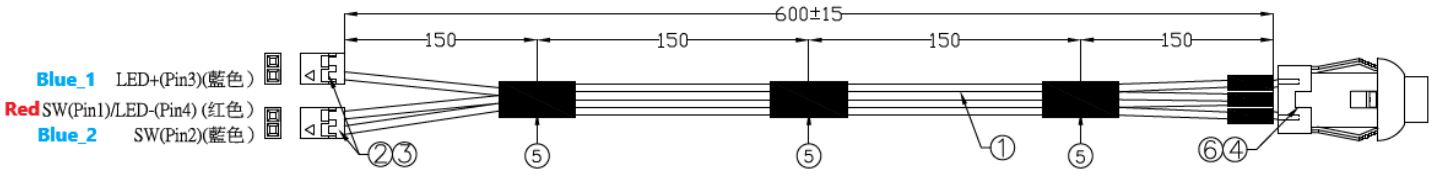
3.10 Die RAID

Die RAID is a controller function which leveraged user capacity to back up the data in NAND flash. Die RAID supported can ensure the user data in the NAND Flash more consistent in certain scenario. Innodisk M.2 (P80) 3TO8 series is default enable the Die RAID function for the industrial application.

3.11 InnoOSR Back-up/Recovery



Pin Header Number	Pin Define	Installation for Innodisk Demo Cable (PN: 7W3000000920)	Rating
1	Power	NA	3.3V ± 5%
2	GPIO Pin30, Output for InnoOSR LED indication	Blue cable_1	3.3V ± 5%
3	GND	Red	NA
4	GPIO Pin31, Input for InnoOSR Recovery Trigger, Low active	Blue cable_2	3.3V ± 5%



3.11.1 InnoOSR Back-up Implementation Process

Process of InnoOSR Back-up / Recovery can be found in Independent "Innodisk InnoOSR Implementation Process" document.

3.11.2 InnoOSR Recovery Triggering Methods

There are two methods to trigger OS recovery process listed as follows:

Button triggering: With Pin3 & 4 of the 1 x 4 pin headers located on the end of M.2 PCB shorted for more than 5 seconds, the recovery process will start. Back-up image of which this process leads to can be established by our InnoOSR software tool.

Software triggering: Our InnoOSR software tool can also trigger the recovery process. However, due to the recovery process itself essentially means covering your operating OS up, you may experience system crash and progress bar can only be read via LED signal linked directly to InnoOSR device.

3.11.3 InnoOSR LED Indicator

- Recovery on process: Light flashing
- Recovery finish: Light on

4. Installation Requirements

4.1 M.2 (P80) 3TO8 Pin Directions

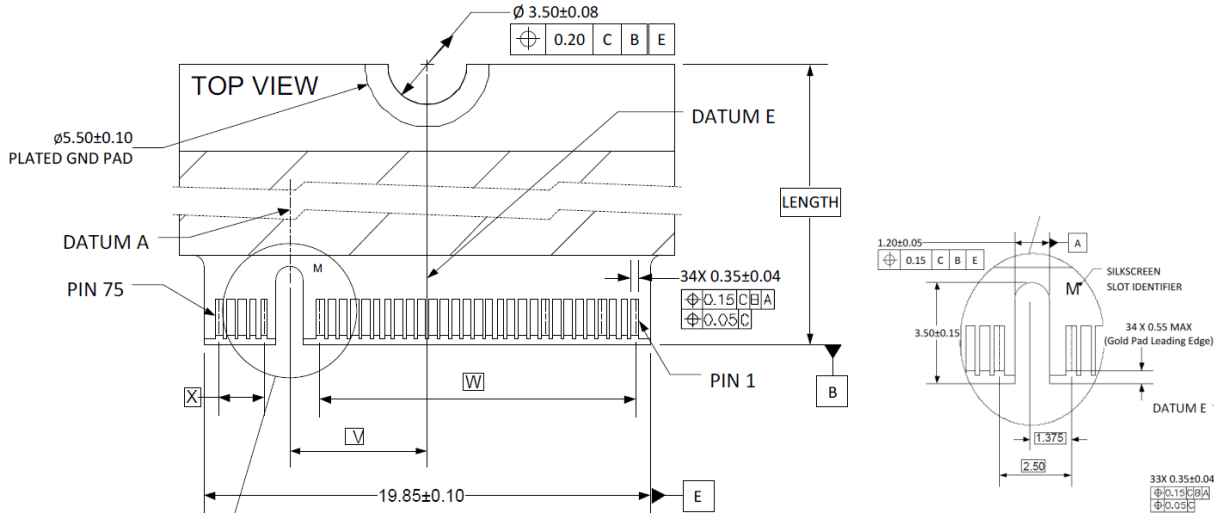


Figure 6: Signal Segment and Power Segment

4.2 Electrical Connections for M.2 (P80) 3TO8

M.2 interconnect is based on a 75 position Edge Card connector. The 75 position connector is intended to be keyed so as to distinguish between families of host interfaces and the various Sockets used in general Platforms. M.2 (P80) 3TO8 is compliant with M.2 Socket 3 key M.

4.3 Device Drive

M.2 (P80) 3TO8 is compliant with NVMe 1.4. Both Operation System and BIOS should include NVMe driver to compatible with NVMe device. Nowadays, most of OS includes NVMe in-box driver now. For more information about the driver support in each OS, please visit the website https://nvmexpress.org/drivers/. For BIOS NVMe driver support please contact with motherboard manufacturers.

5. SMART Feature Set

This log page is used to provide SMART and general health information. The information provided is over the life of the controller and is retained across power cycles. More details about Set Features command; please refer to NVM Express 1.4

5.1 Get Log Page (Log Identifier 02h)

Innodisk 3TO8 series SMART / Health Information Log are listed in following table.

Table 10: Get Log Page – SMART / Health Information Log

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>0</td><td>Critical Warning: This field indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set to ‘1’. If a bit is cleared to ‘0’, then that critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. Bits in this field represent the state at the time the Get Log Page command is processed and may not reflect the state at the time a related asynchronous event notification, if any, occurs or occurred.
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>0</td><td>If set to ‘1’, then the available spare capacity has fallen below the threshold.</td></tr>
<tr><td>1</td><td>If set to ‘1’, then a temperature is:
a) greater than or equal to an over temperature threshold.
b) less than or equal to an under temperature threshold.</td></tr>
<tr><td>2</td><td>If set to ‘1’, then the NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability.</td></tr>
<tr><td>3</td><td>If set to ‘1’, then all of the media has been placed in read only mode. The controller shall not set this bit to '1' if the read-only condition on the media is a result of a change in the write protection state of a namespace.</td></tr>
<tr><td>4</td><td>If set to ‘1’, then the volatile memory backup device has failed. This field is only valid if the controller has a volatile memory backup solution.</td></tr>
<tr><td>5</td><td>If set to ‘1’, then the Persistent Memory Region has become read-only or unreliable.</td></tr>
<tr><td>7:6</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>1:2</td><td>Composite Temperature: Contains a value corresponding to a temperature in degrees Kelvin that represents the current composite temperature of the controller and namespace(s) associated with that controller. The manner in which this value is computed is implementation specific and may not represent the actual temperature of any physical point in the NVM subsystem. The value of this field may be used to trigger an asynchronous event.
Warning and critical overheating composite temperature threshold values are reported by the WCTEMP and CCTEMP fields in the Identify Controller data structure.</td></tr>
<tr><td>3</td><td>Available Spare: Contains a normalized percentage (0 to 100%) of the remaining spare capacity available.</td></tr>
<tr><td>4</td><td>Available Spare Threshold: When the Available Spare falls below the threshold indicated in this field, an asynchronous event completion may occur. The value is indicated as a normalized percentage (0 to 100%). The values 101 to 255 are reserved.</td></tr>
<tr><td>5</td><td>Percentage Used: Contains a vendor specific estimate of the percentage of NVM subsystem life used based on the actual usage and the manufacturer’s prediction of NVM life. A value of 100 indicates that the estimated endurance of the NVM in the NVM subsystem has been consumed, but may not indicate an NVM subsystem failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value shall be updated once per power-on hour (when the controller is not in a sleep state).
Refer to the JEDEC JESD218A standard for SSD device life and endurance measurement techniques.</td></tr>
<tr><td>6</td><td>Endurance Group Critical Warning Summary: This field indicates critical warnings for the state of Endurance Groups. Each bit corresponds to a critical warning type, multiple bits may be set to ‘1’. If a bit is cleared to ‘0’, then that critical warning does not apply to any Endurance Group. Critical warnings may result in an asynchronous event notification to the host. Bits in this field represent the current associated state and are not persistent.
If a bit is set to ‘1’ in one or more Endurance Groups, then the corresponding bit shall be set to ‘1’ in this field.
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>0</td><td>If set to ‘1’, then the available spare capacity of one or more Endurance Groups has fallen below the threshold.</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>2</td><td>If set to ‘1’, then the reliability of one or more Endurance Groups has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability.</td></tr>
<tr><td>3</td><td>If set to ‘1’, then the namespaces in one or more Endurance Groups have been placed in read only mode not as a result of a change in the write protection state of a namespace.</td></tr>
<tr><td>7:4</td><td>Reserved</td></tr>
</table></td></tr>
</table>

7:31	**Reserved**
32:47	**Data Units Read:** Contains the number of 512 byte data units the host has read from the controller as part of processing a SMART Data Units Read Command; this value does not include metadata. This value is reported in thousands (i.e., a value of 1 corresponds to 1,000 units of 512 bytes read) and is rounded up (e.g., one indicates that the number of 512 byte data units read is from 1 to 1,000, three indicates that the number of 512 byte data units read is from 2,001 to 3,000). Refer to the specific I/O Command Set specification for the list of SMART Data Units Read Commands that affect this field. A value of 0h in this field indicates that the number of SMART Data Units Read is not reported.
48:63	**Data Units Written:** Contains the number of 512 byte data units the host has written to the controller as part of processing a User Data Out Command; this value does not include metadata. This value is reported in thousands (i.e., a value of 1 corresponds to 1,000 units of 512 bytes written) and is rounded up (e.g., one indicates that the number of 512 byte data units written is from 1 to 1,000, three indicates that the number of 512 byte data units written is from 2,001 to 3,000). Refer to the specific I/O Command Set specification for the list of User Data Out Commands that affect this field. A value of 0h in this field indicates that the number of Data Units Written is not reported.
64:79	**Host Read Commands:** Contains the number of SMART Host Read Commands completed by the controller. Refer to the specific I/O Command Set specification for the list of SMART Host Read Commands that affect this field.
80:95	**Host Write Commands:** Contains the number of User Data Out Commands completed by the controller. Refer to the specific I/O Command Set specification for the list of User Data Out Commands that affect this field.
96:111	**Controller Busy Time:** Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O Queue (specifically, a command was issued via an I/O Submission Queue Tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O Completion Queue). This value is reported in minutes.
112:127	**Power Cycles:** Contains the number of power cycles.
128:143	**Power On Hours:** Contains the number of power-on hours. This may not include time that the controller was powered and in a non-operational power state.
144:159	**Unsafe Shutdowns:** Contains the number of unsafe shutdowns. This count is incremented when the controller does not report it is safe to power down prior to loss of main power.

160:175	**Media and Data Integrity Errors:** Contains the number of occurrences where the controller detected an unrecovered data integrity error. Errors such as uncorrectable ECC, CRC checksum failure, or LBA tag mismatch are included in this field. Errors introduced as a result of a Write Uncorrectable command (refer to the NVM Command Set Specification) may or may not be included in this field.
176:191	**Number of Error Information Log Entries:** Contains the number of Error Information log entries over the life of the controller.
192:195	**Warning Composite Temperature Time:** Contains the amount of time in minutes that the controller is operational and the Composite Temperature is greater than or equal to the Warning Composite Temperature Threshold (WCTEMP) field and less than the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure in Figure 275. If the value of the WCTEMP or CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.
196:199	**Critical Composite Temperature Time:** Contains the amount of time in minutes that the controller is operational and the Composite Temperature is greater than or equal to the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure. If the value of the CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.
200:201	**Temperature Sensor 1:** Contains the current temperature reported by the embedded thermal sensor in the controller.
202:203	**Temperature Sensor 2:** Contains the current temperature reported by the embedded thermal sensor in the NAND Flash (Channel #0 and CE #0).
204:205	**Temperature Sensor 3:** Contains the current temperature reported by the embedded thermal sensor in the NAND Flash (Channel #0 and CE #0).
206:207	**Temperature Sensor 4:** Contains the current temperature reported by the embedded thermal sensor in the NAND Flash (Last channel and CE #0).
208:209	**Temperature Sensor 5:** Contains the current temperature reported by temperature sensor 5.
210:211	**Temperature Sensor 6:** Contains the current temperature reported by temperature sensor 6.
212:213	**Temperature Sensor 7:** Contains the current temperature reported by temperature sensor 7.
214:215	**Temperature Sensor 8:** Contains the current temperature reported by temperature sensor 8.
216:219	**Thermal Management Temperature 1 Transition Count:** Contains the number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature.
220:223	**Thermal Management Temperature 2 Transition Count:** Contains the number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance (e.g., heavy throttling) in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature.

224:227	**Total Time For Thermal Management Temperature 1:** Contains the number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature.
228:231	**Total Time For Thermal Management Temperature 2:** Contains the number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance (e.g., heavy throttling) in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature.
232:337	**Reserved**
338:345	**Later Bad Count**
346:353	**Power-On hours Count**
354:361	**Drive Power Cycle Count**
362:369	**Total Bad Block Count**
370:377	**User Max Erase Count**
378:385	**User Avg Erase Count**
386:393	**Device Life**
394:401	**Spare Block Count**
402:409	**Program Fail Count**
410:417	**Erase Fail Count**
418:425	**Unexpected Power Loss Count**
426:433	**Temperature (Kelvin - K °K)**
434:441	**Flash ID**
442:449	**Later Bad Block Info (Read / Write / Erase)**
450:457	**Total LBAs Written (unit = 32MB)**
458:465	**Total LBAs Read (unit = 32MB)**

6. Part Number Rule

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	D	**U**	**M**	**2**	**8**	**-**	**A**	**2**	**8**	**D**	**S**	**2**	**K**	**C**	**A**	**D**	**F**	**1**	**0**	**G**	**-**	**X**	**X**

Definition

Code 1st (Disk)	**Code 14th (Operation Temperature)**
D : Disk	C: Standard Grade (0℃~ +70℃)
	W: Industrial Grade (-40℃~ +85℃)

Code 2nd (Feature set)	**Code 15th (Internal control)**
U : Embedded series	A: PIN HEADER 90° (Horizontal Pin Headers)
	B: PIN HEADER 180° (Vertical Pin Headers)

Code 3rd ~5th (Form factor)	**Code 16th (Channel of data transfer)**
M28: M.2 Type 2280-D2-M	D: Dual Channels
	Q: Quad Channels

Code 7th ~9th (Capacity)			**Code 17th (Flash Type)**
A28: 128GB	B56: 256GB	C12: 512GB	F: Kioxia 3D TLC
1TB: 1TB	2TB: 2TB		

Code 10th ~12th (Controller)	**Code 18th ~20th (Hidden Area Size)**	
DS1: PCIe 3TO8 series	10G: 10 GB Hidden	20G: 20 GB Hidden
	30G: 30GB Hidden	60G: 60GB Hidden
	90G: 90GB Hidden	

Code 13th (Flash mode)	**Code 22nd~ (Customization Code)**
K: 112 layers 3D TLC	