

Approval Sheet

Customer	
Product Number	M3DW-4GSS2C0C-D (4GB)
Module speed	PC3-12800
Pin	204pin
Cl-tRCD-tRP	11-11-11
SDRAM Operating Temp	0°C~85°C
Date	13 rd July 2015

Approval by Customer

P/N:

Signature:

Date:

Sales: _____ Sr. Technical Manager: John Hsieh

Rev 1.1

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
		CL=7	CL=9	CL=11			
PC3-12800	P	1066	1333	1600	13.125	13.125	13.125

- JEDEC Standard 204-pin Dual In-Line Memory Module
- Intend for PC3-12800 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt (-0.075/+0.075V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- Embedded Thermal Sensor
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8 μ s ($T_A \leq +85^{\circ}\text{C}$)
- 16/10/1 Addressing (row/column/rank)-4GB
- SDRAM operating temperature range $0^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
- Programmable Device Operation:
 - Burst Type: Sequential or Interleave
 - Device CAS# Latency: 7, 9, 11
 - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant (*Section 14*)

2. Environmental Requirements

iDIMM is intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +65	°C	1
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.
2. Up to 9850 ft.

3. SDRAM Parameters by device density

RTT_Nom Setting	Parameter	4Gb	Units
tRFC	REF command ACT or REF command time	260	ns
tREFI	Average periodic refresh interval	0°C ≤ TCASE ≤ 85°C	7.8 μs
		85°C ≤ TCASE ≤ 95°C	3.9 μs

4. Ordering Information

ECCSODIMM							
Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC	Thermal Sensor
M3DW-4GSS2C0C-D	4GB	PC3-12800	512Mx72	9	1	Y	Y

5. Pin Configurations (Front side/Back side)

X72 ECCSODIMM

204-Pin DDR3 SO-UDIMM							
FRONT				BACK			
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	53	V88	105	A1	157	DM5
3	V88	55	DQ24	107	A0	159	DQ42
5	DQ0	57	DQ25	109	VDD	161	DQ43
7	DQ1	59	DM3	111	CK0	163	V88
9	V88	61	V88	113	CK0#	165	DQ48
11	DM0	63	DQ26	115	VDD	167	DQ49
13	DQ2	65	DQ27	117	A10/AP	169	V88
15	DQ3	67	V88	119	BA0	171	DQ86#
17	V88	69	CB0	121	WE#	173	DQ86
19	DQ8	71	CB1	123	VDD	175	V88
21	DQ9	73	V88	125	CAS#	177	DQ50
23	V88	75	DQ88#	127	CB0#	179	DQ51
25	DQ81#	77	DQ88	129	NC/CB1#	181	V88
27	DQ81	79	V88	131	VDD	183	DQ56
29	V88	81	CB2	133	DQ32	185	DQ57
31	DQ10	83	CB3	135	DQ33	187	V88
33	DQ11	85	VDD	137	V88	189	DM7
35	V88	87	CKE0	139	DQ84#	191	DQ58
37	DQ16	89	NC/CKE1#	141	DQ84	193	DQ59
39	DQ17	91	BA2	143	V88	195	V88
41	V88	93	VDD	145	DQ34	197	BA0
43	DQ82#	95	A12/BC#	147	DQ35	199	VDD8PD
45	DQ82	97	A8	149	V88	201	BA1
47	V88	99	A5	151	DQ40	203	VTT
49	DQ18	101	VDD	153	DQ41		
51	DQ19	103	A3	155	V88		
2	V88	54	DQ28	106	A2	158	V88
4	DQ4	56	DQ29	108	BA1	160	DQ46
6	DQ5	58	V88	110	VDD	162	DQ47
8	V88	60	DQ83#	112	ParIn/NC/ CK1	164	V88
10	DQ80#	62	DQ83	114	ErrOut/NC/ CK1#	166	DQ52
12	DQ80	64	V88	116	VDD	168	DQ53
14	V88	66	DQ30	118	NC/CB3#	170	V88
16	DQ6	68	DQ31	120	NC/CB2#	172	DM5
18	DQ7	70	V88	122	RAS#	174	DQ54
20	V88	72	CB4	124	VDD	176	DQ55
22	DQ12	74	CB5	126	ODT0	178	V88
24	DQ13	76	DM8	128	NC/ODT1	180	DQ60
26	V88	78	V88	130	A13	182	DQ61
28	DM1	80	CB6	132	VDD	184	V88
30	RESET#	82	CB7	134	DQ36	186	DQ87#
32	V88	84	VREFCA	136	DQ37	188	DQ87
34	DQ14	86	VDD	138	V88	190	V88
36	DQ15	88	A15*	140	DM4	192	DQ62
38	V88	90	A14*	142	DQ38	194	DQ63
40	DQ20	92	A9	144	DQ39	196	V88
42	DQ21	94	VDD	146	V88	198	EVENT#
44	DM2	96	A11	148	DQ44	200	8DA
46	V88	98	A7	150	DQ45	202	8CL
48	DQ22	100	A6	152	V88	204	VTT
50	DQ23	102	VDD	154	DQ85#		
52	V88	104	A4	156	DQ85		

Notes:
 * These pins are not used in this module.
 CB2#, CB3# (pin 120, 118) are used for a 4 rank module.

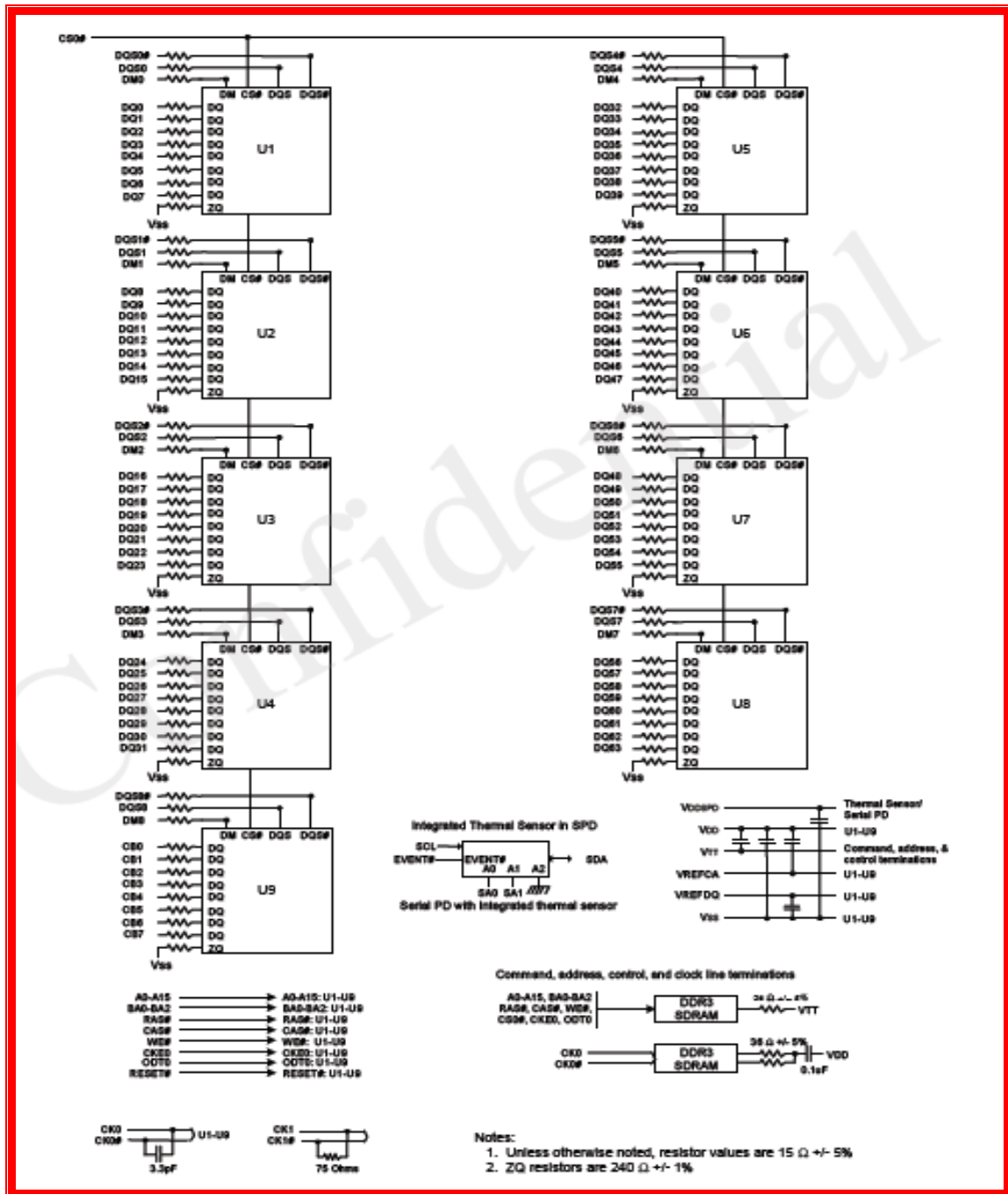
6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	V _{DD}	Power Supply
/WE	SDRAM write enable	V _{DDID}	V _{DD} Identification Flag
/S0 - /S1	DIMM Rank Select Lines	V _{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V _{REFDQ}	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V _{REFCA}	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V _{SS}	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	V _{DDSPD}	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	V _{TT}	SDRAM I/O termination supply.

7. Function Block Diagram:

- (4GB, 1 Rank, 512Mx72 DDR3 ECCSODIMM)



8. SDRAM Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note	
T _{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T _{STG}	Storage Temperature	-55 to 100	°C	4,5	
V _{IN} , V _{OUT}	Voltage on any pins relative to V _{ss}	-0.4 to +1.975	V	4	
V _{DD}	Voltage on VDD supply relative to V _{ss}	-0.4 to +1.975	V	4,6	
V _{DDQ}	Voltage on VDDQ supply relative to V _{ss}	-0.4 to +1.975	V	4,6	

Note:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM.

For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

- a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
- b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
V_{IH} (DC)	DC Input High (Logic1) Voltage	$V_{REF} + 0.1$	-	V _{DD}	V	3
V_{IL} (DC)	DC Input Low (Logic 0) Voltage	V _{SS}	-	$V_{REF} - 0.1$	V	3
V_{IH} (AC)	AC Input High (Logic1) Voltage	$V_{REF} + 0.175$	-	-	V	3
V_{IL} (AC)	AC Input Low (Logic 0) Voltage	-	-	$V_{REF} - 0.175$	V	3
V_{REFDQ} (DC)	Reference Voltage for DQ, DM inputs	$0.49V_{DDQ}$	$0.5V_{DDQ}$	$0.51V_{DDQ}$	V	4,5
V_{REFCA} (DC)	Reference Voltage for ADD,CMD inputs	$0.49V_{DDQ}$	$0.5V_{DDQ}$	$0.51V_{DDQ}$	V	4,5
Single Ended AC/DC output Levels						
V_{OH} (DC)	DC output high measurement level (for IV curve linearity)	-	$0.8 \times V_{DDQ}$	-	V	
V_{OM} (DC)	DC output mid measurement level (for IV curve linearity)	-	$0.5 \times V_{DDQ}$	-	V	
V_{OL} (DC)	DC output low measurement level (for IV curve linearity)	-	$0.2 \times V_{DDQ}$	-	V	
V_{OH} (AC)	AC output high measurement level (for output SR)	-	$V_{TT} + 0.1 \times V_{DDQ}$	-	V	6
V_{OL} (AC)	AC output low measurement level (for output SR)	-	$V_{TT} - 0.1 \times V_{DDQ}$	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
VIHdiff	Differential Input high	+0.2	-	Note 9	V	7
VILdiff	Differential Input logic Low	Note 9	-	-0.2	V	7
VIHdiff(ac)	Differential Input high ac	2* (VIH (AC)- VREF)	-	Note 9	V	8
VILdiff(ac)	Differential Input logic Low ac	Note 9	-	2* (VREF- VIL (AC))	V	8
Differential AC and DC Output Levels						
VOHdiff(AC)	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10
Note:						
<ol style="list-style-type: none"> Under all conditions VDDQ must be less than or equal to VDD. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together. For DQ and DM, Vref = VrefDQ. For input only pins except RESET#, Vref = VrefCA. The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV). For reference: approx. VDD/2 +/- 15 mV. The swing of $\pm 0.1 \times VDDQ$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $VTT = VDDQ/2$ Used to define a differential signal slew-rate. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU, DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot. The swing of $\pm 0.2 \times VDDQ$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $VTT = VDDQ/2$ at each of the differential outputs. 						

10. Operating, Standby, and Refresh Currents

- 4GB ECC SODIMM (1 Rank, 512Mx8 DDR3 SDRAMs $T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$)

Symbol	Parameter/Condition	12800	Unit	
I DD0	One bank; Active - Precharge	325	mA	
I DD1	One bank; Active - Read - Precharge	395	mA	
I DD2N	Precharge Standby Current	180	mA	
IDD2NT	Precharge Standby ODT Current	210	mA	
I DD2P	Precharge Power Down Current	Fast Mode	100	mA
	Precharge Power Down Current	Slow Mode	80	mA
I DD2Q	Precharge Quiet Standby Current	170	mA	
I DD3N	Active Standby Current	260	mA	
I DD3P	Active Power-Down Current	180	mA	
I DD4R	Operating Current Burst Read	840	mA	
I DD4W	Operating Current Burst Write	900	mA	
I DD5B	Burst Refresh Current	1980	mA	
I DD6	Self-Refresh Current: Normal Temperature Range	120	mA	
I DD6ET	Self-Refresh Current: Extended Temperature Range	160	mA	
I DD7	Operating Bank Interleave Read Current	1335	mA	
I DD8	Low precharge current	180	mA	

11. SPD Serial Presence Detect – (4GB)

1 RANK UNBUFFERED DDR SDRAM DIMM based on 512Mx8, 8Banks, 8K Refresh, DDR3 SDRAMs with SPD

Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
0	Number of Serial PD Bytes Written during Production	92	
1	SPD Revision	10	
2	Key Byte/DRAM Device Type	0B	
3	Key Byte/Module type	08	
4	SDRAM Density and Banks	04	
5	SDRAM Address	21	
6	Module Nominal Voltage, VDD	00	
7	Module Organization	01	
8	Module Memory Bus Width	0B	
9	Fine Timebase (FTB) Dividend/Divisor	52	
10	Medium Timebase (MTB) Dividend	01	
11	Medium Timebase (MTB) Divisor	08	
12	SDRAM Minimum Cycle Time (tCKmin)	0A	
13	Reserve	00	
14	CAS latency, least Significant Byte	FE	
15	CAS latency, most Significant Byte	00	
16	Minimum CAS Latency Time (tAAmin)	69	
17	Minimum Write Recovery Time (tWRmin)	78	

Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	69	
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	30	
20	Minimum Row Precharge Delay Time (tRPmin)	69	
21	Upper Nibbles for tRAS and tRC	11	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	18	
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	81	
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	20	
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	08	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	3C	
28	Upper Nibble for tFAW	00	
29	Minimum Four Activate Window Delay Time (tFAWmin)	F0	
30	SDRAM Optional Features	83	
31	SDRAM Thermal and Refresh Options	0D	
32	Module Thermal Sensor	00	
33	SDRAM Device Type	00	

34-59	Reserve	00	
60-63	Module Type Specific Section,	04 11 1F 00	
64-117	Reserve	00	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	86 F1	
119	Module ID: Module Manufacturing Location	02	
120-121	Module ID: Module Manufacturing Date	09 33	
122-125	Module Serial Number	00	
126-127	SPD Cyclical Redundancy Code	40 06	
128-255	reserve	-	

12. Timing Parameters

(T_{CASE} = 0 °C ~ 70 °C; V_{DDQ} = V_{DD}, See AC Characteristics)

Symbol	Parameter	PC3-12800		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.5	3.3	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-70	70	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-60	60	Ps
JIT (CC)	Cycle to Cycle Period Jitter	140		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	120		Ps
TJIT (duty)		-	-	Ps
TERR (2per)	Cumulative error across 2 cycle	-103	103	Ps
TERR (3per)	Cumulative error across 3 cycle	-122	122	Ps
TERR (4per)	Cumulative error across 4 cycle	-136	136	Ps
TERR (5per)	Cumulative error across 5 cycle	-147	147	Ps
TERR (6per)	Cumulative error across 6 cycle	-155	155	Ps
TERR (7per)	Cumulative error across 7 cycle	-163	163	Ps
TERR (8per)	Cumulative error across 3 cycle	-169	169	Ps
TERR (9per)	Cumulative error across 4 cycle	-175	175	Ps
TERR (10per)	Cumulative error across 5 cycle	-180	180	Ps

TERR (11per)	Cumulative error across 6 cycle	-184	184	Ps
TERR (12per)	Cumulative error across 7 cycle	-188	188	Ps
TERR (nper)	Cumulative error across 13~50 cycle	$tERR(nper)min = (1 + 0.68ln(n)) *$ $tJIT(per)min$ $tERR(nper)max = (1 + 0.68ln(n)) *$ $tJIT(per)max$		Ps
Data Timing				
Symbol	Parameter	Min.	Max.	Unit
tDSQ	DQS, DQS# to DQ skew, per group, per access	-	100	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-450	225	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	225	Ps
tDS(base) AC150	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	10	-	Ps
tDH(base) DC 100	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	45	-	Ps
Data Strobe Timing				
Symbol	Parameter	Min.	Max.	Unit
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps

tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
Command and Address Timing				
Symbol	Parameter	Min.	Max.	Unit
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK

tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup($t_{RP} / t_{CK(avg)}$)		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	35	9 tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	40	-	ns
tIS (base)	Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	45		ns
tIH(base)	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	170		ps
tIS(base) AC150	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	120		ps
Calibration Timing				
Symbol	Parameter	Min.	Max.	Unit
tZQinit	Power-up and RESET calibration time	Max. (512nCK, 640ns)	-	nCK
tZQoper	Normal operation Full calibration time	Max. (256nCK, 320ns)	-	nCK
tZQCS	Normal operation Short calibration time	Max. (64nCK, 80ns)	-	nCK

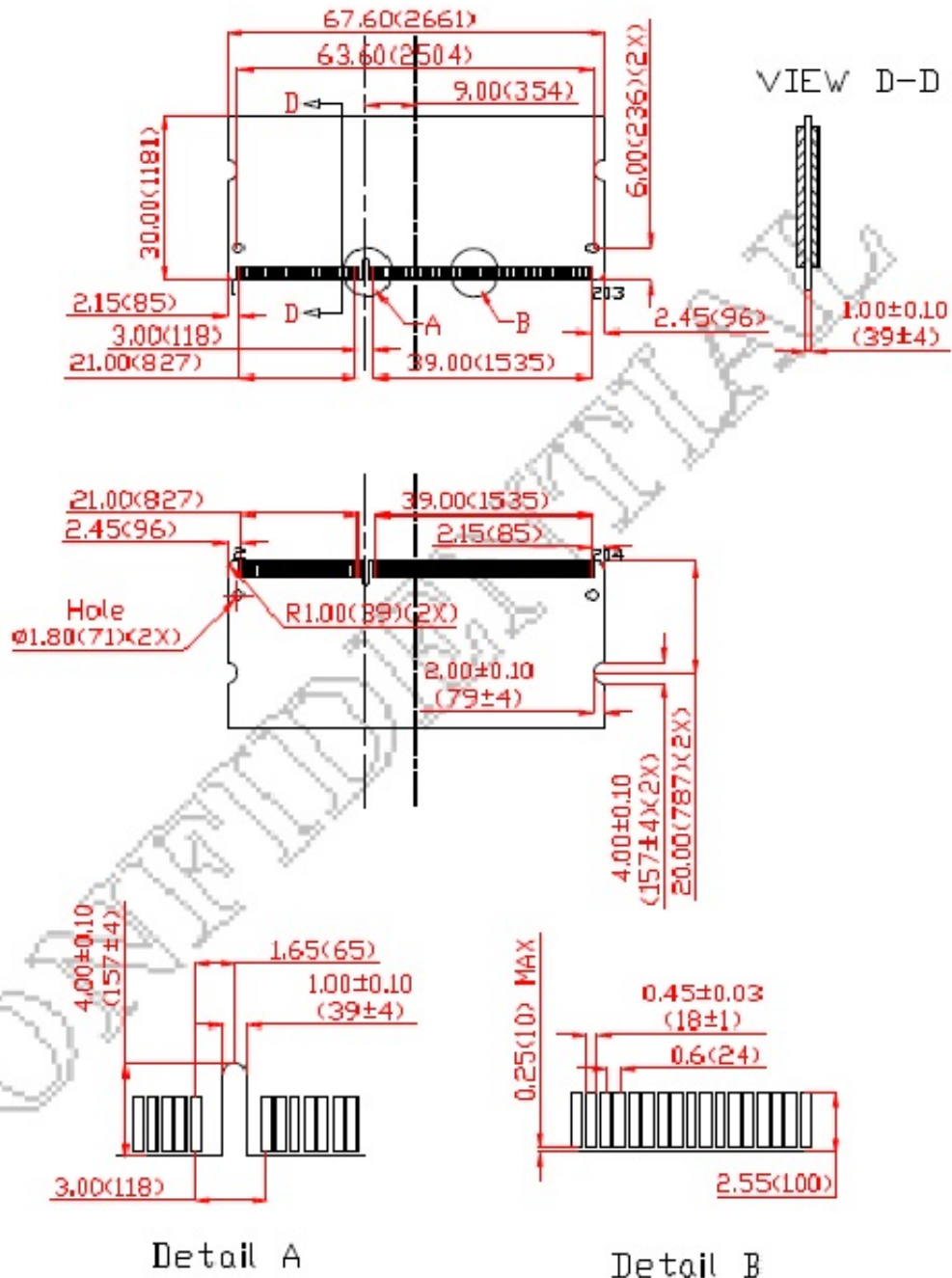
Reset Timing				
Symbol	Parameter	Min.	Max.	Unit
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK, tRFC(min) + 10ns)	-	
Self Refresh Timings				
Symbol	Parameter	Min.	Max.	Unit
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC(min) + 10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE9min) + 1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK, 10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK, 10ns)	-	
Power Down Timings				
Symbol	Parameter	Min.	Max.	Unit
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	

tCKE	CKE minimum pulse width	max(3nCK, 5ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCK(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	Parameter	Min.	Max.	Unit
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK

tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns
tAON	RTT-turn-on	-225	225	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)

13. PACKAGE DIMENSION

- (4GB, 1 Rank, 512Mx8 DDR3 base ECCSODIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

14. RoHS Declaration



Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M3DW-4GSS2C0C/-(X) complies with the requirement of RoHS directives 2011/65/EU and 2006/12/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI (Cr+6)	< 1000 ppm
Polybromodiphenyl ether (PBDE)	< 1000 ppm
Polybrominated Biphenyls (PBB)	< 1000 ppm
Perfluorooctane Sulfonate (PFOS)	Not Contained

Date issued: 2013/01/22

Manufacturer: : InnoDisk Co., Ltd.
 Address : 9F, No. 100, Sec.1 Xintai 5th Rd.,
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Authorized Signature :

QA Dept. Director - Ryan Tsai

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Revision Log

Rev	Date	Modification
0.1	12 th August 2013	Preliminary Edition
1.0	25 th February 2014	Official released.
1.1	13 rd July 2015	Modify Page2: VDD=VDDQ= 1.5 Volt (-0.075/+0.075V)