

# Approval Sheet

Customer	
Product Number	M3DW-4GSS2CN9-E
Module speed	PC3-10600
Pin	204pin
CI-tRCD-tRP	9-9-9
SDRAM Operating Temp	0°C ~85°C
Date	29 <sup>th</sup> August 2014

Approval by Customer

P/N:

Signature:

Date:

Sales: \_\_\_\_\_ Sr. Technical Manager: John Hsieh

Rev 1.0

# 1. Features

## Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
		CL=7	CL=9	CL=11			
<b>PC3-10600</b>	<b>N</b>	1066	1333	1333	13.5	13.5	13.5

- JEDEC Standard 204-pin Dual In-Line Memory Module
- Intend for PC3-10600 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt ( $\pm 0.075V$ )
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- Embedded Thermal Senso
- 8 bit pre-fetch
- Two different termination values (Rtt\_Nom & Rtt\_WR)
- Auto & self refresh  $7.8\mu s$  ( $T_A \leq +85^\circ C$ )
- 16/10/1 Addressing (row/column/rank)-4GB
- SDRAM operating temperature range  $0^\circ C \leq T_A \leq +85^\circ C$
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 7, 9, 11
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant (*Section 12*)

## 2. Environmental Requirements

iDIMM is intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +65	°C	1
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.  
 2. Up to 9850 ft.

## 3. SDRAM Parameters by device density

RTT_Nom Setting	Parameter	4Gb	Units
tRFC	REF command ACT or REF command time	260	ns
tREFI	Average periodic refresh interval	0°C ≤ TCASE ≤ 85°C	7.8 μs
		85°C ≤ TCASE ≤ 95°C	3.9 μs

#### 4. Ordering Information

ECCSODIMM							
Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC	Thermal Sensor
<b>M3DW-4GSS2CN9-E</b>	4GB	PC3-10600	512Mx72	9	1	Y	Y

## 5. Pin Configurations (Front side/Back side)

### X72 ECC SODIMM

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	VREFDQ	2	VSS	53	VSS	54	DQ28	103	A3	104	A4	155	VSS	156	DQS5_t
3	VSS	4	DQ4	55	DQ24	56	DQ29	105	A1	106	A2	157	DM5	158	VSS
5	DQ0	6	DQ5	57	DQ25	58	VSS	107	A0	108	BA1	159	DQ42	160	DQ46
7	DQ1	8	VSS	59	DM3	60	DQS3_c	109	VDD	110	VDD	161	DQ43	162	DQ47
9	VSS	10	DQS0_c	61	VSS	62	DQS3_t	111	CK0_t	112	Par_In, NC, CK1_t	163	VSS	164	VSS
11	DM0	12	DQS0_t	63	DQ26	64	VSS	113	CK0_c	114	Err_Out_n, NC, CK1_c	165	DQ48	166	DQ52
13	DQ2	14	VSS	65	DQ27	66	DQ30	115	VDD	116	VDD	167	DQ49	168	DQ53
15	DQ3	16	DQ6	67	VSS	68	DQ31	117	A10/AP	118	S3_n	169	VSS	170	VSS
17	VSS	18	DQ7	69	CB0	70	VSS	119	BA0	120	S2_n	171	DQS6_c	172	DM6
19	DQ8	20	VSS	71	CB1	72	CB4	121	WE_n	122	RAS_n	173	DQS6_t	174	DQ54
21	DQ9	22	DQ12	Key				123	VDD	124	VDD	175	VSS	176	DQ55
23	VSS	24	DQ13	73	VSS	74	CB5	125	CAS_n	126	ODT0	177	DQ50	178	VSS
25	DQS1_c	26	VSS	75	DQS8_c	76	DM8	127	S0_n	128	ODT1	179	DQ51	180	DQ60
27	DQS1_t	28	DM1	77	DQS8_t	78	VSS	129	S1_n	130	A13	181	VSS	182	DQ61
29	VSS	30	RESET_n	79	VSS	80	CB6	131	VDD	132	VDD	183	DQ56	184	VSS
31	DQ10	32	VSS	81	CB2	82	CB7	133	DQ32	134	DQ36	185	DQ57	186	DQS7_c
33	DQ11	34	DQ14	83	CB3	84	VREFCA	135	DQ33	136	DQ37	187	VSS	188	DQS7_t
35	VSS	36	DQ15	85	VDD	86	VDD	137	VSS	138	VSS	189	DM7	190	VSS
37	DQ16	38	VSS	87	CKE0	88	A15	139	DQS4_c	140	DM4	191	DQ58	192	DQ62
39	DQ17	40	DQ20	89	CKE1	90	A14	141	DQS4_t	142	DQ38	193	DQ59	194	DQ63
41	VSS	42	DQ21	91	BA2	92	A9	143	VSS	144	DQ39	195	VSS	196	VSS
43	DQS2_c	44	DM2	93	VDD	94	VDD	145	DQ34	146	VSS	197	SA0	198	EVENT_n
45	DQS2_t	46	VSS	95	A12/BC_n	96	A11	147	DQ35	148	DQ44	199	VDDSPD	200	SDA
47	VSS	48	DQ22	97	A8	98	A7	149	VSS	150	DQ45	201	SA1	202	SCL
49	DQ18	50	DQ23	99	A5	100	A6	151	DQ40	152	VSS	203	VTT	204	VTT
51	DQ19	52	VSS	101	VDD	102	VDD	153	DQ41	154	DQS5_c				

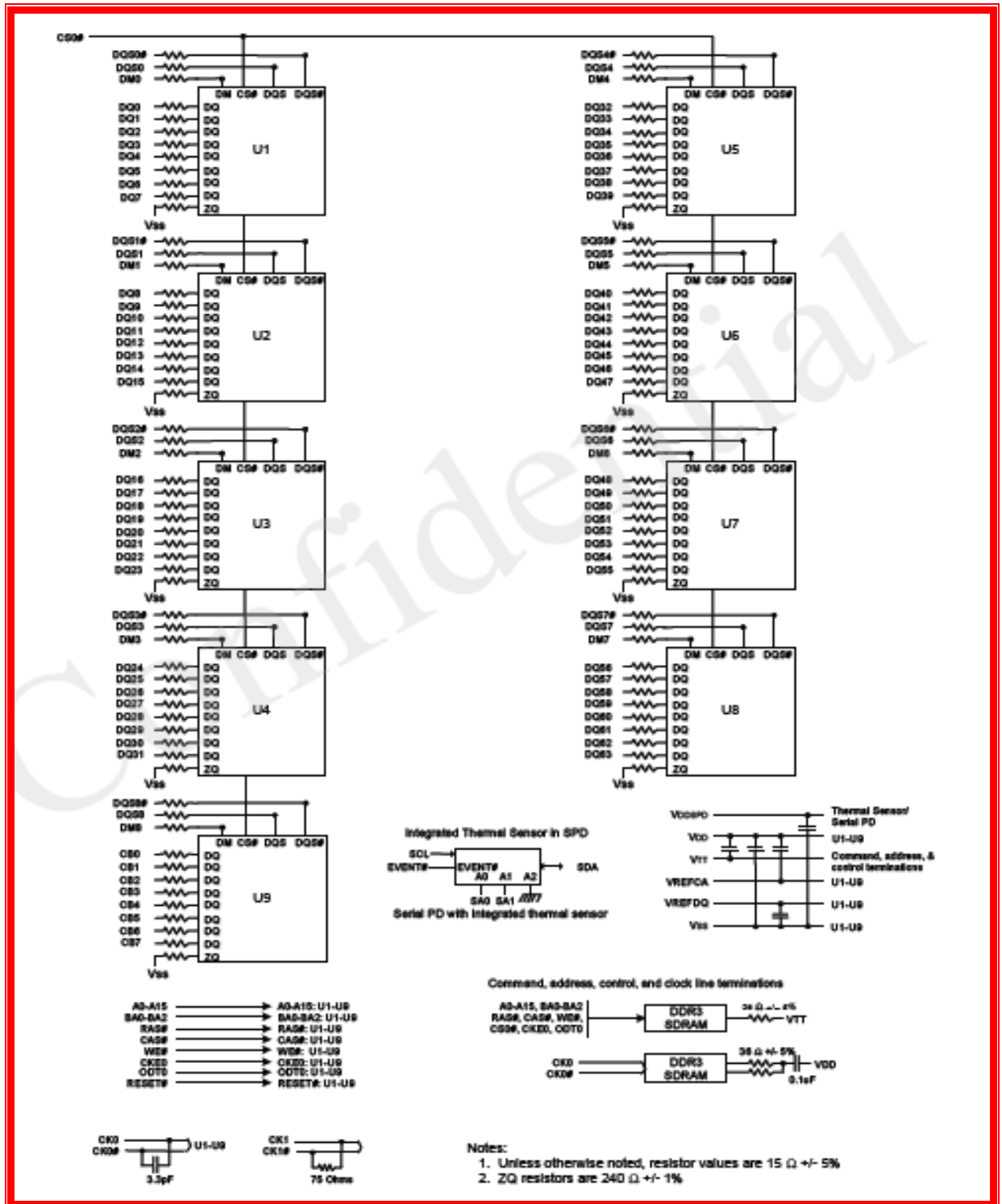
## 6. Architecture

### Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	V <sub>DD</sub>	Power Supply
/WE	SDRAM write enable	V <sub>DDID</sub>	V <sub>DD</sub> Identification Flag
/S0 - /S1	DIMM Rank Select Lines	V <sub>DDQ</sub>	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V <sub>REFDQ</sub>	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V <sub>REFCA</sub>	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V <sub>SS</sub>	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	V <sub>DDSPD</sub>	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	V <sub>TT</sub>	SDRAM I/O termination supply.

### 7. Function Block Diagram:

- (4GB, 1 Rank 512Mx8 DDR3 ECCSODIMM)



Note: Temperature sensor accuracy (max):

- ± 1 °C from +75 °C to +95 °C
- ± 2 °C from +40 °C to +125 °C
- ± 3 °C from -40 °C to +125 °C



## 8. SDRAM Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note	
T <sub>OPER</sub>	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T <sub>STG</sub>	Storage Temperature	-55 to 100	°C	4,5	
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pins relative to V <sub>ss</sub>	-0.4 to +1.975	V	4	
V <sub>DD</sub>	Voltage on VDD supply relative to V <sub>ss</sub>	-0.4 to +1.975	V	4,6	
V <sub>DDQ</sub>	Voltage on VDDQ supply relative to V <sub>ss</sub>	-0.4 to +1.975	V	4,6	

**Note:**

- Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center / top side of the DRAM.  
For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
  - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- V<sub>DD</sub> and V<sub>DDQ</sub> must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x V<sub>DDQ</sub>, When V<sub>DD</sub> and V<sub>DDQ</sub> are less than 500 mV; VREF may be equal to or less than 300 mV



## 9. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
<b>Recommended DC Operating Conditions</b>						
<b>V<sub>DD</sub></b>	Supply Voltage	1.425	1.5	1.575	V	1,2
<b>V<sub>DDQ</sub></b>	Supply Voltage	1.425	1.5	1.575	V	1,2
<b>Single Ended AC/DC Input Levels</b>						
<b>V<sub>IH</sub> (DC)</b>	DC Input High (Logic1) Voltage	$V_{REF} + 0.1$	-	V <sub>DD</sub>	V	3
<b>V<sub>IL</sub> (DC)</b>	DC Input Low (Logic 0) Voltage	V <sub>SS</sub>	-	$V_{REF} - 0.1$	V	3
<b>V<sub>IH</sub> (AC)</b>	AC Input High (Logic1) Voltage	$V_{REF} + 0.175$	-	-	V	3
<b>V<sub>IL</sub> (AC)</b>	AC Input Low (Logic 0) Voltage	-	-	$V_{REF} - 0.175$	V	3
<b>V<sub>REFDQ</sub> (DC)</b>	Reference Voltage for DQ, DM inputs	0.49V <sub>DDQ</sub>	0.5V <sub>DDQ</sub>	0.51V <sub>DDQ</sub>	V	4,5
<b>V<sub>REFCA</sub> (DC)</b>	Reference Voltage for ADD,CMD inputs	0.49V <sub>DDQ</sub>	0.5V <sub>DDQ</sub>	0.51V <sub>DDQ</sub>	V	4,5
<b>Single Ended AC/DC output Levels</b>						
<b>V<sub>OH</sub> (DC)</b>	DC output high measurement level (for IV curve linearity)	-	0.8 x V <sub>DDQ</sub>	-	V	
<b>V<sub>OM</sub> (DC)</b>	DC output mid measurement level (for IV curve linearity)	-	0.5 x V <sub>DDQ</sub>	-	V	
<b>V<sub>OL</sub> (DC)</b>	DC output low measurement level (for IV curve linearity)	-	0.2 x V <sub>DDQ</sub>	-	V	
<b>V<sub>OH</sub> (AC)</b>	AC output high measurement level (for output SR)	-	$V_{TT} + 0.1 \times V_{DDQ}$	-	V	6
<b>V<sub>OL</sub> (AC)</b>	AC output low measurement level (for output SR)	-	$V_{TT} - 0.1 \times V_{DDQ}$	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
<b>Differential AC/DC Input Levels</b>						
<b>VIHdiff</b>	Differential Input high	+0.2	-	Note 9	V	7
<b>VILdiff</b>	Differential Input logic Low	Note 9	-	-0.2	V	7
<b>VIHdiff(ac)</b>	Differential Input high ac	2* (VIH (AC)- VREF)	-	Note 9	V	8
<b>VILdiff(ac)</b>	Differential Input logic Low ac	Note 9	-	2* (VREF- VIL (AC) )	V	8
<b>Differential AC and DC Output Levels</b>						
<b>VOHdiff(AC)</b>	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
<b>VOLdiff(AC)</b>	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10
<b>Note:</b>						
<ol style="list-style-type: none"> <li>Under all conditions VDDQ must be less than or equal to VDD.</li> <li>VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.</li> <li>For DQ and DM, Vref = VrefDQ. For input only pins except RESET#, Vref = VrefCA.</li> <li>The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).</li> <li>For reference: approx. VDD/2 +/- 15 mV.</li> <li>The swing of <math>\pm 0.1 \times VDDQ</math> is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 <math>\Omega</math> and an effective test load of 25 <math>\Omega</math> to <math>V_{TT} = VDDQ/2</math></li> <li>Used to define a differential signal slew-rate.</li> <li>For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.</li> <li>These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.</li> <li>The swing of <math>\pm 0.2 \times VDDQ</math> is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 <math>\Omega</math> and an effective test load of 25 <math>\Omega</math> to <math>V_{TT} = VDDQ/2</math> at each of the differential outputs.</li> </ol>						

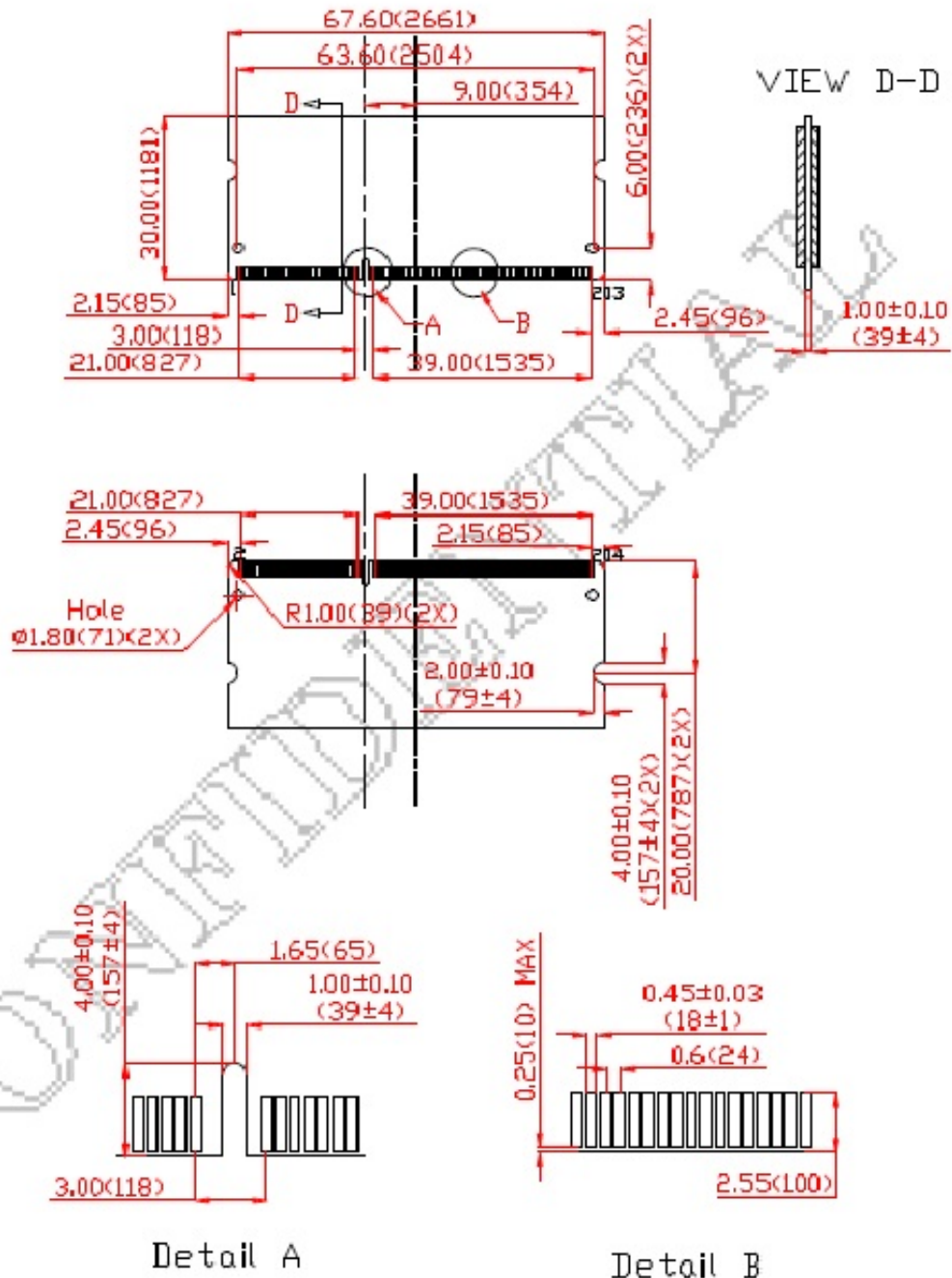
## 10. Operating, Standby, and Refresh Currents

- 4GB ECC SODIMM (1 Rank, 512Mx8 DDR3 SDRAMs  $T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$ )

Symbol	Parameter/Condition	10600	Unit	
I DD0	One bank; Active - Precharge	300	mA	
I DD1	One bank; Active - Read - Precharge	360	mA	
I DD2N	Precharge Standby Current	180	mA	
IDD2NT	Precharge Standby ODT Current	210	mA	
I DD2P	Precharge Power Down Current	Fast Mode	100	mA
	Precharge Power Down Current	Slow Mode	80	mA
I DD2Q	Precharge Quiet Standby Current	170	mA	
I DD3N	Active Standby Current	260	mA	
I DD3P	Active Power-Down Current	180	mA	
I DD4R	Operating Current Burst Read	840	mA	
I DD4W	Operating Current Burst Write	900	mA	
I DD5B	Burst Refresh Current	1750	mA	
I DD6	Self-Refresh Current: Normal Temperature Range	120	mA	
I DD7	Operating Bank Interleave Read Current	1215	mA	
I DD8	Low precharge current	180	mA	

### 11. PACKAGE DIMENSION

- (4GB, 1 Rank 512Mx8 DDR3 base ECCSODIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of  $\pm 0.15 (6)$ , unless otherwise specified.

## 12. RoHS Declaration



### Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M3DW-4GSS2CN9-(X) complies with the requirement of RoHS directives 2011/65/EU and 2006/12/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3<sup>rd</sup> party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI (Cr+6)	< 1000 ppm
Polybromodiphenyl ether (PBDE)	< 1000 ppm
Polybrominated Biphenyls (PBB)	< 1000 ppm
Perfluorooctane Sulfonate (PFOS)	Not Contained

Date issued: 2014/01/22

Manufacturer: : InnoDisk Co., Ltd.  
 Address : 9F, No. 100, Sec.1 Xintai 5<sup>th</sup> Rd.,  
Xizhi City, Taipei 221, Taiwan

Authorized Signature :

QA Dept. Director - *Ryan Tsai*

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## Revision Log

Rev	Date	Modification
0.1	29 <sup>th</sup> August 2014	Preliminary Edition
1.0	29 <sup>th</sup> August 2014	Official released.