innodisk

The Total Solution For Industrial Flash Storage

Approval Sheet

Customer	
Product Number	**M3CW-1GSF1CM7-I**
Module speed	**PC3-8500**
Pin	**240pin**
Cl-tRCD-tRP	**7-7-7**
SDRAM Operating Temp	**0℃~85℃**
Date	**4th May 2016**

Approval by Customer

P/N:

Signature:

Date:

Sales: **Sr. Marketing Manager: John Hsieh**

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
		CL=7	CL=9	CL=11			
PC3-8500	M	1066	1066	1066	13.125	13.125	13.125

- JEDEC Standard 240-pin Dual In-Line Memory Module
- Intend for PC3-8500 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt ± 0.075
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs ($T_A \leq +85°C$)
- 14/10/1 Addressing (row/column/rank)-1GB
- SDRAM operating temperature range
  - $0°C \leq Tcase \leq +85°C$
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 7
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant *(Section 12)*

2. Environmental Requirements

iDIMM's SDRAMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.
2. Up to 9850 ft.

3. SDRAM Parameters by device density

RTT_Nom Setting	Parameter		1Gb	Units
tRFC	REF command ACT or REF command time		110	ns
tREFI	Average periodic refresh interval	0°C≦T_{CASE}≦85°C	7.8	µs
		85°C≦T_{CASE}≦95°C	3.9	µs

4. Ordering Information

DDR3 UDIMM w/ECC						
Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC
M3CW-1GSF1CM7-I	1GB	PC3-8500	128Mx72	9	1	Y

5. Pin Configurations (Front side/Back side)

X72 UDIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	121	V_{SS}	31	DQ25	151	V_{SS}	61	A2	181	A1	91	DQ41	211	V_{SS}
2	V_{SS}	122	DQ4	32	V_{SS}	152	DM3, DQS12, TDQS12	62	V_{DD}	182	V_{DD}	92	V_{SS}	212	DM5, DQS14, TDQS14
3	DQ0	123	DQ5	33	DQS3#	153	NC, DQS12#, TDQS12#	63	NC, CK1	183	V_{DD}	93	DQS5#	213	NC, DQS14#, TDQS14#
4	DQ1	124	V_{SS}	34	DQS3	154	V_{SS}	64	NC, CK1#	184	CK0	94	DQS5	214	V_{SS}
5	V_{SS}	125	DM0, DQS9, TDQS9	35	V_{SS}	155	DQ30	65	V_{DD}	185	CK#0	95	V_{SS}	215	DQ46
6	DQS0#	126	NC, DQS9#, TDQS9#	36	DQ26	156	DQ31	66	V_{DD}	186	V_{DD}	96	DQ42	216	DQ47
7	DQS0	127	V_{SS}	37	DQ27	157	V_{SS}	67	V_{REFCA}	187	EVENT#, NC	97	DQ43	217	V_{SS}
8	V_{SS}	128	DQ6	38	V_{SS}	158	CB4,NC	68	P_{AR_IN},NC	188	A0	98	V_{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC	69	V_{DD}	189	V_{DD}	99	DQ48	219	DQ53
10	DQ3	130	V_{SS}	40	CB1,NC	160	V_{SS}	70	A10/AP	190	BA1	100	DQ49	220	V_{SS}
11	V_{SS}	131	DQ12	41	V_{SS}	161	DM8, DQS17, TDQS17	71	BA0	191	V_{DD}	101	V_{SS}	221	DM6, DQS15, TDQS15
12	DQ8	132	DQ13	42	DQS8#	162	NC, DQS17#, TDQS17#	72	V_{DD}	192	RAS#	102	DQS6#	222	NC, DQS15#, TDQS15#
13	DQ9	133	V_{SS}	43	DQS8	163	V_{SS}	73	WE#	193	S0#	103	DQS6	223	V_{SS}
14	V_{SS}	134	DM1, DQS10, TDQS10	44	V_{SS}	164	CB6,NC	74	CAS#	194	V_{DD}	104	V_{SS}	224	DQ54
15	DQS1#	135	NC, DQS10#, TDQS10#	45	CB2,NC	165	CB7,NC	75	V_{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	V_{SS}	46	CB3,NC	166	V_{SS}	76	S1#,NC	196	A13	106	DQ51	226	V_{SS}
17	V_{SS}	137	DQ14	47	V_{SS}	167	NC	77	ODT1,NC	197	V_{DD}	107	V_{SS}	227	DQ60
18	DQ10	138	DQ15	48	V_{TT},NC	168	RESET#	78	V_{DD}	198	S3#,NC	108	DQ56	228	DQ61
19	DQ11	139	V_{SS}	49	V_{TT},NC	169	CKE1,NC	79	S2#,NC	199	V_{SS}	109	DQ57	229	V_{SS}
20	V_{SS}	140	DQ20	50	CKE0	170	V_{DD}	80	V_{SS}	200	DQ36	110	V_{SS}	230	DM7, DQS16, TDQS16
21	DQ16	141	DQ21	51	V_{DD}	171	A15,NC	81	DQ32	201	DQ37	111	DQS7#	231	NC, DQS16#, TDQS16#
22	DQ17	142	V_{SS}	52	BA2	172	A14	82	DQ33	202	V_{SS}	112	DQS7	232	V_{SS}
23	V_{SS}	143	DM2, DQS11, TDQS11	53	E_{RR_Out}#, NC	173	V_{DD}	83	V_{SS}	203	DM4, DQS13, TDQS13	113	V_{SS}	233	DQ62
24	DQS2#	144	NC, DQS11#, TDQS11#	54		174	A12/BC#	84	DQS4#	204	NC, DQS13#, TDQS13#	114	DQ58	234	DQ63
25	DQS2	145	V_{SS}	55	A11	175	A9	85	DQS4	205	V_{SS}	115	DQ59	235	V_{SS}
26	V_{SS}	146	DQ22	56	A7	176	V_{DD}	86	V_{SS}	206	DQ38	116	V_{SS}	236	V_{DDSPD}
27	DQ18	147	DQ23	57	V_{DD}	177	A8	87	DQ34	207	DQ39	117	SA0	237	SA0
28	DQ19	148	V_{SS}	58	A5	178	A6	88	DQ35	208	V_{SS}	118	SCL	238	SA1
29	V_{SS}	149	DQ28	59	A4	179	V_{DD}	89	V_{SS}	209	DQ44	119	SA2	239	V_{SS}
30	DQ24	150	DQ29	60	V_{DD}	180	A3	90	DQ40	210	DQ45	120	V_{TT}	240	V_{TT}

NC = No Connect, RFU = Reserved for Future Use

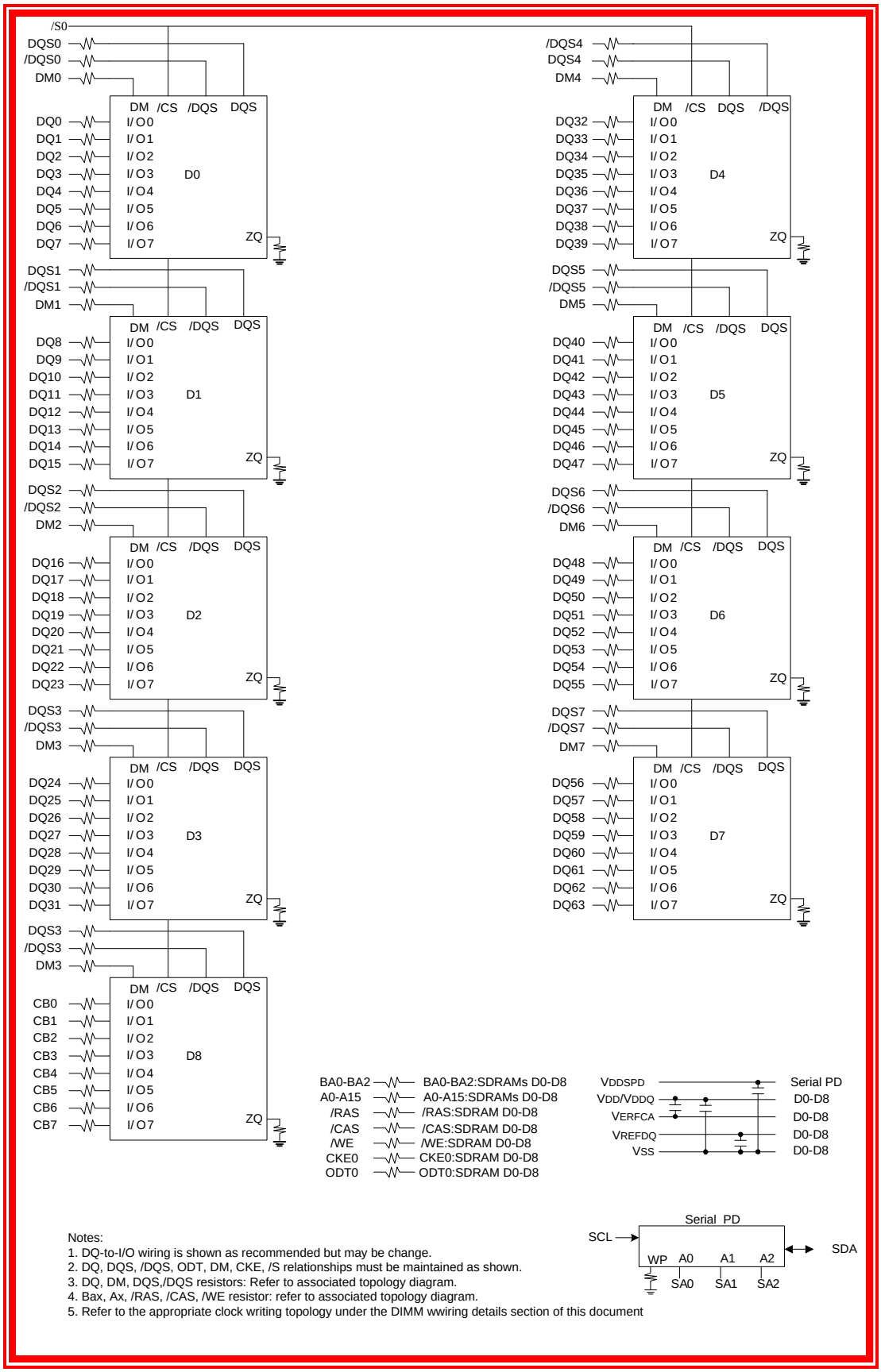
6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	V_{DD}	Power Supply
/WE	SDRAM write enable	V_{DDID}	V_{DD} Identification Flag
/S0 - /S1	DIMM Rank Select Lines	V_{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V_{REFDQ}	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V_{REFCA}	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	V_{TT}	SDRAM I/O termination supply.

7. Function Block Diagram:

- (1GB, 1 Rank, 128Mx8 DDR3 SDRAMs)



Notes:
1. DQ-to-I/O wiring is shown as recommended but may be change.
2. DQ, DQS, /DQS, ODT, DM, CKE, /S relationships must be maintained as shown.
3. DQ, DM, DQS,/DQS resistors: Refer to associated topology diagram.
4. Bax, Ax, /RAS, /CAS, /WE resistor: refer to associated topology diagram.
5. Refer to the appropriate clock writing topology under the DIMM wwiring details section of this document

8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.975	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.975	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.975	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.
For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under
all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 ℃ case temperature. Full specifications are supported in this range, but the following additional
conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
$V_{IH\ (DC)}$	DC Input High (Logic1) Voltage	V_{REF} + 0.1	-	V_{DD}	V	3
$V_{IL\ (DC)}$	DC Input Low (Logic 0) Voltage	V_{SS}	-	V_{REF} - 0.1	V	3
$V_{IH\ (AC)}$	AC Input High (Logic1) Voltage	V_{REF}+ 0.175	-	-	V	3
$V_{IL\ (AC)}$	AC Input Low (Logic 0) Voltage	-	-	V_{REF} - 0.175	V	3
$V_{REFDQ\ (DC)}$	Reference Voltage for DQ, DM inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
$V_{REFCA\ (DC)}$	Reference Voltage for ADD,CMD inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
Single Ended AC/DC output Levels						
$V_{OH\ (DC)}$	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
$V_{OM\ (DC)}$	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
$V_{OL\ (DC)}$	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	
$V_{OH\ (AC)}$	AC output high measurement level (for output SR)	-	VTT + 0.1 x VDDQ	-	V	6
$V_{OL\ (AC)}$	AC output low measurement level (for output SR)		VTT - 0.1 x VDDQ	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
V_{IHdiff}	Differential Input high	+0.2	-	Note 9	V	7
V_{ILdiff}	Differential Input logic Low	Note 9	-	-0.2	V	7
$V_{IHdiff(ac)}$	Differential Input high ac	2* ($V_{IH\ (AC)}$-V_{REF})	-	Note 9	V	8
$V_{ILdiff(ac)}$	Differential Input logic Low ac	Note 9	-	2* (V_{REF}-$V_{IL\ (AC)}$)	V	8
Differential AC and DC Output Levels						
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
4. The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
5. For reference: approx. VDD/2 +/- 15 mV.
6. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2
7. Used to define a differential signal slew-rate.
8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.
10. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

10. Operating, Standby, and Refresh Currents

- 1GB UDIMM w/ECC (1 Rank, 128Mx8 DDR3 SDRAMs T_{CASE} = 0 °C ~ 70 °C)

Symbol	Parameter/Condition		PC3-8500	Unit
I DD0	One bank; Active - Precharge		TBD	mA
I DD1	One bank; Active - Read - Precharge		TBD	mA
I DD2N	Precharge Standby Current		TBD	mA
IDD2NT	Precharge Standby ODT Current		TBD	mA
I DD2P	Precharge Power Down Current	Fast Mode	TBD	mA
	Precharge Power Down Current	Slow Mode	TBD	mA
I DD2Q	Pecharge Quiet Standby Current		TBD	mA
I DD3N	Active Standby Current		TBD	mA
I DD3P	Active Power-Down Current		TBD	mA
I DD4R	Operating Current Burst Read		TBD	mA
I DD4W	Operating Current Burst Write		TBD	mA
I DD5B	Burst Refresh Current		TBD	mA
I DD6	Self-Refresh Current: Normal Temperature Range		TBD	mA
I DD7	Operating Bank Interleave Read Current		TBD	mA
I DD8	RESET Low Current		TBD	mA

11. Timing Parameters

(T_{CASE} = 0 °C ~ 70 °C; V_{DDQ} = V_{DD} , See AC Characteristics)

Symbol	Parameter	PC3-8500		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.875	2.5	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-90	90	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-80	80	Ps
JIT (CC)	Cycle to Cycle Period Jitter	180		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	160		Ps
TJIT (duty)		-	-	Ps
TERR (2per)	Cumulative error across 2 cycle	-132	132	Ps
TERR (3per)	Cumulative error across 3 cycle	-157	157	Ps
TERR (4per)	Cumulative error across 4 cycle	-175	175	Ps
TERR (5per)	Cumulative error across 5 cycle	-188	188	Ps
TERR (6per)	Cumulative error across 6 cycle	-200	200	Ps
TERR (7per)	Cumulative error across 7 cycle	-209	209	Ps
TERR (8per)	Cumulative error across 3 cycle	-217	217	Ps
TERR (9per)	Cumulative error across 4 cycle	-224	224	Ps
TERR (10per)	Cumulative error across 5 cycle	-231	231	Ps

TERR (11per)	Cumulative error across 6 cycle	-237	237	Ps
TERR (12per)	Cumulative error across 7 cycle	-242	242	Ps
TERR (nper)	Cumulative error across 13~50 cycle	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		Ps
Data Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDSQ	DQS, DQS# to DQ skew, per group, per access	-	150	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-600	300	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	300	Ps
tDS(base) AC150	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	25	-	Ps
tDH(base) DC 100	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	100	-	Ps
Data Strobe Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.38		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.38		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-300	300	Ps

tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-600	300	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	300	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.4	0.6	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.4	0.6	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.25	0.25	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.2	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.2	-	tCK(avg)
Command and Address Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK

tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	36	9 tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 7.5ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 10ns)	-	
tFAW	Four activate window for 1KB page size	37.5	-	ns
tFAW	Four activate window for 2KB page size	50	-	ns
tIS (base)	Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	125		ns
tIH(base)	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	200		ps
tIS(base) AC150	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	-		ps
Calibration Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tZQinit	Power-up and RESET calibration time	Max. (512nCK, 640ns)	-	nCK
tZQoper	Normal operation Full calibration time	Max. (256nCK, 320ns)	-	nCK
tZQCS	Normal operation Short calibration time	Max. (64nCK, 64ns)	-	nCK
Reset Timing				

Symbol	Parameter	Min.	Max.	Unit
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK,tRFC(min) +10ns)	-	
Self Refresh Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC(min) +10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE9min) +1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK,10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK,10ns)	-	
Power Down Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK,5.625ns)	-	
tCPDED	Command pass disable delay	1	-	nCK

tPD	Power Down Entry to Exit Timing	tCK(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	1	9	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	1	9	ns

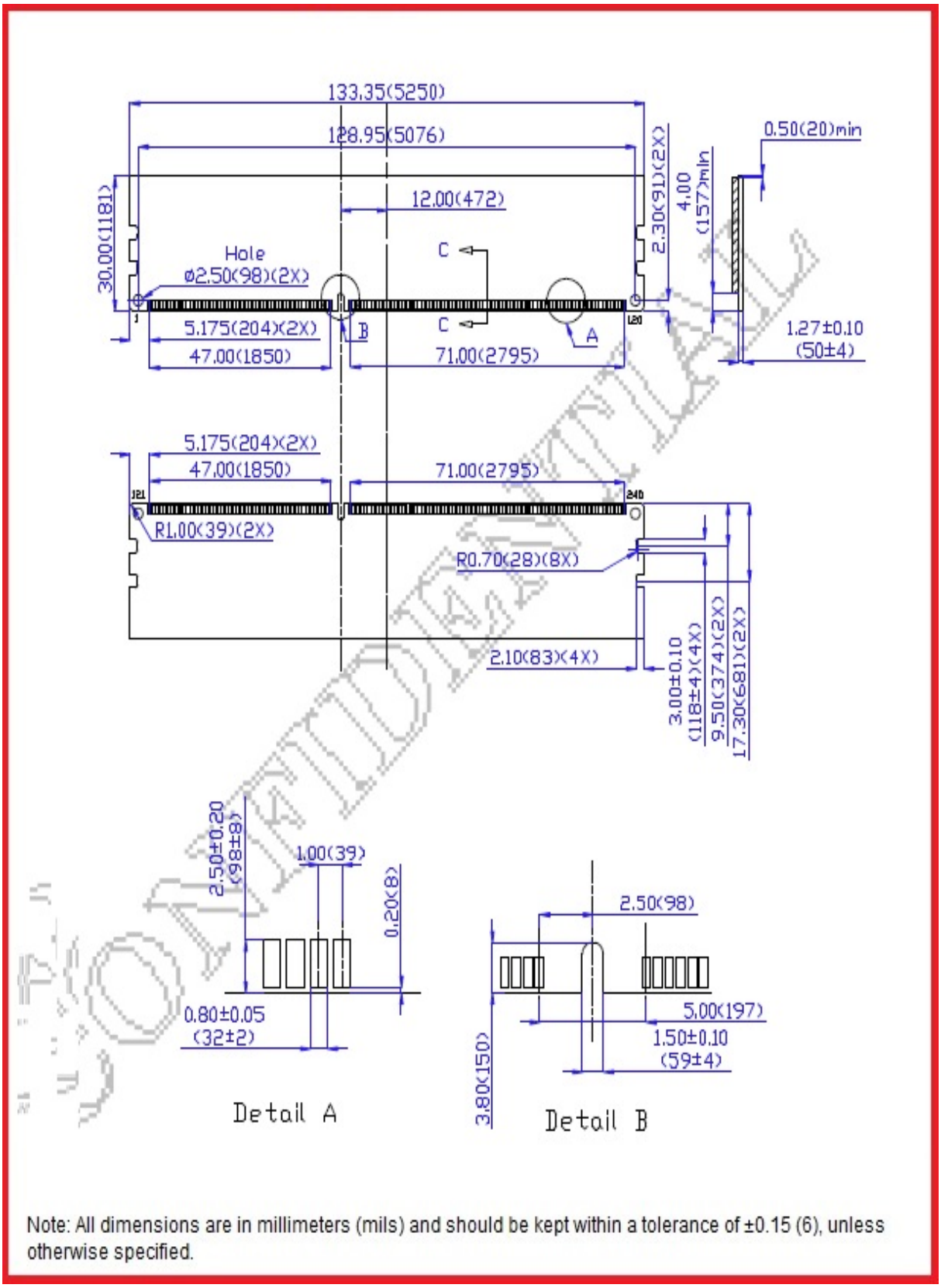
tAON	RTT-turn-on	-300	300	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)

Write Leveling Timing

Symbol	Parameter	Min.	Max.	Unit
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	245	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	245	-	ps
tWLO	Write leveling output delay	0	9	ns
tWLOE	Write leveling output error	0	2	ns

12. PACKAGE DIMENSION

- (1GB, 1 Rank, 128Mx8 DDR3 base UDIMM w/ECC)



13. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI (Cr+6)	< 1000 ppm
Polybromodiphenyl ether (PBDE)	< 1000 ppm
Polybrominated Biphenyls (PBB)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Richard Lee 李鐘亮

Company Representative Title 公司代表人職稱： CEO 執行長

Date 日期： 2014 / 07 / 29

(Company Stamp/公司大小章)

14. Revision Log

Rev	Date	Modification
0.1	4th May 2016	Preliminary Edition
1.0	4th May 2016	Official released.