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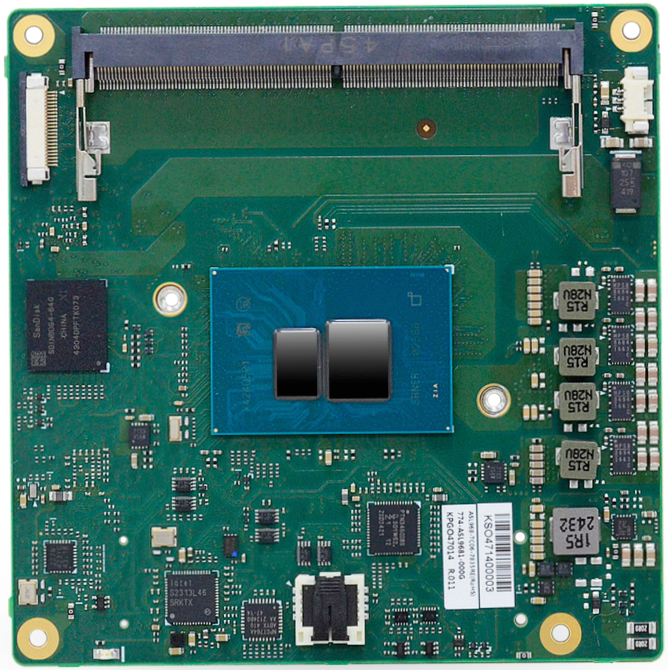


ASL968

COM Express Compact Module
User's Manual

Copyright

Trademarks

COM Express Specification Reference

PICMG® COM Express® Module Base Specification.
http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- Wear an antistatic wrist strap.
- Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

The accessories in the package may not come similar to the information listed below. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- Cooler
- CPU block
- Thermal grease

Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- Heat Spreader Upon Request (MOQ:50pcs)
- COM335 Carrier Board Kit

Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

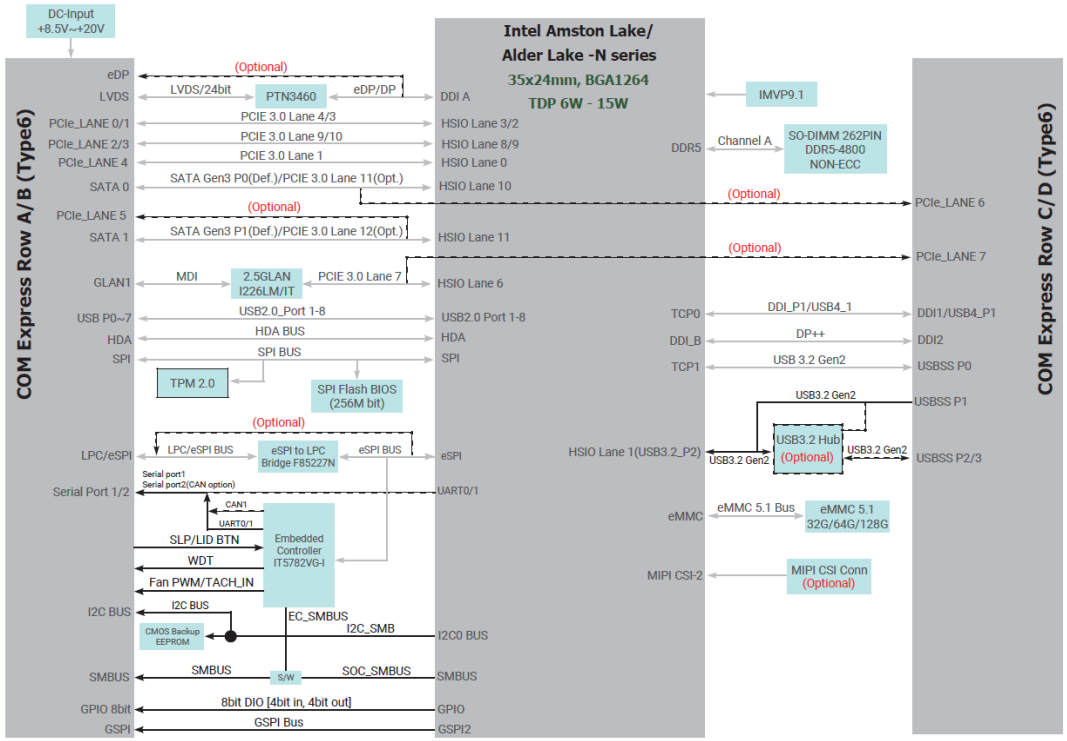
Chapter 1 - Introduction

▶ Specification

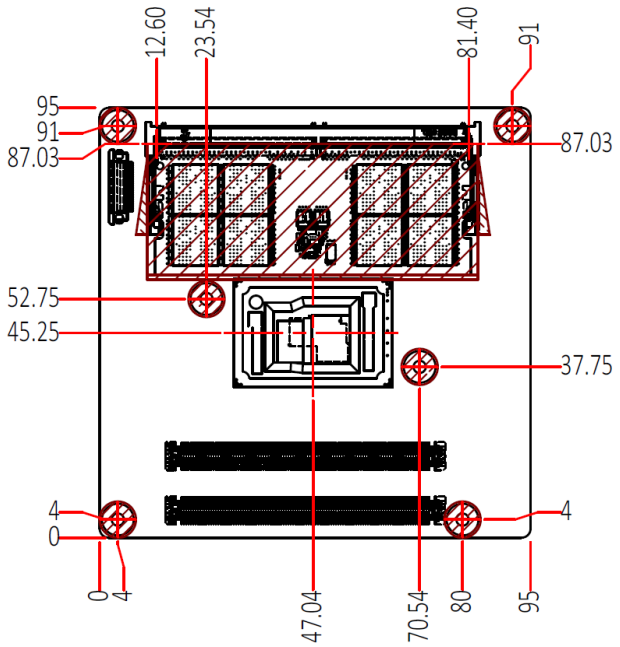
SYSTEM	Processor	Intel® Atom x7000RE series processors (Code Name : Amston Lake) Intel® Atom Processor x7835RE, 8 Cores, 1.3~3.6GHz, 12W Intel® Atom Processor x7433RE, 4 Cores, 1.5~3.4GHz, 9W Intel® Atom Processor x7211RE, 2 Cores, 1.0~3.2GHz, 6W Intel® Core™ 3 Processor N355, 8 Cores, 1.8~3.9GHz, 9/15W Intel® Processor N150, 4 Cores, 1.0~3.6GHz, 6W
	Memory	One 262-pin SODIMM up to 16GB Single Channel DDR5 4800MHz In-band ECC (IBECC) supported
	BIOS	AMI SPI 256Mbit
GRAPHICS	Controller	Intel® UHD
	Feature	DX12, Open GL 4.6, Vulkan 1.2 **HW Decode**: 4K60 10b 4:2:0, 4:4:4 HEVC/VP9/SCC, 4K60 10b 4:2:0 AV1 **HW Encode**: 4K60 10b 4:2:0, 4:4:4 HEVC/VP9/SCC
	Display	2 x DDI 1 x LVDS/eDP **LVDS**: dual channel 1920x1200 @60Hz **eDP**: 4096x2160 @60Hz
	Triple Displays	LVDS/eDP + 2 DDI (support 5 PCIe devices)
EXPANSION	Interface	Up to 8x PCIe x1 (Gen3)(3x PCIe x1 co-layout w/Ethernet and SATA, available upon request) 1 x I^2C 1 x SMBus 1 x LPC/eSPI (BOM option: eSPI; Default option: LPC) 2 x UART (TX/RX only) 1 x CAN (co-layout with UART)
AUDIO	Interface	HD Audio
ETHERNET	Controller	1 x Intel® I226 series (10/100/1000/2500Mbps), co-lay 1 x PCIe x1 (available upon request)
I/O	USB	2 x USB 3.2 Gen2 (option to 4 ports by USB hub) 8 x USB 2.0
	SATA	2 x SATA 3.0 (up to 6Gb/s), co-lay 2 x PCIe x1 (available upon request)
	eMMC5.1	1 x 64GB eMMC
	DIO	1 x 8-bit DIO

WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
SECURITY	TPM	TPM 2.0 (Option: fTPM)
Power	Type	8.5~20V, 5VSB, VCC_RTC (ATX mode) 8.5~12V, VCC_RTC (AT mode)
	Consumption	TBD
OS SUPPORT	Microsoft	Windows 11/10 IoT Enterprise 64-bit
	Linux	Linux
ENVIRONMENT	Temperature	Operating: -40 to 85°C for Amston Lake CPU sku, 0°C~60°C for Twin Lake CPU sku Storage: -40 to 85°C
	Humidity	Operating: 10 to 90% RH Storage: 10 to 90% RH
	MTBF	TBD
MECHANICAL	Dimensions	COM Express® Compact 95mm (3.74") x 95mm (3.74")
	Compliance	PICMG COM Express® R3.1, Type 6
STANDARDS AND CERTIFICATIONS	Certification	CE, FCC, RoHS

▶ Block Diagram



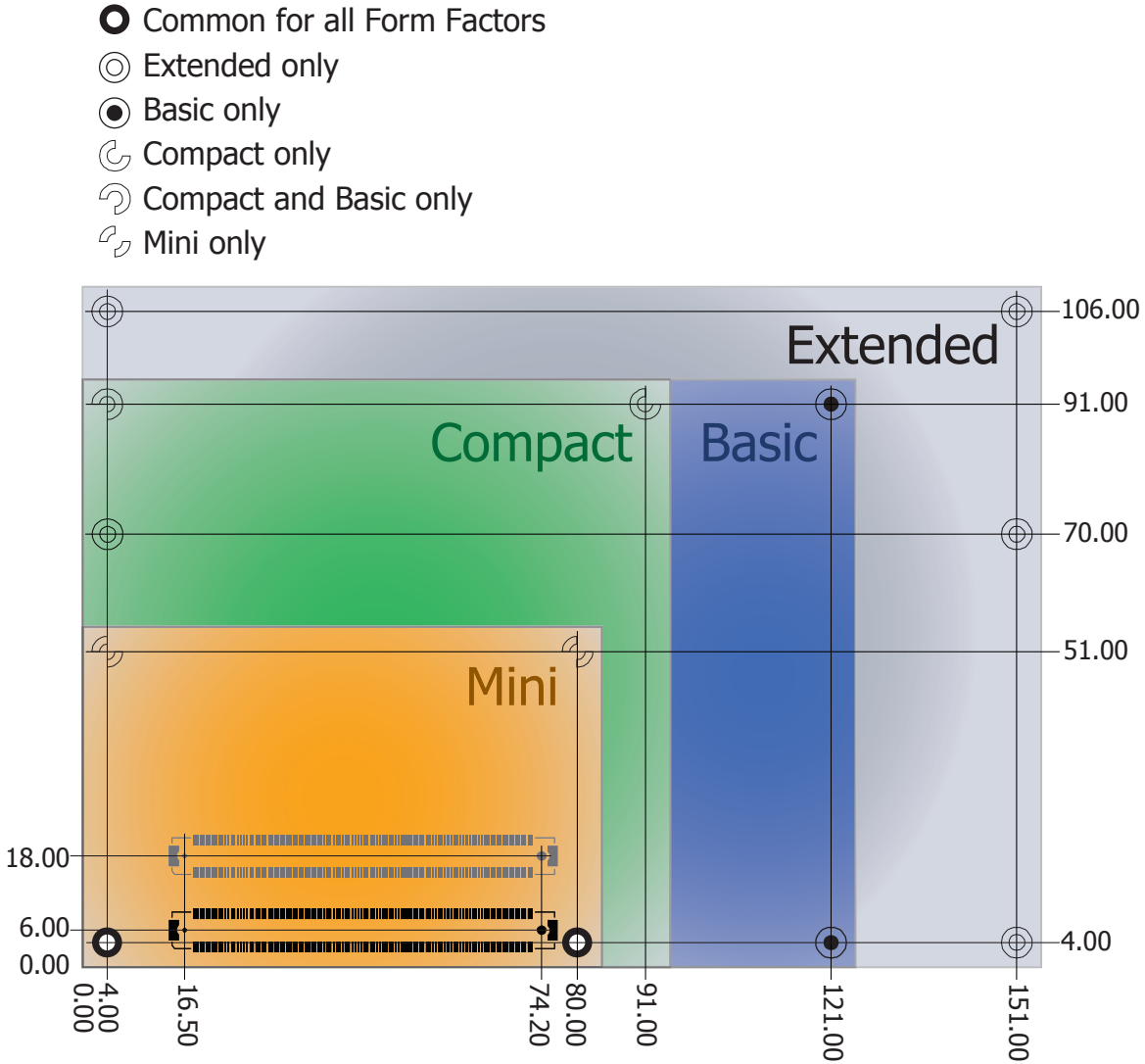
▶ Dimension



Chapter 2 - Concept

▶ COM Express Module Standards

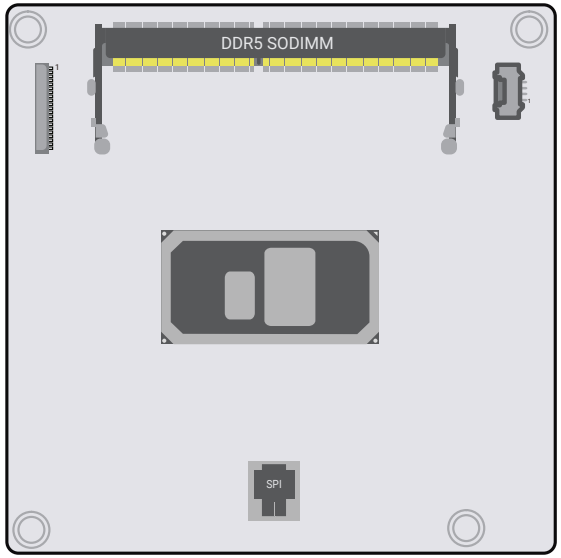
The figure below shows the dimensions of the different types of COM Express modules.
ASL968 is a COM Express compact. The dimension is 95mm x 95mm.



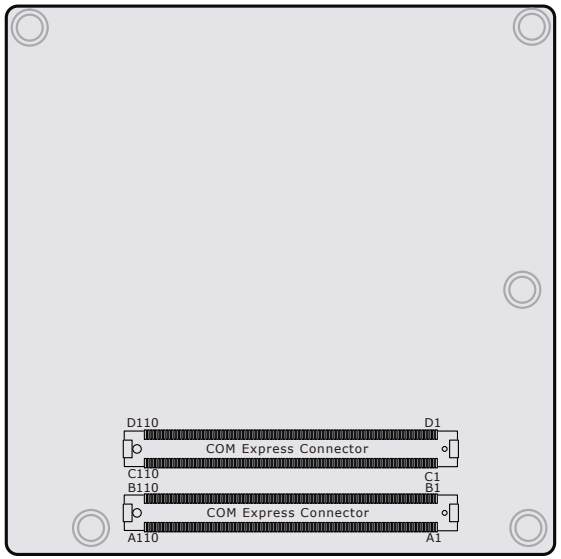
Chapter 3 - Hardware Installation

▶ Board Layout

TOP VIEW



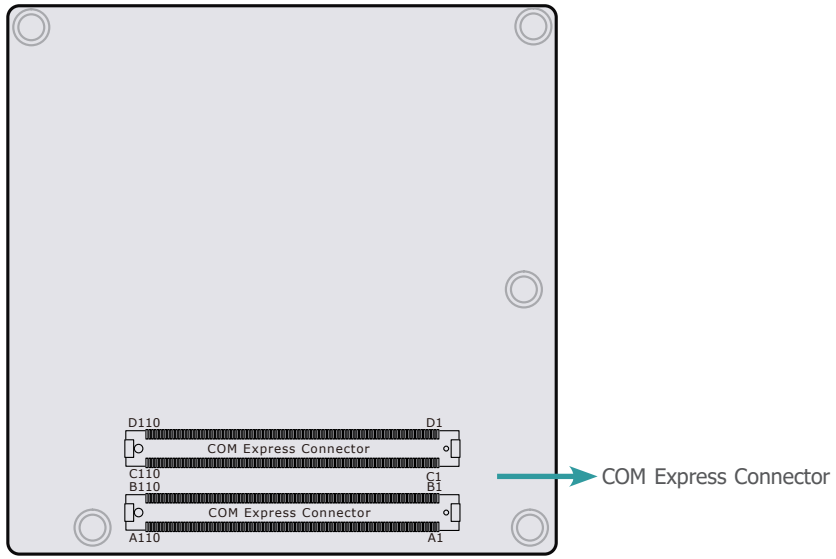
BOTTOM VIEW



▶ Connector

COM Express Connector

The COM Express connector is used to interface the ASL968 COM Express board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.Refer to the following pages for the pin functions of the connector.



▶ Module Pin-Out Types 6 and Optional Features

The table below shows the COM Express standard specifications and the corresponding specifications supported on the ASL968 module.
The features identified as Minimum (Min.) shall be implemented by all Modules.
Features identified up to Maximum (Max) may be additionally implemented by a Module.

Feature	Type 6 Min / Max
• System I/O	
PCI Express Lanes 0 - 5	1 / 6
PCI Express Lanes 6 - 15	0 / 2
PCI Express Lanes 16 - 31	0 / 16
PCI Express Graphics (PEG)	0 / 1
PCI Express Clock	1 / 1
10GBASE-KR LAN Ports 0 - 3	NA
NC-SI	NA
IPMB	NA
NBASE-T LAN Port 0	1 / 1
DDI 0	NA
DDIs 1 - 3	0 / 3
Singler Channel LVDS	0 / 1
Dual Channel LVDS	0 / 1
eDP on LVDS CH A pins	0 / 1
VGA Port	0 / 1
MIPI-CSI connectors	0 / 2
Serial Ports 1 - 2	0 / 2
CAN interface on SER1	0 / 1
SATA Ports	1 / 4
HD Audio	0 / 1
SoundWire Audio	0 / 1
USB 2.0 Ports	4 / 8

Feature	Type 6 Min / Max
• System I/O	
USB0 Client	0 / 1
USB7 Client	0 / 1
USB 3.2 Gen 1 or Gen 2 Ports	0 / 4
USB4 (on DDI pins)	0 / 2
LPC Bus or eSPI	1 / 1
Boot SPI Bus to Carrier / Carrier BIOS Flash Support	0 / 1
GP SPI	0 / 1
GPIO	8 / 8
SDIO (muxed on GPIO)	0 / 1
Rapid Shutdown	0 / 1

Feature	Type 6 Min / Max
• System Management	
SMBus	1 / 1
I2C	1 / 1
Watchdog Timer	0 / 1
Speaker Out	1 / 1
Carrier Board BIOS Flash Support	0 / 1
Reset Functions	1 / 1
Trusted Platform Module (on Module)	0 / 1
• Power Management	
Thermal Protection	0 / 1
Battery Low Alarm	0 / 1
Suspend/Wake Signals	0 / 3
Power Button Support	1 / 1
Power Good	1 / 1
VCC_5V_SBY Contacts	4 / 4
Sleep Input	0 / 1
Lid Input	0 / 1
Carrier Board Fan Control	0 / 1
• Power	
VCC_12V Contacts	24 / 24

▶ COM Express Connector Signal Description

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

AC97/HDA Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
AC/HDA_RST#	A30	O CMOS	3.3V Suspend/3.3V	Add series 33Ω and PD 100KΩ	Connect to CODEC pin 11 RESET#	Reset output to CODEC, active low.
AC/HDA_SYNC	A29	O CMOS	3.3V/3.3V	Add series 33Ω	Connect to CODEC pin 10 SYNC	Sample-synchronization signal to the CODEC(s).
AC/HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V	Add series 33Ω and PD 100KΩ	Connect to CODEC pin 6 BIT_CLK	Serial data clock generated by the external CODEC(s).
AC/HDA_SDOUT	A33	O CMOS	3.3V/3.3V	Add series 33Ω	Connect to CODEC pin 5 SDATA_OUT	Serial TDM data output to the CODEC.
AC/HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V	NC	NC	Serial TDM data inputs from up to 3 CODECs.
AC/HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V	Add series 0Ω and PD 100KΩ	Connect 33 Ω in series to CODEC1 pin 8 SDATA_IN	
AC/HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC0 pin 8 SDATA_IN	

Gigabit Ethernet Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
GBE0_MDI0+	A13	I/O MDI	Less than 3.3V May be active in Suspend		Connect to Magnetics Module MDI0+/-	Gigabit Ethernet Controller 0: Media Dependent Interface DifferentialPairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes or in 2.5, 5.0 and 10 Gbps modes. Some pairs are unused in some modes, per the following:
GBE0_MDI1+	A10	I/O MDI	Less than 3.3V May be active in Suspend		Connect to Magnetics Module MDI1+/-	
GBE0_MDI1-	A9	I/O MDI	Less than 3.3V May be active in Suspend			
GBE0_MDI2+	A7	I/O MDI	Less than 3.3V May be active in Suspend		Connect to Magnetics Module MDI2+/-	
GBE0_MDI2-	A6	I/O MDI	Less than 3.3V May be active in Suspend			
GBE0_MDI3+	A3	I/O MDI	Less than 3.3V May be active in Suspend		Connect to Magnetics Module MDI3+/-	
GBE0_MDI3-	A2	I/O MDI	Less than 3.3V May be active in Suspend			
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V	OD Buffer Output	Connect to LED and recommend current limit resistor 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 activity indicator, active low.
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V	OD Buffer Output	NC	Gigabit Ethernet Controller 0 link indicator, active low.
GBE0_LINK_MID#	A4	OD CMOS	3.3V Suspend/3.3V	OD Buffer Output	Connect to LED and recommend current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller MID Speed Link indicator. Active low. If active, the link is established but at a speed lower than the maximum speed supported by the Ethernet controller. Note that based on capabilities of the Ethernet controller used this signal might not be active for all possible lower link speeds. This Module pin should be capable of sinking up to 20 mA at a Voh of 0.4 max. Was GBE0_LINK100# in COM Express Rev. 3.0.
GBE0_LINK_MAX#	A5	OD CMOS	3.3V Suspend/3.3V	OD Buffer Output	Connect to LED and recommend current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller MAX Speed Link Indicator. Active low. If active, the link is established at the maximum link speed supported by the controller. This Module pin should be capable of sinking up to 20 mA at a Voh of 0.4 max. Was GBE0_LINK1000# in COM Express Rev. 3.0.
GBE0_CTREF	A14	REF	GND min 3.3V max	NC		

	1000BASE-T 2.5GBASE-T 5.0GBASE-T 10GBASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

SATA Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
SATA0_TX+	A16	O SATA	AC coupled on Module	0.01u AC Coupling capacitor	Connect to SATA0 Conn TX pin	Serial ATA or SAS Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module	0.01u AC Coupling capacitor		
SATA0_RX+	A19	I SATA	AC coupled on Module	0.01u AC Coupling capacitor	Connect to SATA0 Conn RX pin	Serial ATA or SAS Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module	0.01u AC Coupling capacitor		
SATA1_TX+	B16	O SATA	AC coupled on Module	0.01u AC Coupling capacitor	Connect to SATA1 Conn TX pin	Serial ATA or SAS Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module	0.01u AC Coupling capacitor		
SATA1_RX+	B19	I SATA	AC coupled on Module	0.01u AC Coupling capacitor	Connect to SATA1 Conn RX pin	Serial ATA or SAS Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module	0.01u AC Coupling capacitor		
SATA2_TX+	A22	O SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA2_TX-	A23	O SATA	AC coupled on Module	NA		
SATA2_RX+	A25	I SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA2_RX-	A26	I SATA	AC coupled on Module	NA		
SATA3_TX+	B22	O SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA3_TX-	B23	O SATA	AC coupled on Module	NA		
SATA3_RX+	B25	I SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA3_RX-	B26	I SATA	AC coupled on Module	NA		
ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V	Buffer Output	Connect to LED and **recommend** current limit resistor 220Ω to 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.

PCI Express Lanes Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
PCIE_TX0+	A68	O PCIE	AC coupled on Module	0.22u AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 0
PCIE_TX0-	A69			0.22u AC Coupling capacitor		
PCIE_RX0+	B68	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.22uF **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 0
PCIE_RX0-	B69					
PCIE_TX1+	A64	O PCIE	AC coupled on Module	0.22u AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 1
PCIE_TX1-	A65			0.22u AC Coupling capacitor		
PCIE_RX1+	B64	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.22uF **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 1
PCIE_RX1-	B65					
PCIE_TX2+	A61	O PCIE	AC coupled on Module	0.22u AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 2
PCIE_TX2-	A62			0.22u AC Coupling capacitor		
PCIE_RX2+	B61	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.22uF **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 2
PCIE_RX2-	B62					
PCIE_TX3+	A58	O PCIE	AC coupled on Module	0.22u AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 3 (This Port is BOM Option with On board LAN)
PCIE_TX3-	A59			0.22u AC Coupling capacitor		
PCIE_RX3+	B58	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.22uF (This Port is BOM Option with On board LAN) **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 3 (This Port is BOM Option with On board LAN)
PCIE_RX3-	B59					
PCIE_TX4+	A55	O PCIE	AC coupled on Module	0.22u AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 4
PCIE_TX4-	A56			0.22u AC Coupling capacitor		

▶ COM Express Connector Signal Description

PCI Express Lanes Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
PCIE_RX4+	B55	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.22uF **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 4
PCIE_RX4-	B56					
PCIE_TX5+(Optional to SATA1 Port)	A52	O PCIE	AC coupled on Module	Optional	Optional to PCIe or SATA0(Default: SATA1) Device - Connect AC Coupling cap 0.22uF Slot - Connect to PCIE Conn pin	PCI Express differential transmit pairs 5 (This Port is BOM Option with SATA1)
PCIE_TX5-(Optional to SATA1 Port)	A53			Optional		
PCIE_RX5+(Optional to SATA1 Port)	B52	I PCIE	AC coupled off Module	Optional	Optional to PCIe or SATA0(Default: SATA1) **Device** - Connect AC Coupling cap 0.22uF **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 5 (This Port is BOM Option with SATA1)
PCIE_RX5-(Optional to SATA1 Port)	B53			Optional		
PCIE_TX6+ (Optional to SATA0 port)	D19	O PCIE	AC coupled on Module	Optional	Optional to PCIe or SATA0(Default: SATA0) **Device** - Connect AC Coupling cap 0.22uF Slot - Connect to PCIE Conn pin	PCI Express differential transmit pairs 6 (This Port is BOM Option with SATA0)
PCIE_TX6- (Optional to SATA0 port)	D20			Optional		
PCIE_RX6+(Optional to SATA0 port)	C19	I PCIE	AC coupled off Module	Optional	Optional to PCIe or SATA0(Default: SATA0) **Device** - Connect AC Coupling cap 0.22uF **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 6(This Port is BOM Option with SATA0)
PCIE_RX6-(Optional to SATA0 port)	C20			Optional		
PCIE_TX7+ (Optional to SATA port)	D22	O PCIE	AC coupled on Module	Optional	Optional to PCIe or On board LAN (Default: On board LAN) **Device** - Connect AC Coupling cap 0.22uF **Slot** - Connect to PCIE Conn pin	PCI Express differential transmit pairs 7(This Port is BOM Option with On board LAN)
PCIE_TX7- (Optional to SATA port)	D23			Optional		
PCIE_RX7+ (Optional to SATA port)	C22	I PCIE	AC coupled off Module	Optional	Optional to PCIe or On board LAN (Default: On board LAN) **Device** - Connect AC Coupling cap 0.22uF **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 7(This Port is BOM Option with On board LAN)
PCIE_RX7- (Optional to SATA port)	C23			Optional		
PCIE0_CK_REF+	A88	O PCIE	PCIE		Connect to PCIE device, **PCIe CLK Buffer** or slot	Reference clock output for all PCI Express and PCI Express Graphicslanes.
PCIE0_CK_REF-	A89					

PEG Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V	NA		PCI Express Graphics lane reversal input strap. Pull low on the Carrierboard to reverse lane order.

DDI Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
DDI1_PAIR0+/USB4_1_SSTX0+	D26	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI1_PAIR0-/ USB4_1_SSTX0-	D27				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR1+/USB4_1_SSRX0+	D29	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 1 differential pairs/Serial Digital Video B green output differential pair
DDI1_PAIR1-/USB4_1_SSRX0-	D30				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR2+/USB4_1_SSTX1+	D32	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI1_PAIR2-/USB4_1_SSTX1-	D33				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR3+/ USB4_1_SSRX1+	D36	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 3 differential pairs/Serial Digital Video B clock output differential pair.
DDI1_PAIR3-/ USB4_1_SSRX1-	D37				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_CTRLCLK_AUX+/ USB4_1_AUX+	D15	I/O PCIE	AC coupled on Module	PD 100K to GND **(S/W IC between Rpu/PCH)**	Connect to DP AUX+	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND **(S/W IC between Rpu/Rpd resistor)**	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high
DDI1_CTRLCLK_AUX-/ USB4_1_AUX -	D16	I/O PCIE	AC coupled on Module	PU 100K to 3.3V **(S/W IC between Rpu/PCH)**	Connect to DP AUX-	DP AUX- function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V **(S/W IC between 2.2K/100K resistor)**	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high
DDI1_HPD	C24	I CMOS	3.3V / 3.3V	PD 100K to GND	PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI1_DDC_AUX_SEL	D34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort
DDI2_PAIR0+	D39	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI2_PAIR0-	D40				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR1+	D42	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 1 differential pairs/Serial Digital Video B grenn output differential pair
DDI2_PAIR1-	D43				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR2+	D46	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI2_PAIR2-	D47				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR3+	D49	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 3 differential pairs/Serial Digital Video B clock output differential pair
DDI2_PAIR3-	D50				Connect AC Coupling Capacitors 0.1uF to Device	

▶ COM Express Connector Signal Description

DDI Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
DDI2_CTRLCLK_AUX+	C32	I/O PCIE	AC coupled on Module	PD 100K to GND **(S/W IC between Rpu/PCH)**	Connect to DP AUX+	DP AUX+ function if DDI2_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND **(S/W IC between Rpu/Rpd resistor)**	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high
DDI2_CTRLDATA_AUX-	C33	I/O PCIE	AC coupled on Module	PU 100K to 3.3V **(S/W IC between Rpu/PCH)**	Connect to DP AUX-	DP AUX- function if DDI2_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V **(S/W IC between 2.2K/100K resistor)**	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high
DDI2_HPD	D44	I CMOS	3.3V / 3.3V	PD 100K to GND	PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI2_DDC_AUX_SEL	C34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohmresistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort
DDI3_PAIR0+	C39	O PCIE	AC coupled off Module	NA	Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI3_PAIR0-	C40			NA	Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_PAIR1+	C42	O PCIE	AC coupled off Module	NA	Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 1 differential pairs/Serial Digital Video B green output differential pair
DDI3_PAIR1-	C43			NA	Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_PAIR2+	C46	O PCIE	AC coupled off Module	NA	Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI3_PAIR2-	C47			NA	Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_PAIR3+	C49	O PCIE	AC coupled off Module	NA	Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 3 differential pairs/Serial Digital Video B clock output differential pair
DDI3_PAIR3-	C50			NA	Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_CTRLCLK_AUX+	C36	I/O PCIE	AC coupled on Module	NA	Connect to DP AUX+	DP AUX+ function if DDI3_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	NA	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high
DDI3_CTRLDATA_AUX-	C37	I/O PCIE	AC coupled on Module	NA	Connect to DP AUX-	DP AUX- function if DDI3_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	NA	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high
DDI3_HPD	C44	I CMOS	3.3V / 3.3V	NA	PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI3_DDC_AUX_SEL	C38	I CMOS	3.3V / 3.3V	NA	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort

USB Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
USB0+	A46	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 0
USB0-	A45					
USB1+	B46	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 1
USB1-	B45					
USB2+	A43	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 2
USB2-	A42					
USB3+	B43	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 3
USB3-	B42					
USB4+	A40	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 4
USB4-	A39					
USB5+	B40	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 5
USB5-	B39					
USB6+	A37	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 6
USB6-	A36					
USB7+	B37	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 7, USB7 may be configured as a USB client or as a host, or both, at the Module designer's discretion.(CR901-B default set as a host)
USB7-	B36					

▶ COM Express Connector Signal Description

USB Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	Add isolation Diode and PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	Add isolation Diode and PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.3V	Add isolation Diode and PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.3V	Add isolation Diode and PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_SSTX0+	D4	O PCIE	AC coupled on Module	0.1u AC Coupling capacitor	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX0-	D3					
USB_SSRX0+	C4	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX0-	C3					
USB_SSTX1+	D7	O PCIE	AC coupled on Module	0.1u AC Coupling capacitor	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX1-	D6					
USB_SSRX1+	C7	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX1-	C6					
USB_SSTX2+	D10	O PCIE	AC coupled on Module	0.1u AC Coupling capacitor **(Default NA ; BOM Option)**	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX2-	D9					
USB_SSRX2+	C10	I PCIE	AC coupled off Module	**Default NA ; BOM Option)**	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX2-	C9					
USB_SSTX3+	D13	O PCIE	AC coupled on Module	0.1u AC Coupling capacitor **(Default NA ; BOM Option)**	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX3-	D12					
USB_SSRX3+	C13	I PCIE	AC coupled off Module	**Default NA ; BOM Option)**	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX3-	C12					

LVDS Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
LVDS_A0+	A71	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board
LVDS_A0-	A72					
LVDS_A1+	A73	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A1-	A74					
LVDS_A2+	A75	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A2-	A76					
LVDS_A3+	A78	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A3-	A79					
LVDS_A_CK+	A81	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential clock
LVDS_A_CK-	A82					
LVDS_B0+	B71	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board
LVDS_B0-	B72					
LVDS_B1+	B73	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B1-	B74					
LVDS_B2+	B75	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B2-	B76					
LVDS_B3+	B77	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B3-	B78					
LVDS_B_CK+	B81	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel B differential clock
LVDS_B_CK-	B82					
LVDS_VDD_EN	A77	O CMOS	3.3V / 3.3V	PD 100K to GND	Connect to enable control of LVDS panel power circuit	LVDS panel power enable
LVDS_BKLT_EN	B79	O CMOS	3.3V / 3.3V	PD 100K to GND	Connect to enable control of LVDS panel backlight power circuit.	LVDS panel backlight enable
LVDS_BKLT_CTRL	B83	O CMOS	3.3V / 3.3V	PD 100K to GND	Connect to brightness control of LVDS panel backlight power circuit.	LVDS panel backlight brightness control
LVDS_I2C_CK	A83	I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V	Connect to DDC clock of LVDS panel	I2C clock output for LVDS display use
LVDS_I2C_DAT	A84	I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V	Connect to DDC data of LVDS panel	I2C data line for LVDS display use

▶ COM Express Connector Signal Description

eDP Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
eDP_TX2+	A71	O LV_DIFF	AC coupled off module		Connect to eDP connector	eDP differential pairs
eDP_TX2-	A72					
eDP_TX1+	A73	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_TX1-	A74					
eDP_TX0+	A75	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_TX0-	A76					
eDP_TX3+	A81	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_TX3-	A82					
eDP_VDD_EN	A77	O CMOS	3.3V / 3.3V	PD 100K to GND	Connecto to enable eDP power.	eDP power enable
eDP_BKLT_EN	B79	I/O LV_DIFF	AC couple off module	PD 100K to GND	Connect to enable control of eDP backlight power circuit.	eDP backlight enable
eDP_BKLT_CTRL	B83	O CMOS	3.3V / 3.3V	PD 100K to GND	Connect to brightness control of eDP panel backlight power circuit.	eDP backlight brightness control
eDP_AUX+	A83	I/O LV_DIFF	AC couple off module		eDP AUX+	I2C clock output for LVDS display use
eDP_AUX-	A84	I/O LV_DIFF			eDP AUX-	I2C data line for LVDS display use
eDP_HPD	A87	I CMOS	3.3V / 3.3V		eDP connector hot plug detection	Detection of Hot Plug/ Unplug and notification of the link layer

LPC & eSPI Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
LPC_AD0	B4	I/O CMOS	3.3V / 3.3V	LPC_ADC0 (ESPI to LPC bridge)	Connect to LPC device	LPC & eSPI multi-function pin with bridge (LPC Bus support only)
LPC_AD1	B5			LPC_ADC1 (ESPI to LPC bridge)		
LPC_AD2	B6			LPC_ADC2 (ESPI to LPC bridge)		
LPC_AD3	B7			LPC_ADC3 (ESPI to LPC bridge)		
LPC_FRAME#	B3	O CMOS	3.3V / 3.3V	LPC_FRAME# (ESPI to LPC bridge)		LPC frame indicates the start of an LPC cycle
LPC_DRQ0#	B8	I CMOS	3.3V / 3.3V	PU 10K to 3V3		NA (No support)
LPC_DRQ1#	B9			PU 10K to 3V3		
LPC_SERIRQ	A50	I/O CMOS	3.3V / 3.3V	LPC_SERIRQ(ESPI to LPC bridge)		LPC serial interrupt
LPC_CLK	B10	O CMOS	3.3V / 3.3V	LPC_CLK (Default 24MHz)		LPC clock output - 24MHz nominal

SPI Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
SPI_CS#	B97	O CMOS	3.3V Suspend/3.3V	Add series 0Ω	**Connect a series resistor 0Ω to Carrier Board SPI Device CS# pin**	Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1
SPI_MISO	A92	I CMOS	3.3V Suspend/3.3V	Add series 0Ω	**Connect a series resistor 33Ω to Carrier Board SPI Device SO pin**	Data in to Module from Carrier SPI
SPI_MOSI	A95	O CMOS	3.3V Suspend/3.3V	Add series 0Ω	**Connect a series resistor 33Ω to Carrier Board SPI Device SI pin**	Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend/3.3V	Add series 0Ω	**Connect a series resistor 33Ω to Carrier Board SPI Device SCK pin**	Clock from Module to Carrier SPI
SPI_POWER	A91	O	3.3V Suspend/3.3V			Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier
BIOS_DIS0#	A34	I CMOS	NA	PU 10K to 3V3SB_EC		Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to COM Express Module Base Specification Revision 2.1 for strapping options of BIOS disable signals.
BIOS_DIS1#	B88			PU 10K to 3V3SB_EC		

BIOS DIS1#	BIOS DIS0#	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	RefLine
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	0	Module	Module	High	Module	Carrier FWH	1
0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	**0**	**Carrier (Default)**	**Module (Default)**	**SPI1 (Default)**	**Module (Default)**	**SPI0/SPI1 (Default)**	**3**

▶ COM Express Connector Signal Description

VGA Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
VGA_RED	B89	O Analog	Analog	NA	**PD 150R,connect to VGA connector with EMI filter & ESD protect component.**	Red for monitor. Analog output
VGA_GRN	B91	O Analog	Analog	NA	**PD 150R,connect to VGA connector with EMI filter & ESD protect component.**	Green for monitor. Analog output
VGA_BLU	B92	O Analog	Analog	NA	**PD 150R,connect to VGA connector with EMI filter & ESD protect component.**	Blue for monitor. Analog output
VGA_HSYNC	B93	O CMOS	3.3V / 3.3V	NA	**Connect to VGA connector with a3.3V Buffer IC to isolate PCH & Display Device**	Horizontal sync output to VGA monitor
VGA_VSYNC	B94	O CMOS	3.3V / 3.3V	NA	**Connect to VGA connector with a 33V Buffer IC to isolate PCH & Display Device**	Vertical sync output to VGA monitor
VGA_I2C_CK	B95	I/O OD CMOS	3.3V / 3.3V	NA	**Connect to VGA connector with a 3.3V to 5V Level shift circuit.**	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)
VGA_I2C_DAT	B96	I/O OD CMOS	3.3V / 3.3V	NA	**Connect to VGA connector with a 3.3V to 5V Level shift circuit.**	DDC data line.

Serial Interface Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
SER0_TX	A98	O CMOS	3.3V / 12V	Add series isolation diode for older COME spec.	PD 4.7K to GND	General purpose serial port 0 transmitter **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SER0_RX	A99	I CMOS	3.3V / 12V	Add series isolation diode for older COME spec PU 10K to 3V3		General purpose serial port 0 receiver **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SER1_TX	A101	O CMOS	3.3V / 12V	Add series isolation diode for older COME spec	PD 4.7K to GND	General purpose serial port 1 transmitter **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SER1_RX	A102	I CMOS	3.3V / 12V	Add series isolation diode for older COME spec PU 10K to 3V3		General purpose serial port 1 receiver **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**

Power and System Management Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	ASL968	Carrier Board	Description
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3SB_EC	PU 4.7K to 3V3SB	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	Add series isolation diode and PU 10K to 3V3SB	NC PU 4.7K to 3V3SB	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# isnot able to reestablish control of the system, PWR_OK or a powercycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V	Buffer out w/22Ω series resistor		Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimumspecification, a watchdog timeout, or may be initiated by the Module software.
PWR_OK	B24	I CMOS	3.3V / 3.3V	Add series isolation diode and PU 10K to 5V and PD 20K		Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
SUS_STAT#	B18	O CMOS	3.3V Suspend/3.3V	NA		Indicates imminent suspend operation; used to notify LPC devices.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V	PD 100K to GND		Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V	PD 100K to GND		Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V	PD 100K to GND		Indicates system is in Soft Off state.
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3SB		PCI Express wake up signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3SB		General purpose wake up signal. May be used to implement wake-upon PS2 keyboard or mouse activity.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10K to 3V3SB		Indicates that external battery is low. This port provides a battery-low signal to the Module for orderlytransitioning to power saving or power cut-off ACPI modes.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47K to 3V3SB_EC		LID switch. Low active signal used by the ACPI operating system for a LID switch. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 47K to 3V3SB_EC		Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
THRM#	B35	I CMOS	3.3V / 3.3V	Add series isolation diode and PU 10K to 3V3		Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 10K to 3.3V		Active low output indicating that the CPU has entered thermal shutdown.
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3SB_EC		System Management Bus bidirectional clock line.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	Add series isolation diode and PU 10K to 3V3SB	NC PU 4.7K to 3V3SB	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power.
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3SB_EC		System Management Bus bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3SB_EC		System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.

▶ COM Express Connector Signal Description

GPIO Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	ASL968	Carrier Board	Description
GPO0	A93	O CMOS	3.3V / 3.3V			General purpose output pins. **Upon a hardware reset, these outputs should be low.**
GPO1	B54					
GPO2	B57					
GPO3	B63					
GPI0	A54	I CMOS	3.3V / 3.3V	PU 10K to 3.3V		General purpose input pins. **Pulled high internally on the Module.**
GPI1	A63			PU 10K to 3.3V		
GPI2	A67			PU 10K to 3.3V		
GPI3	A85			PU 10K to 3.3V		

Power and GND Signal Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	ASL968	Carrier Board	Description
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power				Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.
VCC_5V_SBY	B84~B87	Power				Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected ifthese functions are not used in the system design.
VCC_RTC	A47	Power				Real-time clock circuit-power input. Nominally +3.0V.
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110, C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Power				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to CarrierBoard GND plane.

Miscellaneous Signal Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
I2C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 1K to 3.3VSB		General purpose I2C port clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 1K to 3.3VSB		General purpose I2C port data I/O line
SPKR	B32	O CMOS	3.3V / 3.3V	PU 10K to 3V3		Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.
WDT	B27	O CMOS	3.3V / 3.3V	PD 100K to GND		Output indicating that a watchdog time-out event has occurred.
FAN_PWNOUT	B101	O OD CMOS	3.3V / 3.3V			Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
FAN_TACHIN	B102	I OD CMOS	3.3V / 3.3V			Fan tachometer input for a fan with a two pulse output. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
TPM_PP	A96	I CMOS	3.3V / 3.3V	PD 10K to GND		Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.

▶ COM Express Connector Signal Description

PEG Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	ASL968	Carrier Board	Description
PEG_TX0+	D52	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 0
PEG_TX0-	D53			NA		
PEG_RX0+	C52	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 0
PEG_RX0-	C53			NA		
PEG_TX1+	D55	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 1
PEG_TX1-	D56			NA		
PEG_RX1+	C55	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 1
PEG_RX1-	C56			NA		
PEG_TX2+	D58	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 2
PEG_TX2-	D59			NA		
PEG_RX2+	C58	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 2
PEG_RX2-	C59			NA		
PEG_TX3+	D61	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 3
PEG_TX3-	D62			NA		
PEG_RX3+	C61	I PCIE	AC coupled off Module	NA		PEG channel 3, Receive Input differential pair 3
PEG_RX3-	C62			NA		
PEG_TX4+	D65	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 4
PEG_TX4-	D66			NA		
PEG_RX4+	C65	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 4
PEG_RX4-	C66			NA		
PEG_TX5+	D68	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 5
PEG_TX5-	D69			NA		
PEG_RX5+	C68	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 5
PEG_RX5-	C69			NA		
PEG_TX6+	D71	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 6
PEG_TX6-	D72			NA		
PEG_RX6+	C71	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 6
PEG_RX6-	C72			NA		
PEG_TX7+	D74	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 7
PEG_TX7-	D75			NA		
PEG_RX7+	C74	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 7
PEG_RX7-	C75			NA		
PEG_TX8+	D78	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 8
PEG_TX8-	D79			NA		
PEG_RX8+	C78	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 8
PEG_RX8-	C79			NA		
PEG_TX9+	D81	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 9
PEG_TX9-	D82			NA		
PEG_RX9+	C81	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 9
PEG_RX9-	C82			NA		
PEG_TX10+	D85	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 10
PEG_TX10-	D86			NA		
PEG_RX10+	C85	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 10
PEG_RX10-	C86			NA		
PEG_TX11+	D88	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 11
PEG_TX11-	D89			NA		
PEG_RX11+	C88	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 11
PEG_RX11-	C89			NA		
PEG_TX12+	D91	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 12
PEG_TX12-	D92			NA		
PEG_RX12+	C91	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 12
PEG_RX13-	C92			NA		
PEG_TX13+	D94	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 13
PEG_TX13-	D95			NA		
PEG_RX13+	C94	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 13
PEG_RX12-	C95			NA		
PEG_RX13-	C92			NA		
PEG_TX14+	D98	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 14
PEG_TX14-	D99			NA		
PEG_RX14+	C98	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 14
PEG_RX14-	C99			NA		
PEG_TX15+	D101	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 15
PEG_TX15-	D102			NA		
PEG_RX15+	C101	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 15
PEG_RX15-	C102			NA		

▶ COM Express Pin Assignments

Pin List for Pin-Out Type 6

The table below is a comprehensive list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 6 in the PICMG COM.0 R3.1 specification.

Pin	Row A	ASL968 Difference	Row B	ASL968 Difference
1	GND (FIXED)		GND (FIXED)	
2	GBE0_MDI3-		GBE0_ACT#	
3	GBE0_MDI3+		LPC_FRAME#/ESPI_CS0#	
4	GBE0_LINKMID#	GBE_LED1000#	LPC_AD0/ESPI_IO_0	
5	GBE0_LINKMAX#	GBE_LED2500#	LPC_AD1/ESPI_IO_1	
6	GBE0_MDI2-		LPC_AD2/ESPI_IO_2	
7	GBE0_MDI2+		LPC_AD3/ESPI_IO_3	
8	GBE0_LINK#		LPC_DRQ0#/ESPI_ALERT0#	PU 10K to 3.3V
9	GBE0_MDI1-		LPC_DRQ1#/ESPI_ALERT1#	PU 10K to 3.3V
10	GBE0_MDI1+		LPC_CLK/ESPI_CK	
11	GND (FIXED)		GND (FIXED)	
12	GBE0_MDI0-		PWRBTN#	
13	GBE0_MDI0+		SMB_CK	
14	GBE0_CTREF	NC	SMB_DAT	
15	SUS_S3#		SMB_ALERT#	
16	SATA0_TX+		SATA1_TX+	
17	SATA0_TX-		SATA1_TX-	
18	SUS_S4#		SUS_STAT#	NC
19	SATA0_RX+		SATA1_RX+	
20	SATA0_RX-		SATA1_RX-	
21	GND (FIXED)		GND (FIXED)	
22	SATA2_TX+	NA	SATA3_TX+	NA
23	SATA2_TX-	NA	SATA3_TX-	NA
24	SUS_S5#		PWR_OK	
25	SATA2_RX+	NA	SATA3_RX+	NA
26	SATA2_RX-	NA	SATA3_RX-	NA
27	BATLOW#		WDT	
28	(S)ATA_ACT#		HDA_SDN2	NC
29	HDA_SYNA		HDA_SDIN1	
30	HDA_RST#		HDA_SDIN0	
31	GND (FIXED)		GND (FIXED)	
32	HDA_BITCLK		SPKR	
33	HDA_SDOUT		I2C_CK	
34	BIOS_DIS0#		I2C_DAT	
35	THRMTRIP#		THRM#	
36	USB6-		USB7-	
37	USB6+		USB7+	
38	USB_6_7_OC#		USB_4_5_OC#	
39	USB4-		USB5-	
40	USB4+		USB5+	
41	GND (FIXED)		GND (FIXED)	
42	USB2-		USB3-	
43	USB2+		USB3+	
44	USB_2_3_OC#		USB_0_1_OC#	
45	USB0-		USB1-	
46	USB0+		USB1+	
47	VCC_RTC		ESPI_EN#	NC
48	RSMRST_OUT#		USB0_HOST_PRSNT	NC
49	GBE0_SDP		SYS_RESET#	
50	LPC_SERIRQ		CB_RESET#	
51	GND (FIXED)		GND (FIXED)	
52	PCIE_TX5+**Note		PCIE_RX5+ **Note	
53	PCIE_TX5- *Note		PCIE_RX5- **Note	
54	GPI0		GPO1	
55	PCIE_TX4+		PCIE_RX4+	
56	PCIE_TX4-		PCIE_RX4-	

Pin	Row A	ASL968 Difference	Row B	ASL968 Difference
57	GND		GPO2	
58	PCIE_TX3+		PCIE_RX3+	
59	PCIE_TX3-		PCIE_RX3-	
60	GND (FIXED)		GND (FIXED)	
61	PCIE_TX2+		PCIE_RX2+	
62	PCIE_TX2-		PCIE_RX2-	
63	GPI1		GPO3	
64	PCIE_TX1+		PCIE_RX1+	
65	PCIE_TX1-		PCIE_RX1-	
66	GND		WAKE0#	
67	GPI2		WAKE1#	
68	PCIE_TX0+		PCIE_RX0+	
69	PCIE_TX0-		PCIE_RX0-	
70	GND (FIXED)		GND (FIXED)	
71	LVDS_A0+/eDP_TX2+**Note		LVDS_B0+	
72	LVDS_A0-/eDP_TX2-**Note		LVDS_B0-	
73	LVDS_A1+/eDP_TX1+**Note		LVDS_B1+	
74	LVDS_A1-/eDP_TX1-**Note		LVDS_B1-	
75	LVDS_A2+/eDP_TX0+**Note		LVDS_B2+	
76	LVDS_A2-/eDP_TX0-**Note		LVDS_B2-	
77	LVDS_VDD_EN/ eDP_VDD_EN **Note		LVDS_B3+	
78	LVDS_A3+		LVDS_B3-	
79	LVDS_A3-		LVDS_BKLT_EN/ eDP_BKLT_EN**Note	
80	GND (FIXED)		GND (FIXED)	
81	LVDS_A_CK+/ eDP_TX3+**Note		DDI0_PAIR3+	
82	LVDS_A_CK-/ eDP_TX3-**Note		DDI0_PAIR3-	
83	LVDS_I2C_CK/ eDP_AUX+**Note		LVDS_BKLT_TRL/ eDP_BKLT_CTRL**Note	
84	LVDS_I2C_DAT/ eDP_AUX-**Note		VCC_5V_SBY	

Pin	Row A	ASL968 Difference	Row B	ASL968 Difference
85	GPI3		VCC_5V_SBY	
86	GP_SPI_MOSI		VCC_5V_SBY	
87	eDP_HPD**		VCC_5V_SBY	
88	PCIE_CLK_REF+		BIOS_DIS1#	
89	PCIE_CLK_REF-		DDI0_HPD	
90	GND(FIXED)		GND(FIXED)	
91	SPI_POWER		VGA_GRN	NA
92	SPI_MISO		VGA_BLU	NA
93	GPO0		VGA_HSYNA	NA
94	SPI_CLK		VGA_VSYNA	NA
95	SPI_MOSI		VGA_I2C_CK	NA
96	TPM_PP		VGA_I2C_DAT	NA
97	TYPE10#	NC	SPI_CS#	
98	SER0_TX		GP_SPI_MISO	
99	SER0_RX		GP_SPI_CK	
100	GND (FIXED)		GND (FIXED)	
101	SER1_TX		FAN_PWMOUT	
102	SER1_RX		FAN_TACHIN	
103	LID#		SLEEP#	
104	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
105	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
106	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
107	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
108	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
109	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
110	GND(FIXED)		GND(FIXED)	

Note:
1. ** PCIE_TX5+/-, PCIE_RX5+/-(in place of SATA1) are BOM option supported by project basis.
2. ** eDP (in place of LVDS) is BOM option supported by project basis.
3. For PCIe device down components on the carrier board, please use and place on the PCIe Lane0 port first.

	Row C	ASL968 Difference		Row D	ASL968 Difference
1	GND (FIXED)		1	GND (FIXED)	
2	GND		2	GND	
3	USB_SSRX0-		3	USB_SSTX0-	
4	USB_SSRX0+		4	USB_SSTX0+	
5	GND		5	GND	
6	USB_SSRX1-		6	USB_SSTX1-	
7	USB_SSRX1+		7	USB_SSTX1+	
8	GND		8	GND	
9	USB_SSRX2-	NA**Note	9	USB_SSTX2-	NA**Note
10	USB_SSRX2+	NA**Note	10	USB_SSTX2+	NA**Note
11	GND (FIXED)		11	GND (FIXED)	
12	USB_SSRX3-	NA**Note	12	USB_SSTX3-	NA**Note
13	USB_SSRX3+	NA**Note	13	USB_SSTX3+	NA**Note
14	GND		14	GND	
15	USB4_1_LSTX	NA	15	DDI1_CTRLCLK_AUX+/ USB4_1_AUX+	USB4 is not supported.
16	USB4_1_LSRX	NA	16	DDI1_CTRLDATA_AUX-/ USB4_1_AUX-	USB4 is not supported.
17	USB4_RT_ENA	NA	17	USB4_PD_I2C_ALERT#	USB4 is not supported.
18	GND_C18		18	PMCALERT#	NA
19	PCIE_RX6+**Note		19	PCIE_TX6+**Note	
20	PCIE_RX6-**Note		20	PCIE_TX6-**Note	
21	GND (FIXED)		21	GND (FIXED)	
22	PCIE_RX7+**Note		22	PCIE_TX7+**Note	
23	PCIE_RX7-**Note		23	PCIE_TX7-**Note	
24	DDI1_HPD		24	GND_D24	
25	SML0_CLK		25	GND_D25	
26	SML0_DAT		26	DDI1_PAIR0+/ USB4_1_SSTX0+	USB4 is not supported.
27	SML1_CLK		27	DDI1_PAIR0-/ USB4_1_SSTX0-	USB4 is not supported.

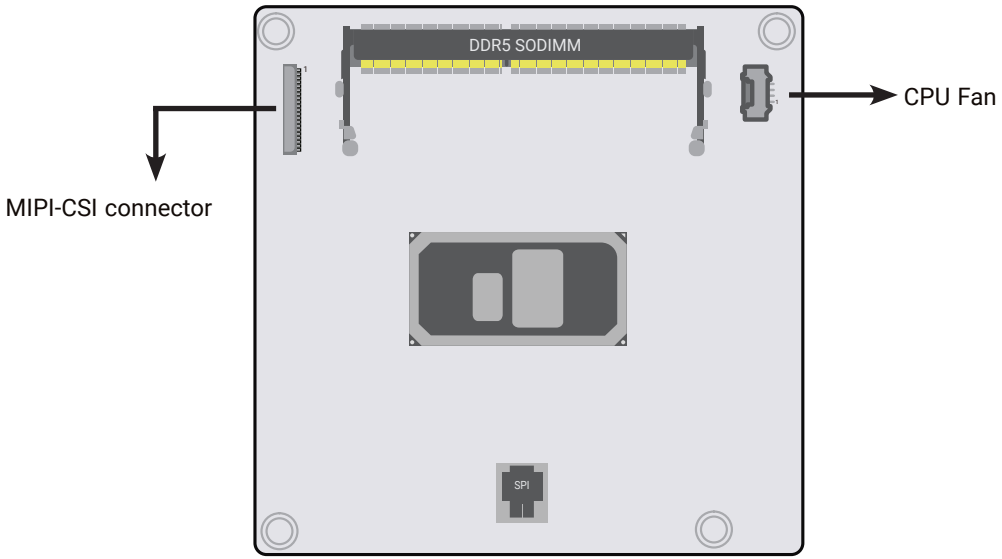
	Row C	ASL968 Difference		Row D	ASL968 Difference
28	SML1_DAT		28	GND_D28	
29	USB4_PD_I2C_CLK	NA	29	DDI1_PAIR1+/ USB4_1_SSRX0+	USB4 is not supported.
30	USB4_PD_I2C_DAT	NA	30	DDI1_PAIR1-/ USB4_1_SSRX0-	USB4 is not supported.
31	GND (FIXED)		31	GND (FIXED)	
32	DDI2_CTRLCLK_AUX+ / USB4_2_AUX+	USB4 is not supported.	32	DDI1_PAIR2+/ USB4_1_SSTX1+	USB4 is not supported.
33	DDI2_CTRLDATA_AUX-/ USB4_2_AUX-	USB4 is not supported.	33	DDI1_PAIR2-/ USB4_1_SSTX1-	USB4 is not supported.
34	DDI2_DDC_AUX_SEL		34	DDI1_DDC_AUX_SEL	
35	USB4_2_LSTX	NA	35	USB4_2_LSRX	USB4 is not supported.
36	DDI3_CTRLCLK_AUX+	NA	36	DDI1_PAIR3+/ USB4_1_SSRX1+	USB4 is not supported.
37	DDI3_CTRLDATA_AUX-	NA	37	DDI1_PAIR3-/ USB4_1_SSRX1-	USB4 is not supported.
38	DDI2_DDC_AUX_SEL	NA	38	GND_D38	
39	DDI3_PAIR0+	NA	39	DDI2_PAIR0+/ USB4_2_SSTX0+	USB4 is not supported.
40	DDI3_PAIR0-	NA	40	DDI2_PAIR0-/ USB4_2_SSTX0-	USB4 is not supported.
41	GND (FIXED)		41	GND (FIXED)	
42	DDI3_PAIR1+	NA	42	DDI2_PAIR1+/ USB4_2_SSRX0+	USB4 is not supported.
43	DDI3_PAIR1-	NA	43	DDI2_PAIR1-/ USB4_2_SSRX0-	USB4 is not supported.
44	DDI3_HPD	NA	44	DDI2_HPD	
45	GP_SPI_CS#(NA)		45	GND_D45	
46	DDI3_PAIR2+	NA	46	DDI2_PAIR2+/ USB4_2_SSTX1+	USB4 is not supported.
47	DDI3_PAIR2-	NA	47	DDI2_PAIR2-/ USB4_2_SSTX1-	USB4 is not supported.
48	RSVD		48	GND_D48	
49	DDI3_PAIR3+	NA	49	DDI2_PAIR3+/ USB4_2_SSRX1+	USB4 is not supported.
50	DDI3_PAIR3-	NA	50	DDI2_PAIR3-/ USB4_2_SSRX1-	USB4 is not supported.
51	GND (FIXED)		51	GND (FIXED)	
52	PEG_RX0+	NA	52	PEG_TX0+	NA
53	PEG_RX0-	NA	53	PEG_TX0-	NA
54	TYPE0# (NA)	NC	54	PEG_LANE_RV#	NC
55	PEG_RX1+	NA	55	PEG_TX1+	NA

	Row C	ASL968 Difference		Row D	ASL968 Difference
56	PEG_RX1-	NA	56	PEG_TX1-	NA
57	TYPE1# (NA)	NC	57	TYPE2# (GND)	
58	PEG_RX2+	NA	58	PEG_TX2+	NA
59	PEG_RX2-	NA	59	PEG_TX2-	NA
60	GND (FIXED)		60	GND (FIXED)	
61	PEG_RX3+	NA	61	PEG_TX3+	NA
62	PEG_RX3-	NA	62	PEG_TX3-	NA
63	GND_C63		63	GND_D63	
64	GND_C64		64	GND_D64	
65	PEG_RX4+	NA	65	PEG_TX4+	NA
66	PEG_RX4-	NA	66	PEG_TX4-	NA
67	RAPID_SHUTDOWN		67	GND	
68	PEG_RX5+	NA	68	PEG_TX5+	NA
69	PEG_RX5-	NA	69	PEG_TX5-	NA
70	GND (FIXED)		70	GND (FIXED)	
71	PEG_RX6+	NA	71	PEG_TX6+	NA
72	PEG_RX6-	NA	72	PEG_TX6-	NA
73	GND		73	GND	
74	PEG_RX7+	NA	74	PEG_TX7+	NA
75	PEG_RX7-	NA	75	PEG_TX7-	NA
76	GND		76	GND	
77	GND_C77		77	GND_D77	
78	PEG_RX8+	NA	78	PEG_TX8+	NA
79	PEG_RX8-	NA	79	PEG_TX8-	NA
80	GND (FIXED)		80	GND (FIXED)	
81	PEG_RX9+	NA	81	PEG_TX9+	NA
82	PEG_RX9-	NA	82	PEG_TX9-	NA
83	GND_C83		83	GND_D83	
84	GND		84	GND	
85	PEG_RX10+	NA	85	PEG_TX10+	NA

	Row C	ASL968 Difference		Row D	ASL968 Difference
86	PEG_RX10-	NA	86	PEG_TX10-	NA
87	GND		87	GND	
88	PEG_RX11+	NA	88	PEG_TX11+	NA
89	PEG_RX11-	NA	89	PEG_TX11-	NA
90	GND (FIXED)		90	GND (FIXED)	
91	PEG_RX12+	NA	91	PEG_TX12+	NA
92	PEG_RX12-	NA	92	PEG_TX12-	NA
93	GND		93	GND	
94	PEG_RX13+	NA	94	PEG_TX13+	NA
95	PEG_RX13-	NA	95	PEG_TX13-	NA
96	GND		96	GND	
97	GND_C97		97	GND_D97	
98	PEG_RX14+	NA	98	PEG_TX14+	NA
99	PEG_RX14-	NA	99	PEG_TX14-	NA
100	GND (FIXED)		100	GND (FIXED)	
101	PEG_RX15+	NA	101	PEG_TX15+	NA
102	PEG_RX15-	NA	102	PEG_TX15-	NA
103	GND		103	GND	
104	VCC_12V	VCC_8.5V~ 20V	104	VCC_12V	VCC_8.5V~ 20V
105	VCC_12V	VCC_8.5V~ 20V	105	VCC_12V	VCC_8.5V~ 20V
106	VCC_12V	VCC_8.5V~ 20V	106	VCC_12V	VCC_8.5V~ 20V
107	VCC_12V	VCC_8.5V~ 20V	107	VCC_12V	VCC_8.5V~ 20V
108	VCC_12V	VCC_8.5V~ 20V	108	VCC_12V	VCC_8.5V~ 20V
109	VCC_12V	VCC_8.5V~ 20V	109	VCC_12V	VCC_8.5V~ 20V
110	GND (FIXED)		110	GND (FIXED)	

Note:

1. **The ASL968 supports two USB 3.2 Gen 2 ports, with an optional expansion to four ports via a USB hub. The USB_SSTX2+/-, USB_SSRX2+/-, USB_SSTX3+/-, and USB_SSRX3+/- connections are BOM-optional and can be enabled by adding a USB hub, based on project requirements.
2. **PCIE_TX6+/-, PCIE_RX6+/-(in place of SATA0) are BOM option supported by project basis.
3. **PCIE_TX7+/-, PCIE_RX7+/-(in place of 2.5GbE LAN) are BOM option supported by project basis.



▶ CPU Fan (J1)

Pin	Assignment
1	Sense
2	+12V
3	GND

▶ MIPI-CSI Connector (CN2)

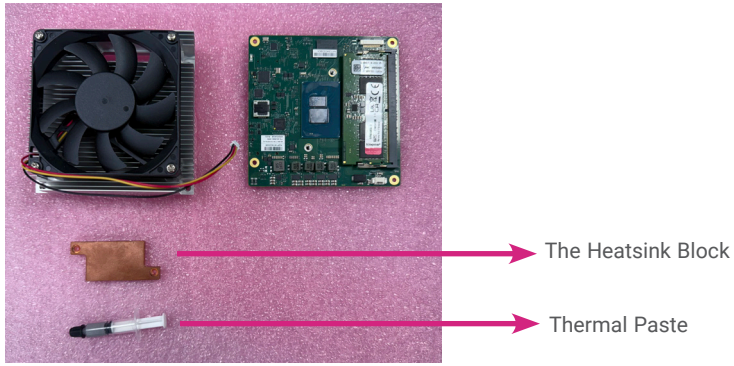
Pin	Assignment
1	CAM0_VCC
2	CAM0_VCC
3	GND
4	CSI0_RX0+
5	CSI0_RX0-
6	GND
7	CSI0_RX1+
8	CSI0_RX1-
9	GND
10	CSI0_RX2+
11	CSI0_RX2-
12	CAM0_RST#(1.8V)
13	CSI0_RX3+
14	CSI0_RX3-
15	GND
16	CSI0_CK+
17	CSI0_CK-
18	GND
19	I2C_CAM0_CK(1.8V)
20	I2C_CAM0_DAT(1.8V)
21	CAM0_PWR#(1.8V)
22	CAM0_MC(1.8V)

▶ Installing ASL968 onto a Carrier Board

Important:
The carrier board (COM335) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install ASL968 onto the carrier board of your choice.

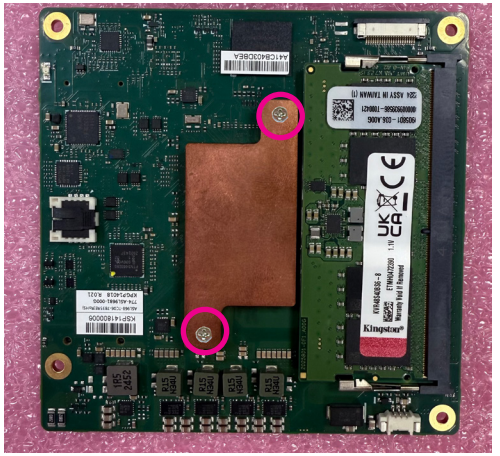
Step 1: Apply Thermal Paste to the CPU

Squeeze a small amount of thermal paste onto the CPU surface.
Apply it in a diagonal "X" pattern for even coverage.



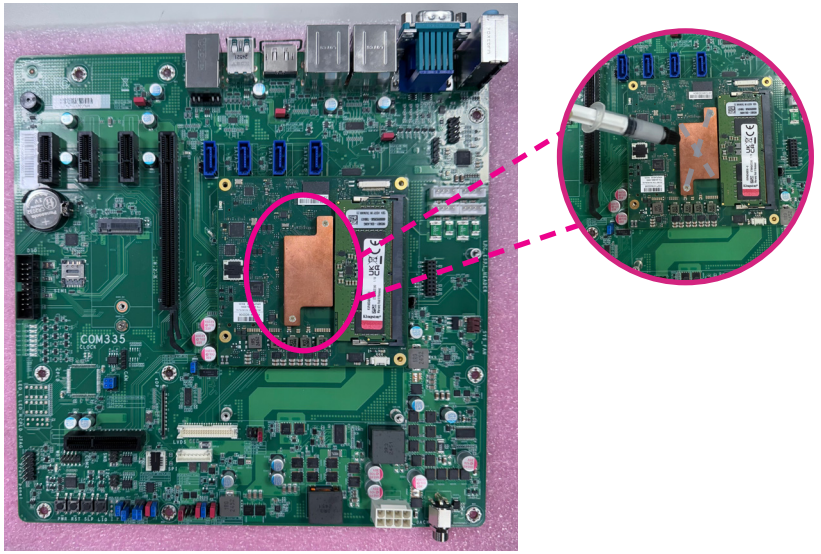
Step 2: Install the Heatsink Block

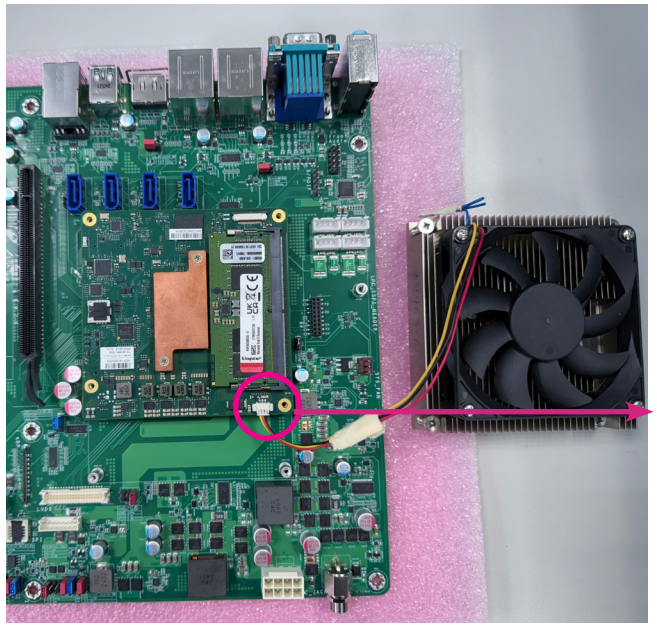
Carefully place the heatsink block on top of the CPU.
Align it properly and tighten the screws to secure it in place.



Step 3: Install ASL968 onto a Carrier Board

Mount the ASL968 onto a carrier board.
Once installed, apply thermal paste diagonally on top of the heatsink block.
Make sure the connector is properly connected to the ASL968.

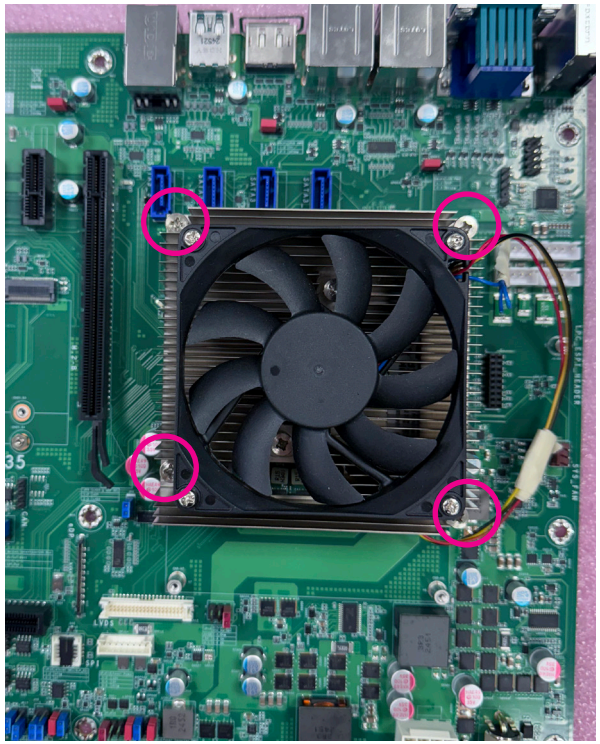




Make sure the connector is properly connected to the ASL968.

Step 4: Attach the Cooling Fan

Align the cooling fan with the heatsink block.
Place it on top and secure it with screws.
Use the provided mounting screws to install the heat sink onto the module.



Chapter 4 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message “Press DEL to run setup” will appear on the screen. If the message disappears before you respond, restart the system or press the “Reset” button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

KEYs	Function
Right and Left Arrows	Moves the highlight left or right to select a menu.
Up and Down Arrows	Moves the highlight up or down between submenus or fields.
<Esc>	Exits to the BIOS setup utility
+ (plus key)	Scrolls forward through the values or options of the hightlighted field.
- (minus key)	Scolls backward through the values or options of the hightlighted field.
<F1>	Displays general help
<F2>	Displays previous values
<F9>	Optimized defaults
<F10>	Saves and reset the setup program.
<Enter>	Press <Enter> to enter the highlighted submenu

Scroll Bar

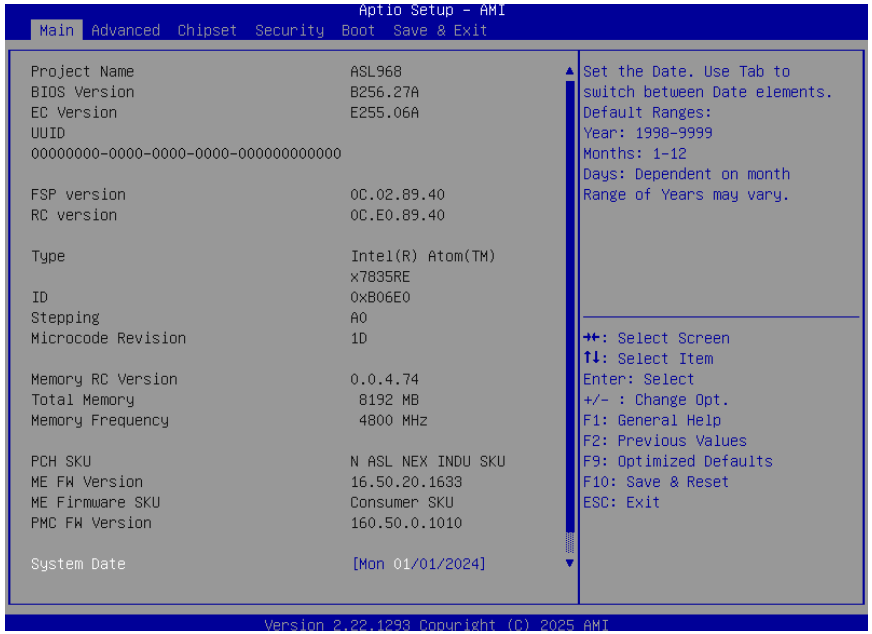
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

When “▶” appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <month>, <date>, <year>. Press "Tab" to switch to the next field and press "-" or "+" to modify the value.

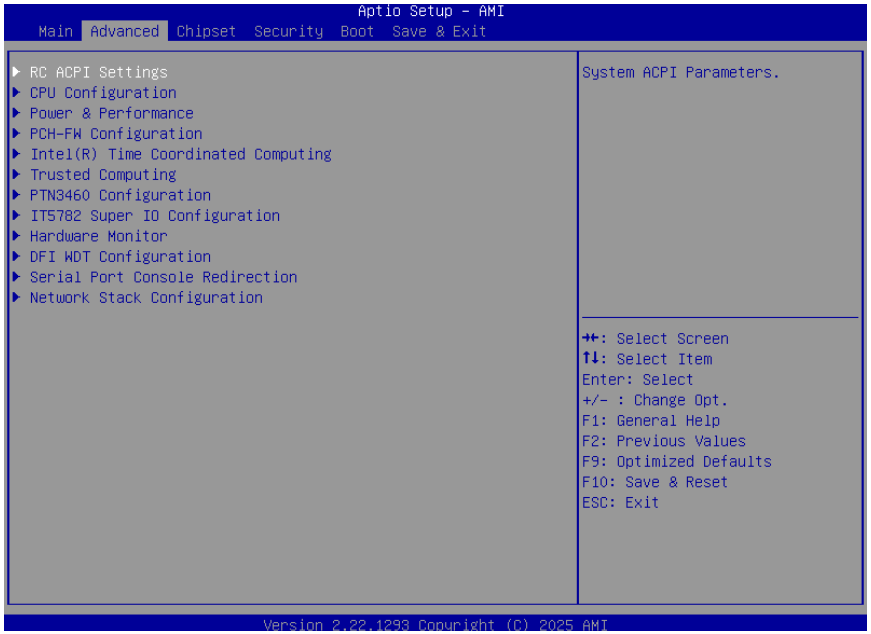
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

▶ Advanced

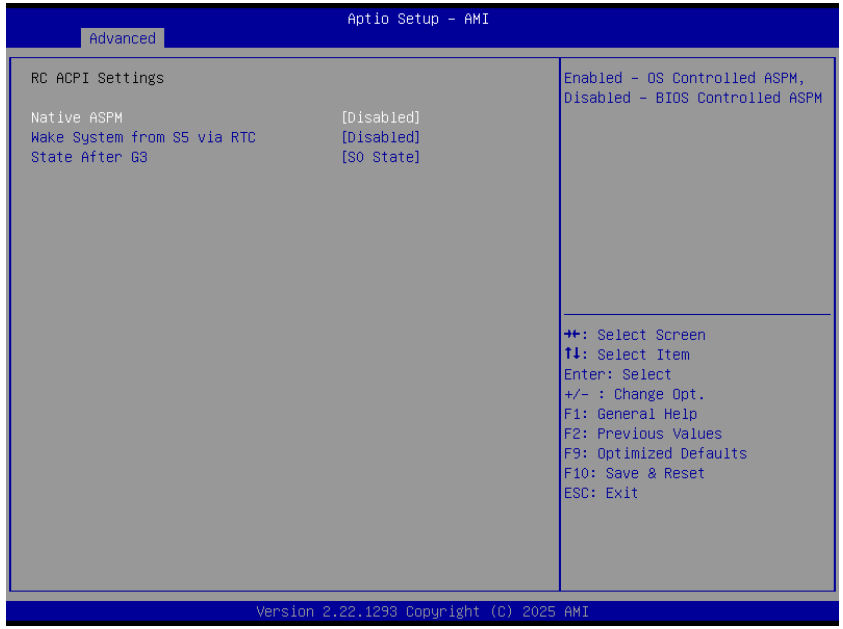
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

RC ACPI Configuration



Wake system from S5 via RTC

When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day — hour, minute, and second — for the system to wake up.

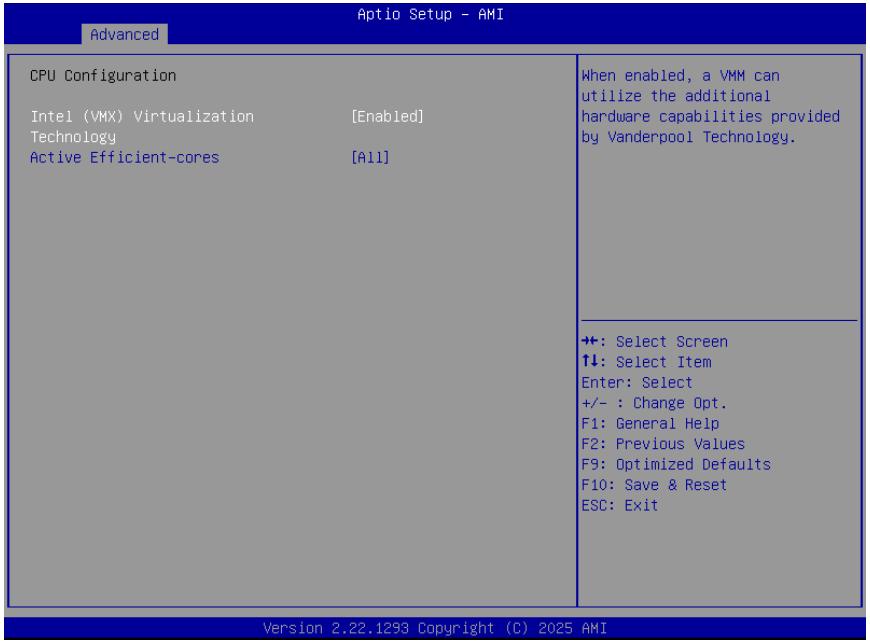
State After G3

Select between S0 State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

- **S0 State** The system automatically powers on after power failure.
- **S5 State** The system enter soft-off state after power failure. Power-on signal input is required to power up the system.

▶ Advanced

CPU Configuration



Intel (VMX) Virtualization Technology

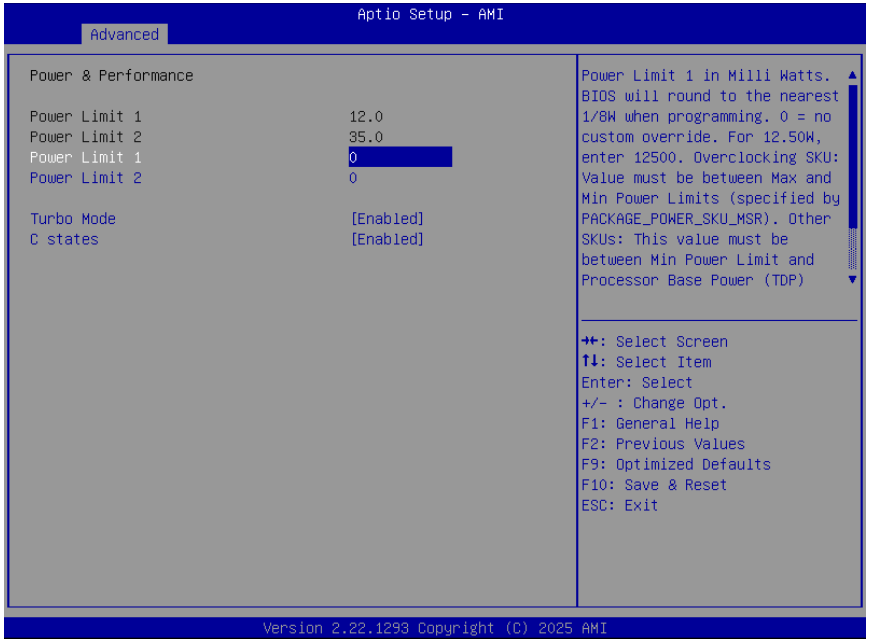
When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores

Select number of cores to enable in each processor package.

▶ Advanced

Power & Performance



Turbo Mode

Enable or disable turbo mode of the processor.
This field will only be displayed when EIST is enabled.

C states

Enable or disable CPU Power Management. It allows CPU to enter "C states" when it's idle and nothing is executing.

▶ Advanced

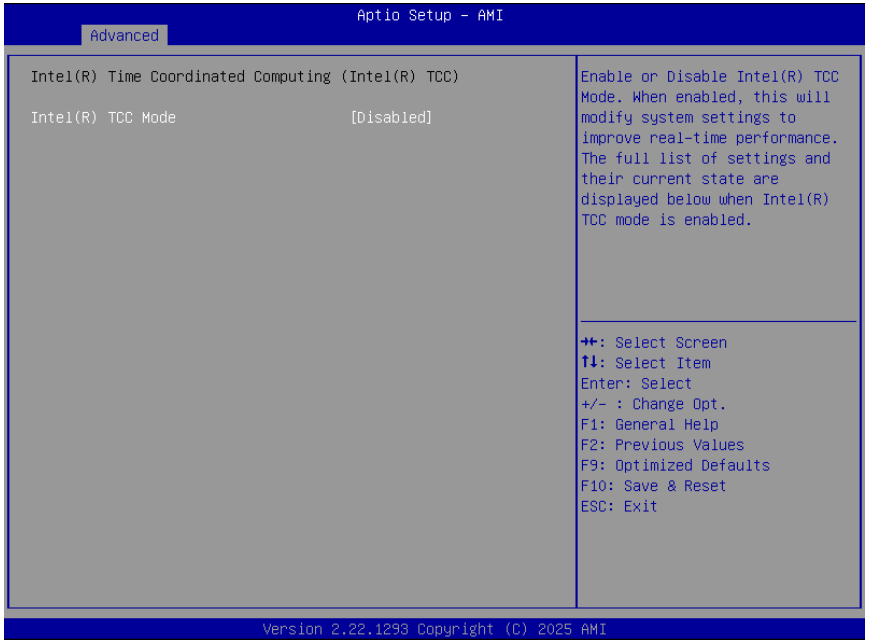
PCH-FW Configuration

ME FW Image Re-Flash

Enable / Disable Me FW Image Re-Flash function.

▶ Advanced

Intel(R) Time Coordinated Computing



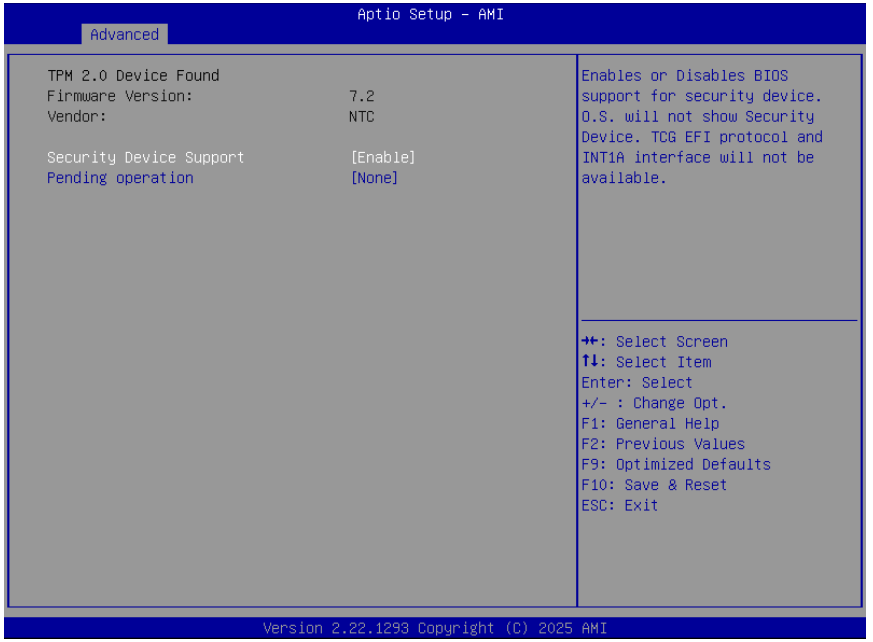
Enable or Disable Intel(R) TCC Mode. When enbaled, this will modify system settings to improve real-time performance.

Intel(R) TCC Mode

Enable or Disable Intel(R) TCC Mode. When enabled, this will modify system settings to improve real-time performance.
The full list of settings and their current state are displayed below when Intel(R) TCC mode is enabled.

▶ Advanced

Trusted Computing



Security Device Support

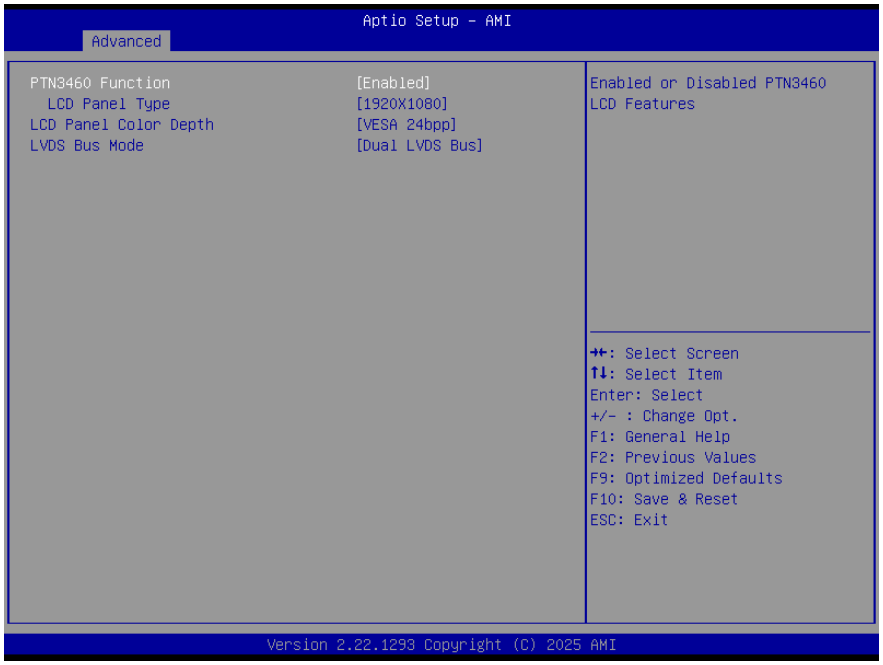
This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys.

Pending operation

To clear the existing TPM encryption, select "TPM Clear" and restart the system. This field is not available when "Security Device Support" is disabled.

▶ Advanced

PTN3460 Configuration



PTN3460 Function

Enable or Disable PTN3460 LCD Features. When this field is disabled, the following fields will remain hidden.

LCD Panel Type

Select the resolution of the LCD Panel — 800X480, 800X600, 1024X768, 1366X768, 1280X1024, 1920X1080, or 1920X1200.

LCD Panel Color Depth

Select the color depth of the LCD Panel — VESA 24bpp, JEIDA 24bpp, VESA and JEIDA 18 bpp.

LVDS Bus Mode

Select PTN3460 LVDS BUS Mode — Single LVDS Bus /Dual LVDS Bus

Note:
The configuration must match the specifications of your LCD Panel in order for the LCD Panel to display properly.

Note:
It might cause system hang-up when disable EDID emulation with PTN3460 chip on the board.

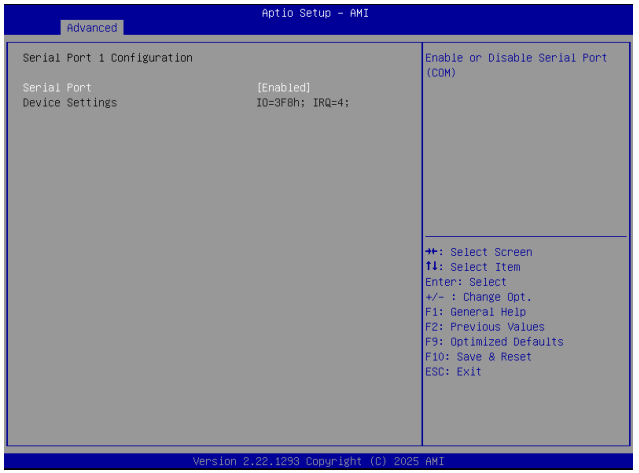
▶ Advanced

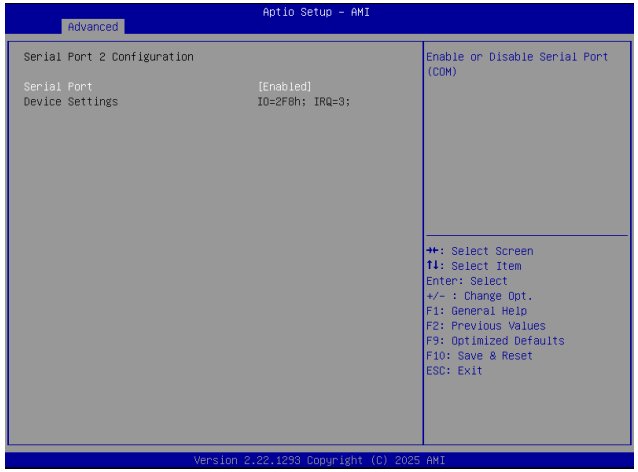
IT5782 Super IO Configuration

Serial Port Configuration
Set Parameters of Serial Ports. See next page.

▶ Advanced

IT5782 Super IO Configuration ▶ Serial Port 1, 2 Configuration

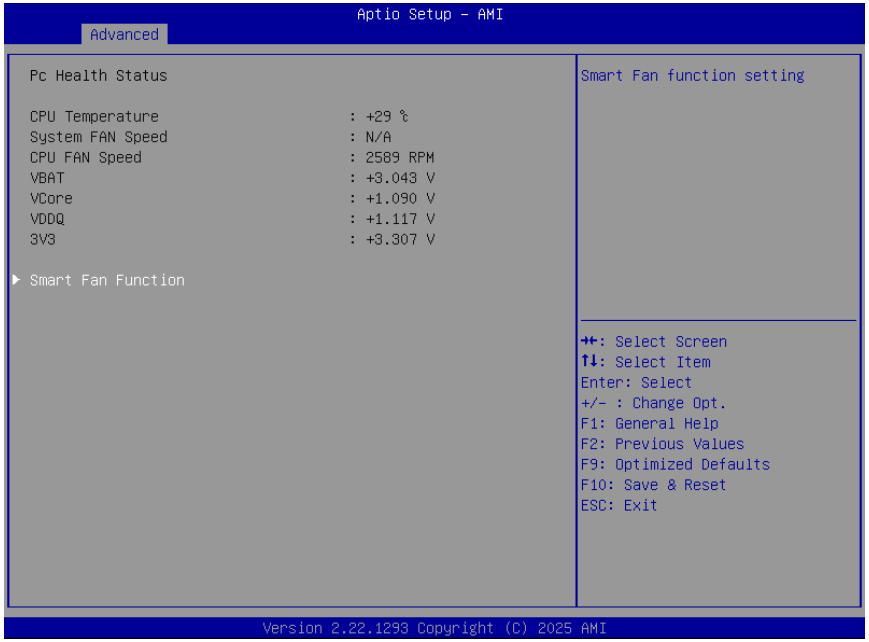




Serial Port
Enable or disable serial port.

▶ Advanced

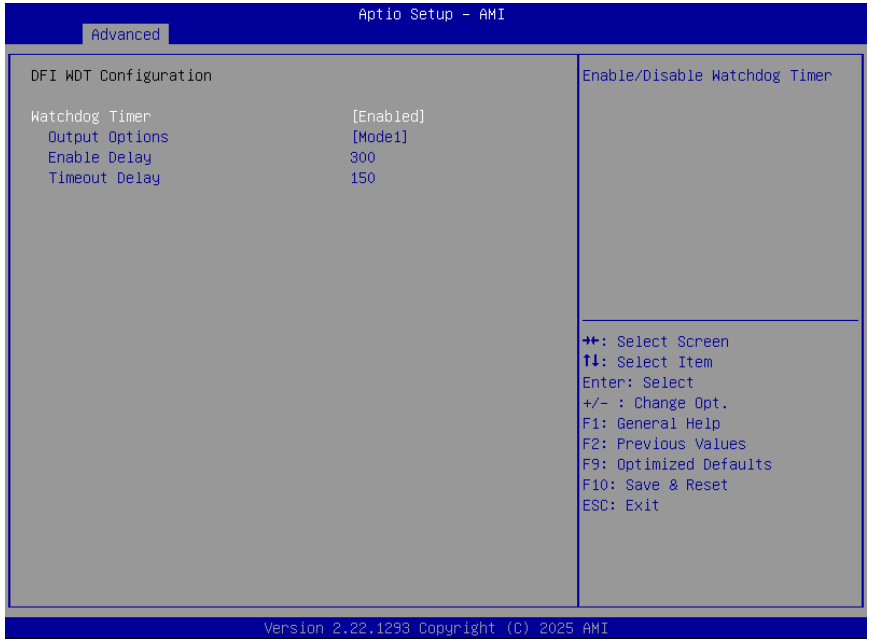
Hardware Monitor



Lists voltage, termperature, and fan speed.

▶ Advanced

DFI WDT Configuration



Watchdog Timer

Enable or disable watchdog timer.

Output Options

Mode1 = A Watchdog timeout causes the system to be reset.
Mode2 = WDT pin goes high upon timeout of the watchdog timer.
Mode3 = Generate NMI upon timeout of the watchdog timer.

Enable Delay

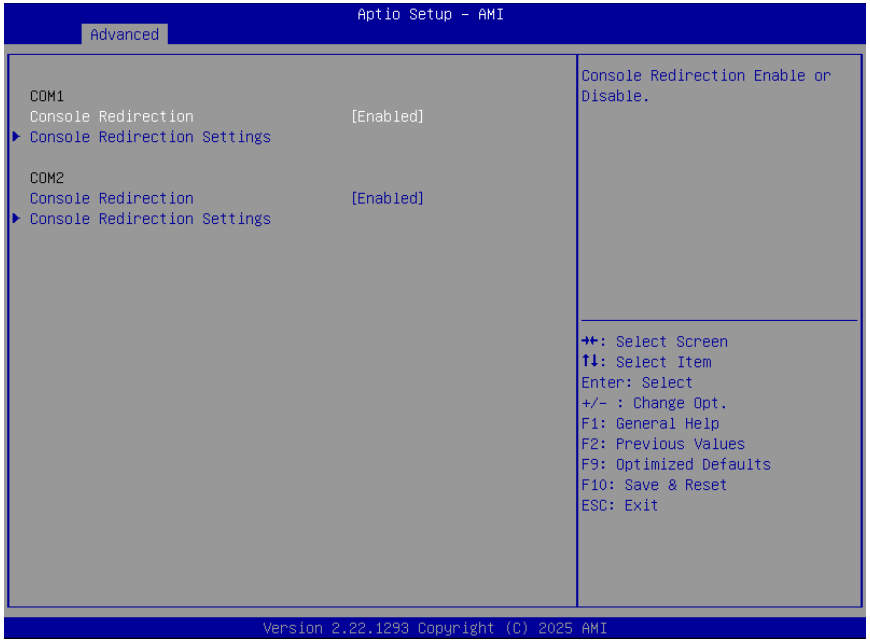
The enable delay allows time for the OS to boot and the application to load and initialize. The unit is 1 sec.

Timeout Delay

The timeout delay allows time for period of the watchdog timer. The unit is 0.1 sec.

▶ Advanced

Serial Port Console Redirection

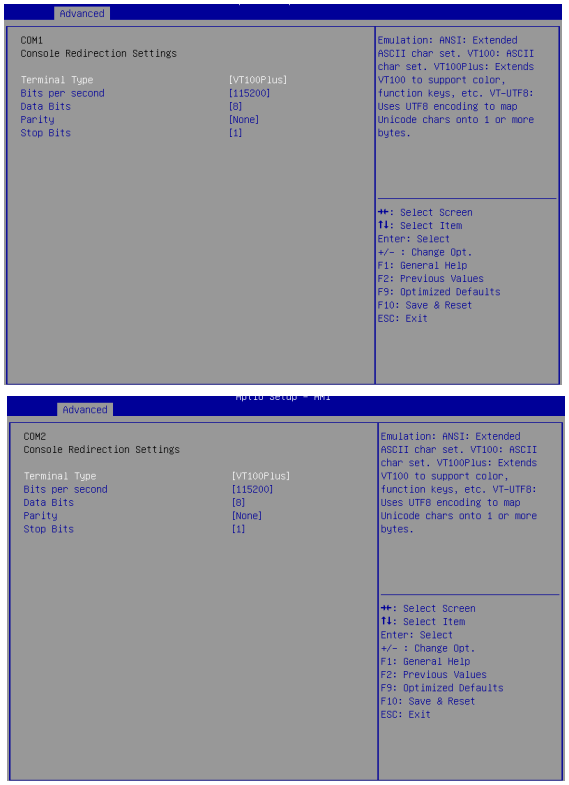


Console Redirection
Console Redirection Enable or Disable.

Console Redirection Settings
See following pages.

▶ Advanced

Serial Port Console Redirection ▶ Console Redirection Settings



Configure the serial settings of the current COM port.

Terminal Type
Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

Bits per second
Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

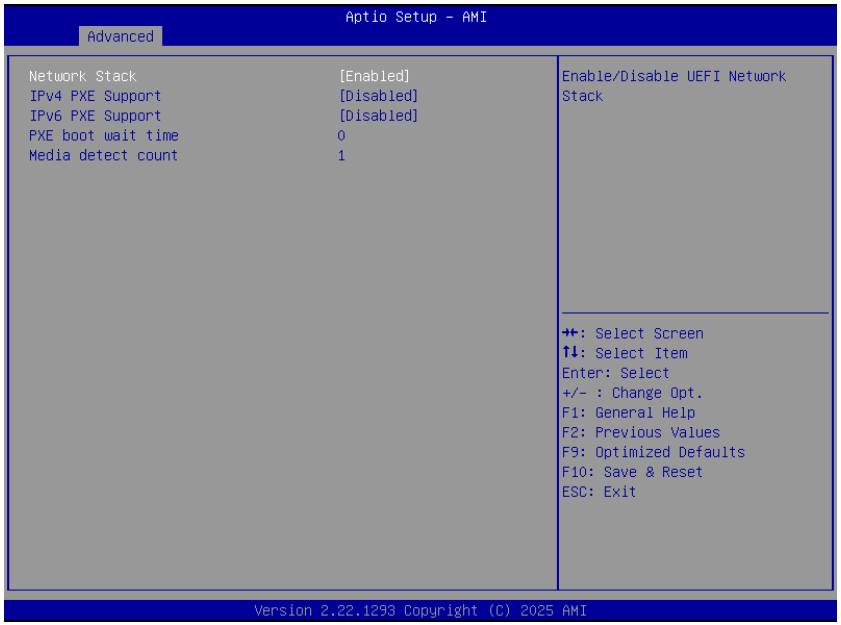
Data Bits
Select data bits: 7 bits or 8 bits.

Parity
Select parity bits: None, Even, Odd, Mark or Space.

Stop Bits
Select stop bits: 1 bit or 2 bits.

▶ Advanced

Network Stack Configuration



Network Stack

Enable or disable (Default) UEFI network stack. The following fields will appear when this field is enabled.

Ipv4 PXE Support Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

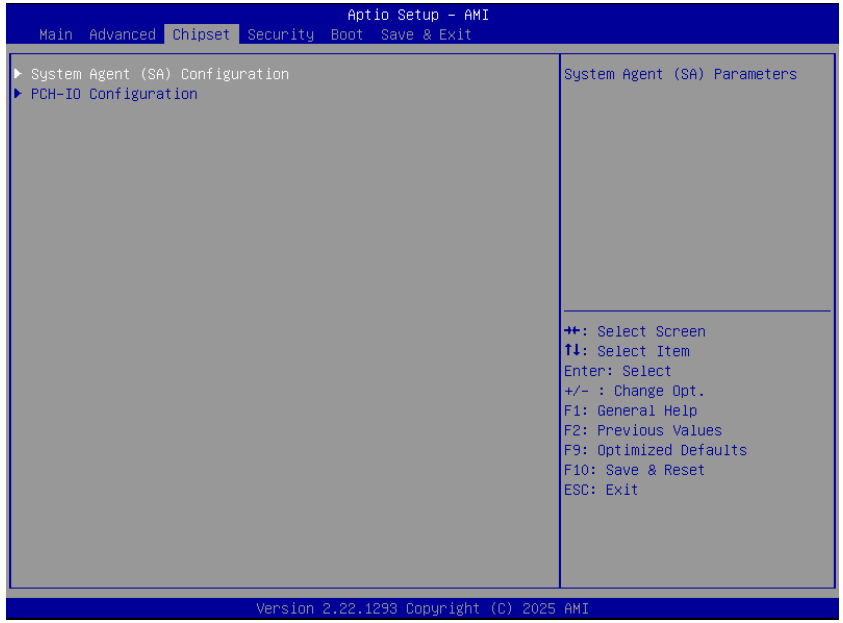
PXE boot wait time

Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

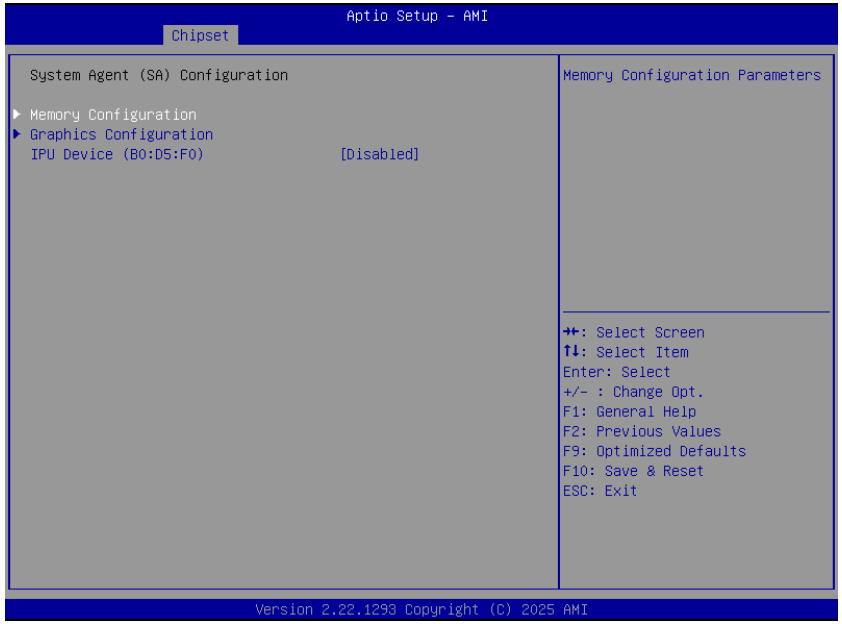
Media detect count

Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

▶ Chipset

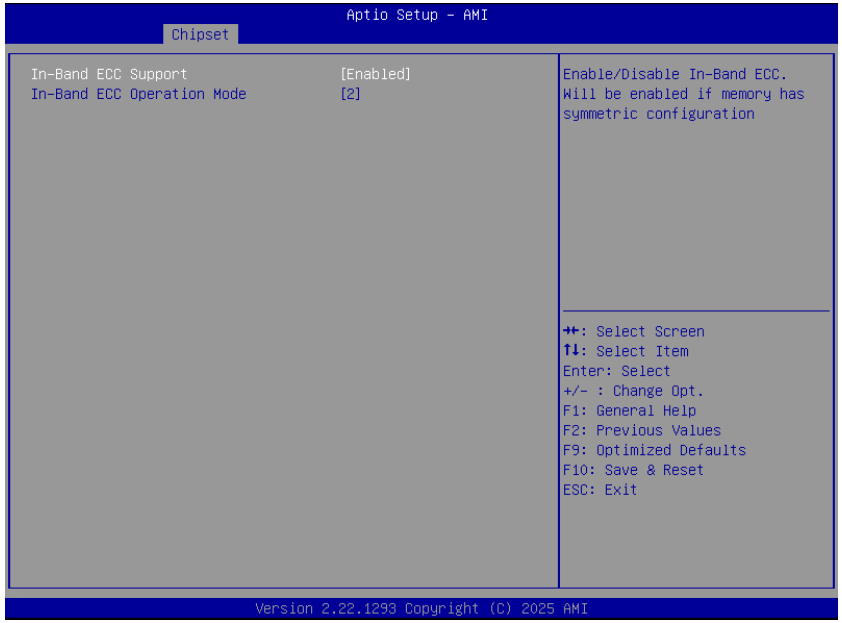


System Agent (SA) Configuration



▶ Chipset

System Agent (SA) Configuration ▶ Memory Configuration



In-Band ECC

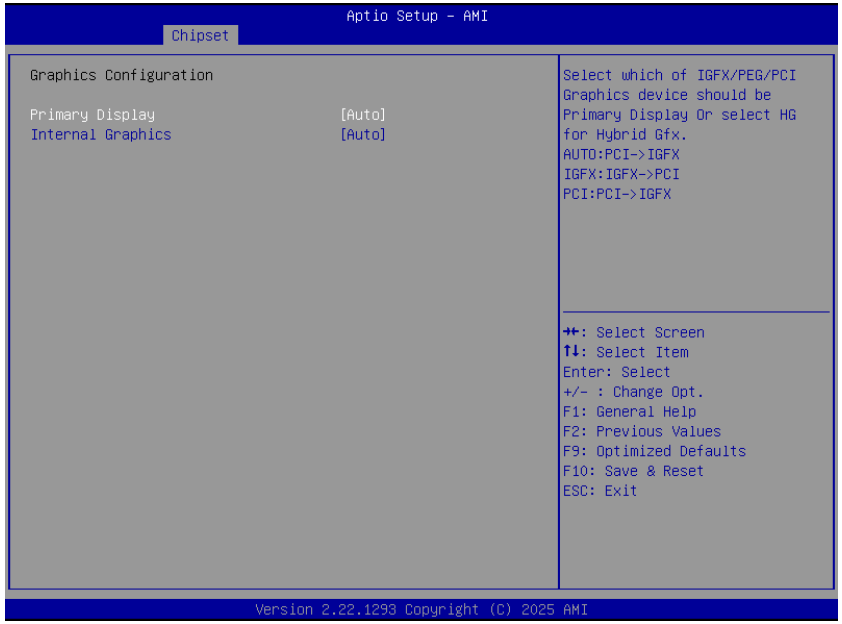
Enable/Disable (Default) In-Band ECC

In-Band ECC Operation Mode

0: Functional Mode protects requests based on the address range,
1: Makes all requests non protected and ignore range checks,
2: Makes all requests protected and ignore range checks.

▶ Chipset

System Agent (SA) Configuration ▶ Graphics Configuration



Primary Display

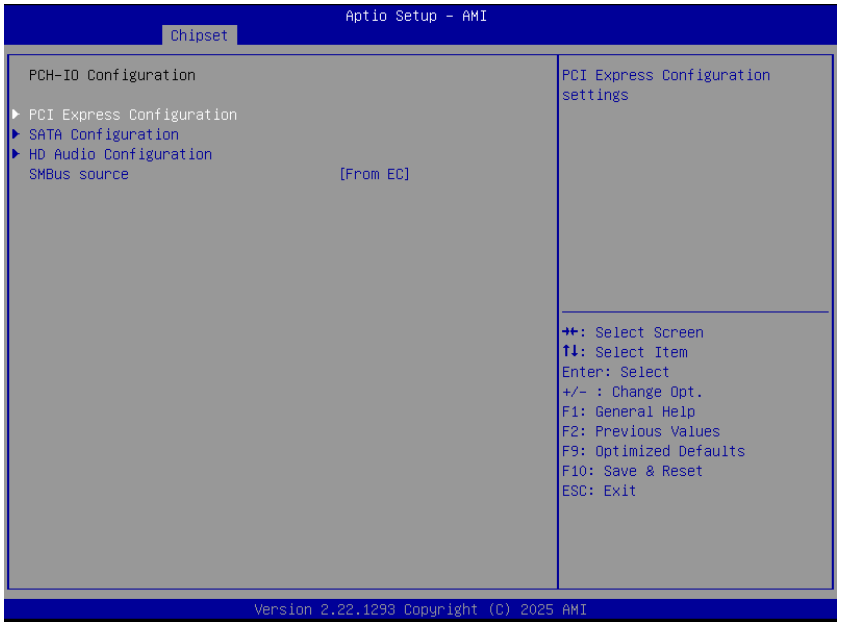
Select which of IGFX/PCI Graphics device to be the primary display.

Internal Graphics

Keep IGFX "Enabled" or "Disabled" based on the setup options, or select "Auto" for auto-detection.

▶ Chipset

PCH-IO Configuration



Select one of the PCI Express channels and press enter to configure the following settings.

PCI Express Configuration

PCI Express Configuration Settings

SATA And RST Configuration

SATA Device Otpions Settings

HD Audio Configuration

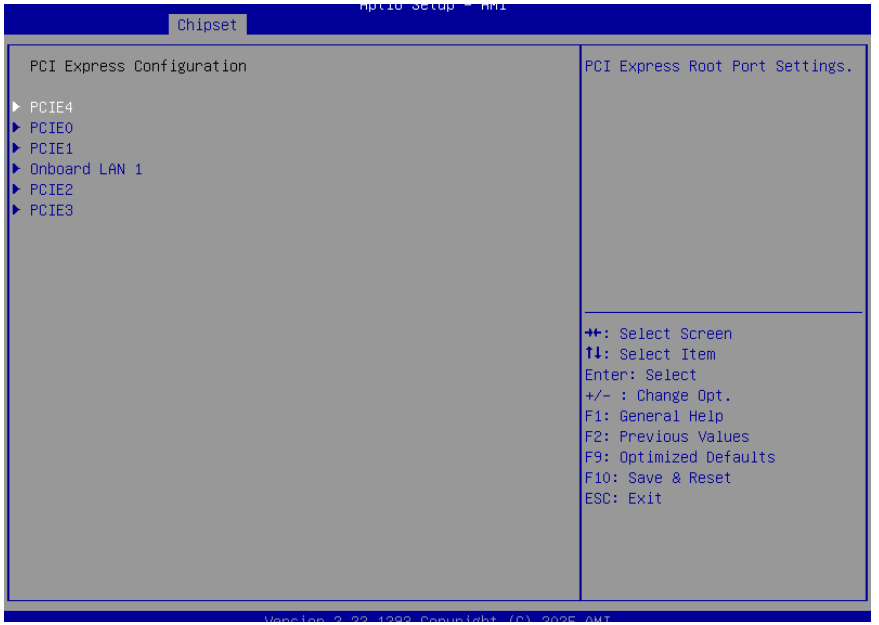
HD Audio Subsystem Configuration Settings

SMBus Source

Choose where SMBus comes from.

▶ Chipset

PCH-IO Configuration ▶ PCI Express Configuration



Select one of the PCI Express channels and press enter to configure the following settings.

PCIe Express Root Port 0,1,2,3,4

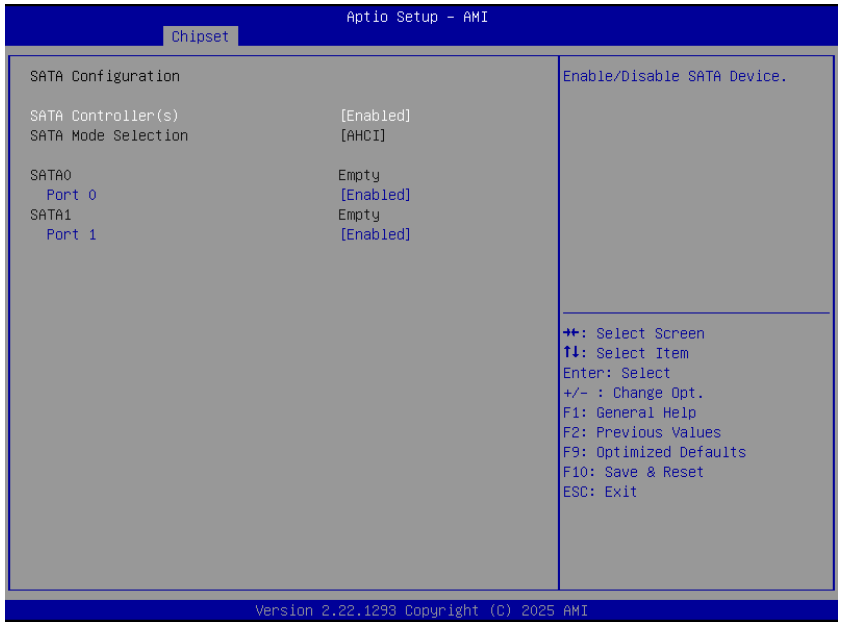
Control the PCI Express Root Port.

Onboard LAN1

Control the PCI Express Root Port.

▶ Chipset

PCH-IO Configuration ▶ SATA Configuration



SATA Controller(s)

This field is used to enable or disable the Serial ATA controller.

SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.

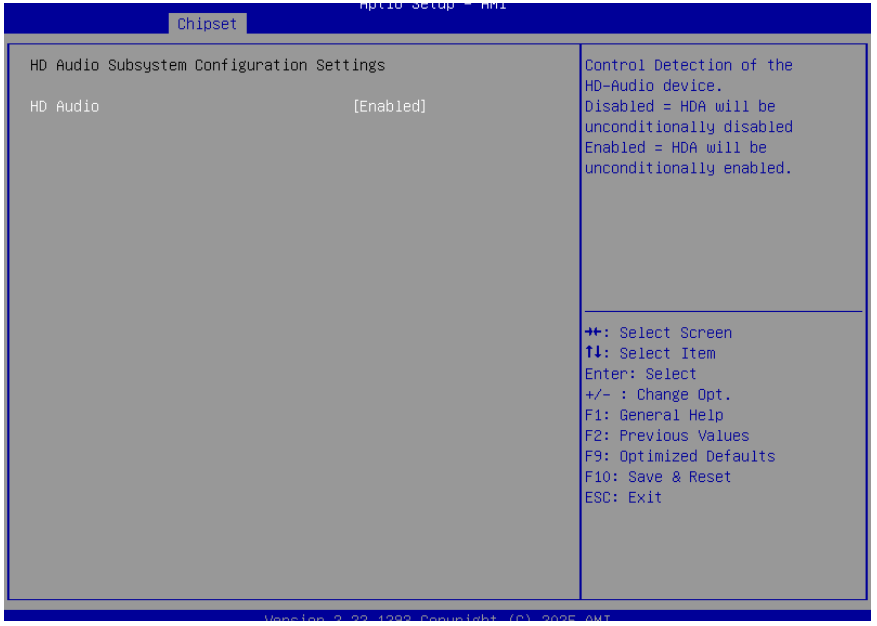
- **AHCI** This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

Ports

Enable or disable the Serial ATA ports.

▶ Chipset

PCH-IO Configuration ▶ HD Audio Configuration

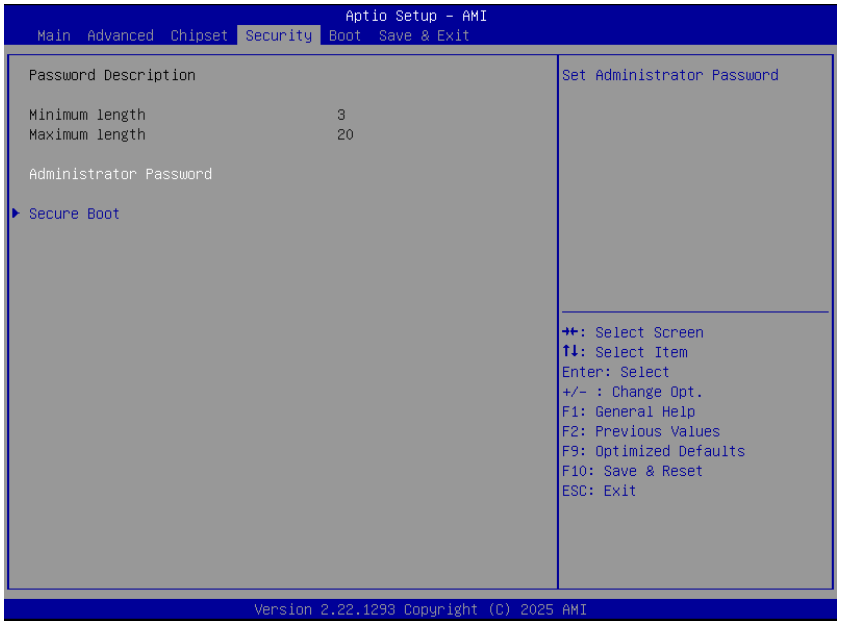


HD Audio

Control the detection of the HD Audio device.

- **Disabled** HDA will be unconditionally disabled.
- **Enabled** HDA will be unconditionally enabled.

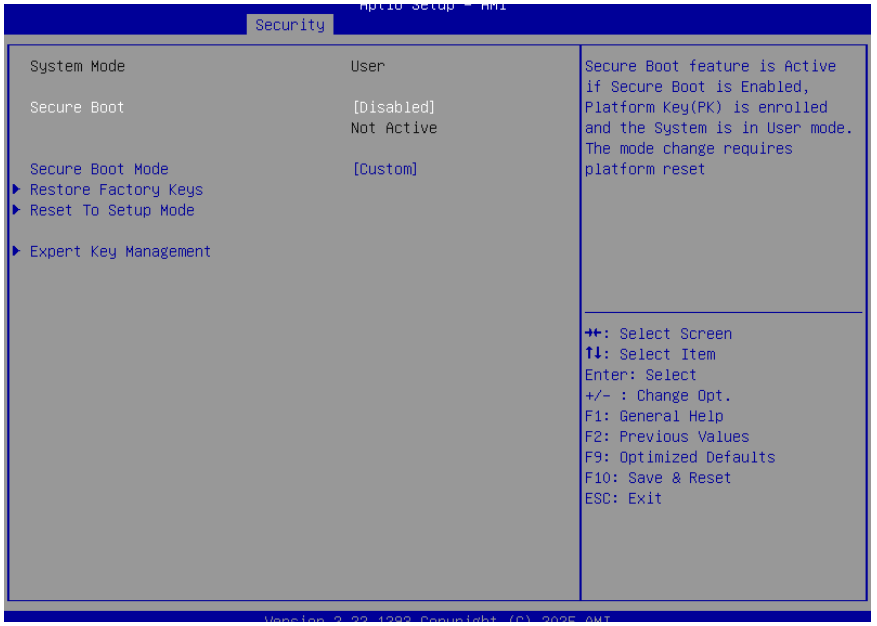
▶ Security



Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

Secure Boot



Secure Boot

Secure Boot feature is Active if secure Boot is Enabled, Platform Key (PK) is enrolled and the system is in user mode. The mode change requires platform reset.

Secure Boot Mode

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

Restore Factory Keys

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

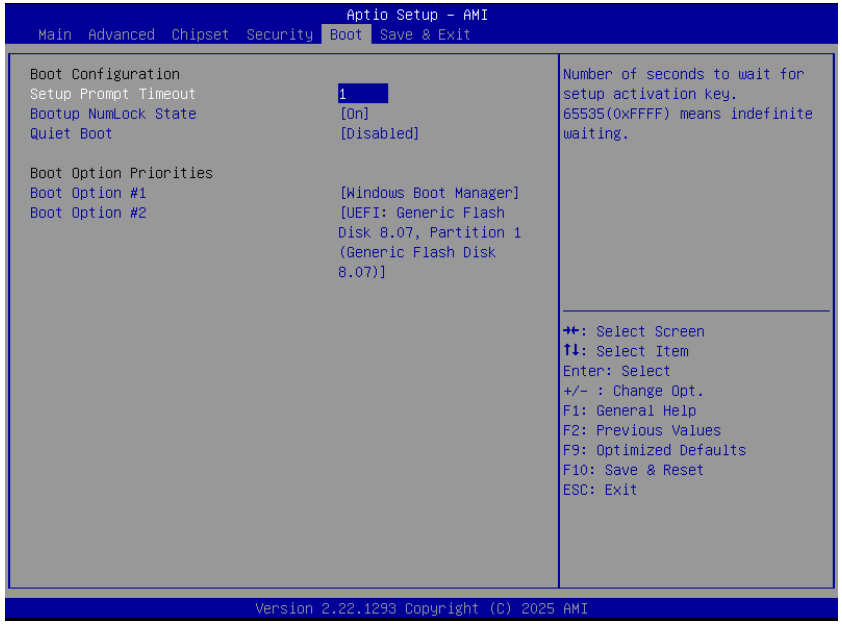
Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

Key Management

Enables expert users to modify Secure Boot Policy variables without full authentication.

▶ Boot



Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state: On or Off.

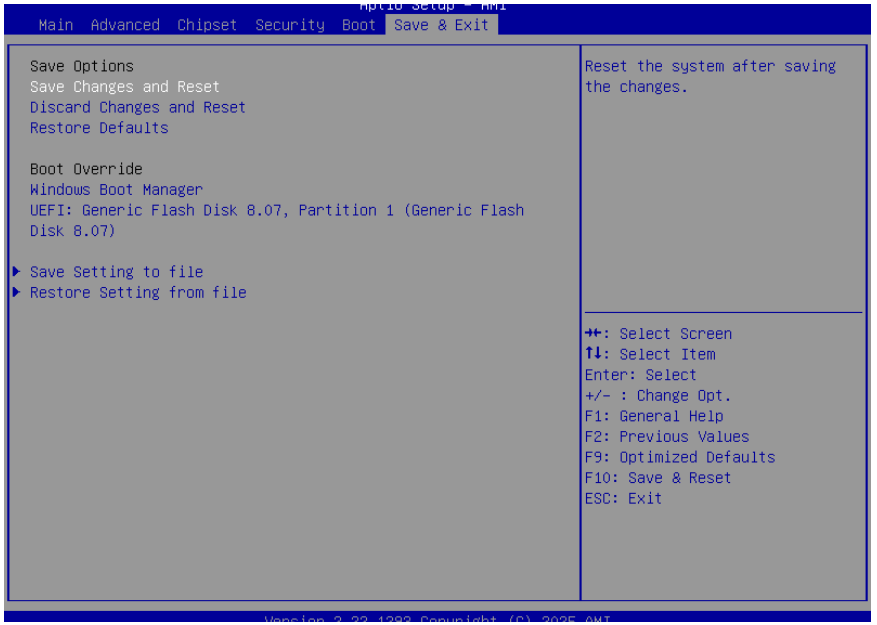
Quiet Boot

This section is used to enable or disable quiet boot option.

Boot Option Priorities

Rearrange the system boot order of available boot devices.

▶ Save & Exit



Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

Boot Override

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The “Boot Option Priorities” configured in the Boot menu will not be changed.

► Save Setting to file

Select this option to save BIOS configuration settings to a USB flash device.

► Restore Setting from file

This field will appear only when a USB flash device is detected. Select this field to restore setting from the USB flash device.

▶ Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

▶ Notice: BIOS SPI ROM

- 1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

Note:

a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.

b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

c. After updating unique MAC Address from manufacturing, NVM will be protected immediately after power cycle.
Users cannot update NVM or MAC address.