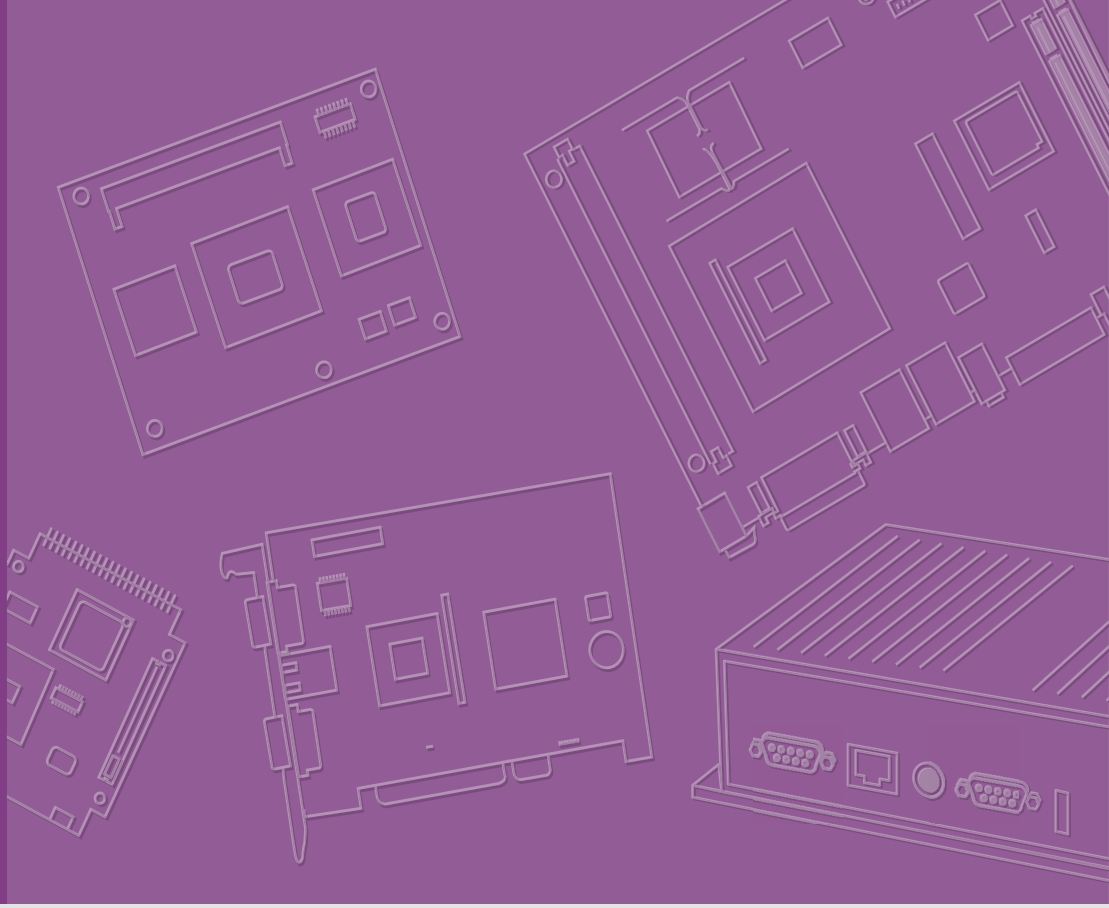

User Manual

SOM-E781

AMD EPYC™ 8004 Processor
COM-HPC® Server Size E
Module with Proprietary Pinout

ADVANTECH

Enabling an Intelligent Planet

Copyright

Acknowledgments

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Product Warranty (2 Years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Part No. 2006E78100 Edition 1

Printed in Taiwan March 2025

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Test conditions for passing also include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

FM

This equipment has passed FM certification. According to the National Fire Protection Association, work sites are categorized into different classes, divisions, and groups based on hazard considerations. This equipment is compliant with the specifications for Class I, Division 2, Groups A, B, C, and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions, and Notes

Warning! *Warnings indicate conditions that could cause personal injury if not observed!*

Caution! *Cautions are included to help prevent hardware damage and data loss. For example,*

"Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions."

Note! *Notes provide additional and/or optional information.*

Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all feedback in writing to support@advantech.com.

Packing List

Before system installation, check that the items listed below are included and in good condition. If any item does not accord with the list, contact your dealer immediately.

- SOM-E781 CPU module

Part No	CPU	Cores	Base Freq.	Max Turbo Freq.	CPU TDP	CPU Threads	DDR5 RDIMM	PCIe lanes	Thermal solution	Operating Temp.
SOM-E781S64-U3A1	EYPC™ 8534P	64	2.3GHz	3.1GHz	200W	128	4800MT/s	79(Gen5*72 &Gen3*7)	Active * Optional Accessories	0 ~ 50°C
SOM-E781S16-U4A1	EYPC™ 8124P	16	2.45GHz	3.0GHz	125W	32	4800MT/s	79(Gen5*72 &Gen3*7)	Active * Optional Accessories	0 ~ 50°C

* Other combinations are based on the specific project. Please contact sales for details.

The thermal solution is not included in the standard package. Please remember to place an order for a thermal solution.

Development Board

Part No.	Description
SOM-DH7000-00A2	COM-HPC Size E proprietary Dev. Board A2

Optional Accessories

Part No.	Description
1970005652T001	One piece heatsink, 225W 119.3x78.9x22.6mm
1970006083N000	C.L R3 200x160x76.16mm SC SOM-E781

Safety Precautions - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
- Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped and damaged.
    - The equipment shows obvious signs of breakage.
15. Do not leave the equipment in an environment with a storage temperature of below -20°C (-4°F) or above 60°C (140°F) as this may damage the components. The equipment should be kept in a controlled environment.
16. CAUTION: Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
17. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position should not exceed 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Term	Definition
AC'97	Audio CODEC (Coder-Decoder)
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PC-AT systems
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system
CAN	Controller-area network (CAN or CAN bus) is a vehicle bus standard designed to allow micro-controllers to communicate with each other within a vehicle without a host computer
DDI	Digital Display Interface – containing DisplayPort, HDMI/DVI, and SDVO
EAPI	Embedded Application Programmable Interface Software interface for COM Express® specific industrial function ■ System information ■ Watchdog timer ■ I2C Bus ■ Flat Panel brightness control ■ User storage area ■ GPIO
GbE	Gigabit Ethernet
GPIO	General purpose input output
HDA	Intel High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high-definition audio that is capable of playing back more channels at higher quality than AC'97.
I2C	Inter Integrated Circuit – 2-wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values
ME	Management Engine
PC-AT	"Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel-based personal computers in the 1990s
PEG	PCI Express Graphics
RTC	Real Time Clock – battery-backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information
TPM	Trusted Platform Module, chip to enhance the security features of a computer system
UEFI	Unified Extensible Firmware Interface
WDT	Watchdog Timer

Contents

Chapter 1

General Information

This chapter gives background information on the SOM-E781 CPU Computer on Module.

Sections include:

- Introduction
- Functional Block Diagram
- Product Specifications

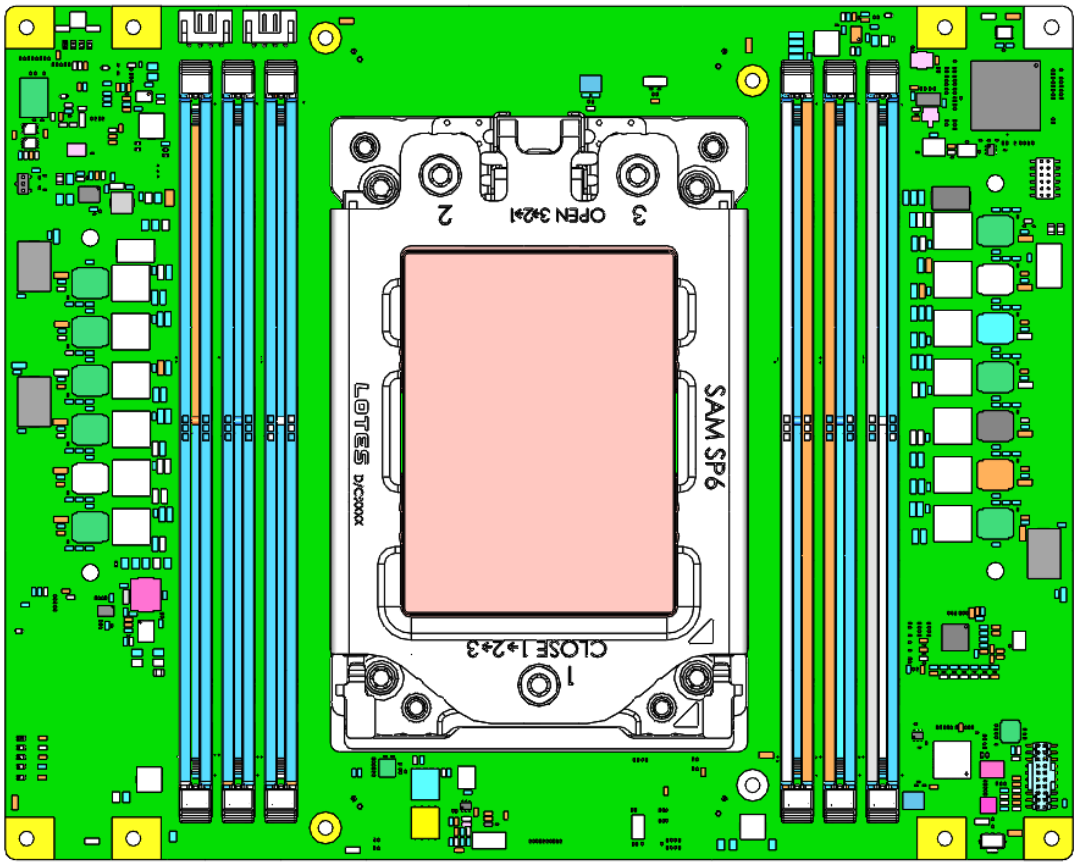
1.1 Introduction

The Advantech SOM-E781 is a COM-HPC CPU Module featuring an AMD EPYC 8004 server-grade CPU. Designed as a COM-HPC Server Size E module with proprietary pinout, it supports up to 576GB of DDR5 memory and provides up to 72 PCIe Gen5 lanes and 7 PCIe Gen3 lanes.

This product supports 1 x Intel i226, 2 x SATA 3.0, 4 x USB 3.2 Gen1, 4 x USB 2.0, 2 x COM ports (4-wire), and TPM 2.0. The SOM-E781 supports an operating temperature range of 0 ~ 60°C (with a QFCS and fan).

Advantech iManager (SUSI 4) satisfies diverse requirements by supporting multi-level watchdog timers, voltage & temperature monitoring, thermal protection & mitigation, LCD backlight on/off & brightness control, and embedded storage. All Advantech COM-HPC modules integrate iManager and WISE-PaaS/RMM.

1.2 Functional Block Diagram



1.3 Product Specifications

1.3.1 Compliance

- PICMG COM-HPC Revision 1.10 (proprietary pinout)
- Size E 200 x 160 mm
- Pin-out Server Type compatible (proprietary pinout)

1.3.2 Feature List

Table 1.1: Feature List

Feature Type	Connector	Feature	COM HPC Definition		SOM-E781
			Max.	Min.	
Display	J1	eDP	0	0	0
	J1	DDI0	0	0	0
	J1	DDI1	0	0	0
	J2	DDI2	0	0	0
Expansion	J1	PCI Express	25	0	25
	J2	PCI Express	54	0	54
Serial	J1	SMBus	1	0	1
	J1	I2C Bus	2	0	2
	J1	IPMB	1	0	0
	J1	UART	2	0	2
I/O	J1-J2	NBASE-T (max. 10G)	1	0	1
	J2	ETH KR (max 25G)	0	0	0
	J2	ETH KR CEI	0	0	0
	J1	USB 2.0	8	0	4
	J1-J2	USB 3.2 Gen 1	4	0	4
	J1	USB C PD I2C	1	0	0
	J1	Soundwire/DMIC	0	0	0
	J1	I2S/2xSNDW	0	0	0
	J1	HD Audio	0	0	0
	J1	SATA	2	0	1
	J1	ESPI	1	0	1
	J1	BOOT_SPI	1	0	1
	J1	GP_SPI	1	0	0
	J1	GPIO	12	0	12
	J1	MISC	1	0	0
	J1	Functional Safety	1	0	0
	J1	Fan PWM/Tachometer	2	0	2
	J1	Trusted Platform Modules	1	0	1
PowerI	J1-J2	Power	50	0	50
	J1-J2	Standby Power	4	0	4
	J1-J2	GND	227	0	227
	J1	RSVD	10	0	10

1.3.3 Processor System

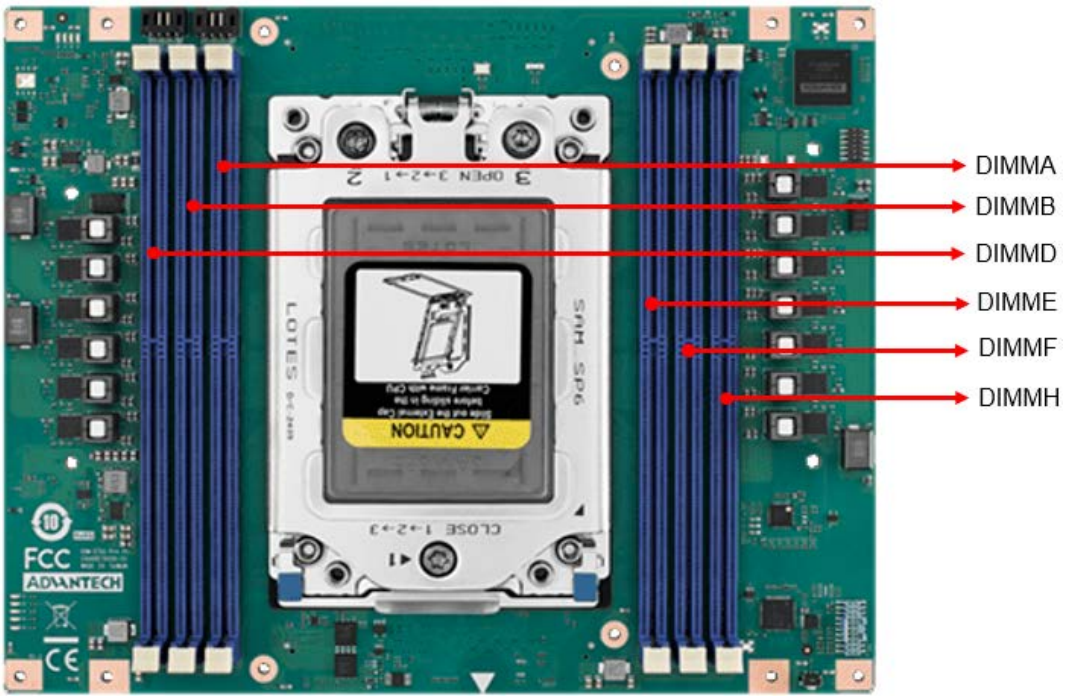
Table 1.2: Processor System					
CPU	**Cores**	**Cores Clock**	**Max Turbo Freq.**	**Cache (MB)**	**TDP (W)**
EYPC™ 8534P	64	2.3GHz	3.1GHz	128	200W
EYPC™ 8124P	16	2.45GHz	3.0GHz	64	125W

1.3.4 Memory

There are a total of 6 memory sockets on SOM-E781. These support 96GB max capacity with 287-pin RDIMM sockets.

6 x RDIMM, 1 x DPC, 4800 MT/s, max DIMM capacity 96GB, up to 576GB.

Table 1.3: Quantity of Memory Installed				
	1	2	4	6
DIMMA	V	V	V	V
DIMMB				V
DIMMD			V	V
DIMME		V	V	V
DIMMF				V
DIMMH			V	V



1.3.5 Expansion Interfaces

1.3.5.1 PCIe Gen5 x16

PCI Express x16: Supports 2 groups by default for 4 x PCIe x16, compliant with PCIe Gen5 (32.0 GT/s) specifications, configurable to PCIe x16, x8, x4. Several configurable combinations may need BIOS modification. Please contact Advantech sales or FAE for more details.

1.3.5.2 PCIe Gen5 x8 (Proprietary*1)

PCI Express x8: Supports 1 x PCIe x8 by default, compliant with PCIe Gen5 (32.0 GT/s) specifications, configurable to PCIe x8 or PCIe x4. Several configurable combinations may need BIOS modification. Please contact Advantech sales or FAE for more details.

1.3.5.3 PCIe Gen3 x4 (Proprietary*1)

PCI Express x4: Supports 1 x PCIe x4 by default, compliant with PCIe Gen3 (8.0 GT/s) specifications, configurable only to PCIe x4.

1.3.5.4 PCIe Gen3 x1 (Proprietary *2, BMC *1)

PCI Express x1: Supports 1 x PCIe x1 by default, compliant with PCIe Gen3 (8.0 GT/s) specifications.

Table 1.4:

Group	PCIe Lane	Source	Port	Default
Group 0 Low (J1)	PCIe0	PCIE G2 group	#0	PCIe x16_Slot1
	PCIe1		#1	
	PCIe2		#2	
	PCIe3		#3	
	PCIe4		#4	
	PCIe5		#5	
	PCIe6		#6	
	PCIe7		#7	
Group 0 High (J1)	PCIe8		#8	
	PCIe9		#9	
	PCIe10		#10	
	PCIe11		#11	
	PCIe12		#12	
	PCIe13		#13	
	PCIe14		#14	
	PCIe15		#15	

Table 1.5:				
Group	**PCIe Lane**	**Source**	**Port**	**Default**
Group 1 (J2)	PCIe16	PCIE P2 group	#0	PCIe x16_Slot3
	PCIe17		#1	
	PCIe18		#2	
	PCIe19		#3	
	PCIe20		#4	
	PCIe21		#5	
	PCIe22		#6	
	PCIe23		#7	
	PCIe24		#8	
	PCIe25		#9	
	PCIe26		#10	
	PCIe27		#11	
	PCIe28		#12	
	PCIe29		#13	
	PCIe30		#14	
	PCIe31		#15	

Table 1.6:				
Group	**PCIe Lane**	**Source**	**Port**	**Default**
Group 2 (J2)	PCIe32	PCIE P0 group	#0	PCIe x16_Slot2
	PCIe33		#1	
	PCIe34		#2	
	PCIe35		#3	
	PCIe36		#4	
	PCIe37		#5	
	PCIe38		#6	
	PCIe39		#7	
	PCIe40		#8	
	PCIe41		#9	
	PCIe42		#10	
	PCIe43		#11	
	PCIe44		#12	
	PCIe45		#13	
	PCIe46		#14	
	PCIe47		#15	

Table 1.7:				
Group	**PCIe Lane**	**Source**	**Port**	**Default**

Table 1.7:				
Group 3 (J2)	PCIe48	PCIE P3 group	#0	PCIe x16_Slot4
	PCIe49		#1	
	PCIe50		#2	
	PCIe51		#3	
	PCIe52		#4	
	PCIe53		#5	
	PCIe54		#6	
	PCIe55		#7	
	PCIe56		#8	
	PCIe57		#9	
	PCIe58		#10	
	PCIe59		#11	
	PCIe60		#12	
	PCIe61		#13	
	PCIe62		#14	
	PCIe63		#15	

Table 1.8:				
Group	**PCIe Lane**	**Source**	**Port**	**Default**
Group ADD (J1)	PCIeA0	PCIE G0 group	#0	PCIe x8_Slot1
	PCIeA1		#1	
	PCIeA2		#2	
	PCIeA3		#3	
	PCIeA4		#4	
	PCIeA5		#5	
	PCIeA6		#6	
	PCIeA7		#7	

Table 1.9:				
Group	**PCIe Lane**	**Source**	**Port**	**Default**
Group ADD (J2)	PCIeA8	PCIE P4 group	#0	PCIe x4_Slot1
	PCIeA9		#1	
	PCIeA10		#2	
	PCIeA11		#3	
	~~PCIeA12~~	PCIE G0 group	#0	~~PCIe x4_Slot2~~
	~~PCIeA13~~		#1	
	~~PCIeA14~~		#0	~~PCIe x4_Slot3~~
	~~PCIeA15~~		#1	

1.3.6 Serial Bus

1.3.6.1 SMBus

Supports the SMBus 2.0 specification.

1.3.6.2 I²C Bus

Supports I2C bus 7-bit address modes. Supports standard mode up to 100 Kb/s, fast mode up to 400 Kb/s.

1.3.7 I/O

1.3.7.1 Gigabit Ethernet

- **Ethernet:** Intel I226 Gigabit LAN supports 10/100/1000 Mbps & 2.5 Gbps Speed.

1.3.7.2 SATA

Supports 2 x SATA Gen3 (6.0 Gb/s), backward-compliant to SATA Gen2 (3.0 Gb/ s) and Gen1 (1.5 Gb/s). The maximum data rate is 600 MB/s. It supports AHCI 1.3.1 mode (does not support IDE mode).

1.3.7.3 USB 3.2 / USB 2.0

COM-HPC supports USB 3.2 but the SOM-E781 supports 4 x USB 3.2 Gen1 (5 Gbps)

ports and 4 x USB 2.0 (480 Mbps) ports.

Notice: Advantech strongly recommends using a certified cable to maximize USB 3.2 Gen1 performance.

1.3.7.4 USB 3.2 Gen1

Table 1.10: USB 3.2 Gen1

Server Type	P00	P01	P02	P03
SoC	P0	P1	P2	P3
Server Type	OC_01		OC_23	
SoC USB_OC#	OC_01		OC_23	

1.3.7.5 USB 2.0

Table 1.11: USB 2.0

Server Type	P00	P01	P02	P03
SoC	P0	P1	P2	P3
Server Type	OC_01		OC_23	
SoC USB_OC#	OC_01		OC_23	

1.3.7.6 SPI Bus

It supports BIOS flash only. The SPI clock can be 50MHz, with a capacity up to 256Mb, 1.8V.

1.3.7.7 GPIO

12 programmable general purpose input or output (GPIO).

1.3.7.8 Watchdog

Supports multi-level watchdog time-out output. Provides 1-65535 levels, from 100ms to 109.22 minute intervals.

1.3.7.9 Serial port

2 x 2-wire serial port (Tx/Rx) supports 16550 UART compliance.

- Programmable FIFO or character mode
- 16-byte FIFO buffer on transmitter and receiver in FIFO mode
- Programmable serial-interface characteristics: 5-, 6-, 7-, or 8-bit character
- Even, odd, or no parity bit selectable
- 1, 1.5, or 2 stop bits selectable
- Baud rate up to 115.2K

1.3.7.10 TPM

Supports TPM 2.0 module.

1.3.7.11 Smart Fan

Supports 1 Fan PWM control signal and 1 tachometer input for fan speed detection. Provides 2 on-module connectors with another on the carrier board following PICMG COM HPC R1.10 specifications.

1.3.7.12 BIOS

The BIOS chip is on the module by default. Users can place the BIOS chip on the carrier board with an appropriate design and jumper setting in BSEL#[2:0]

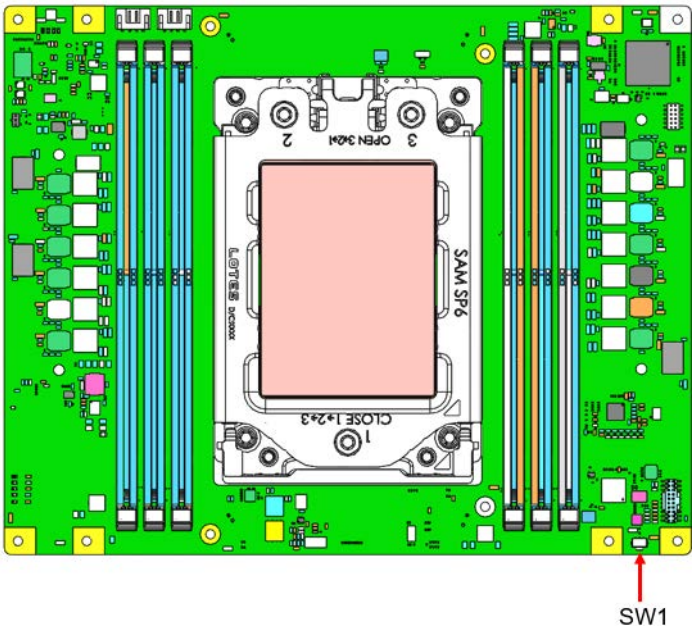
Table 1.12: BIOS

BSEL #2	BSEL #1	BSEL S#0	Boot up destination/function
NA	NA	Open	Boot from the module's SPI BIOS
NA	NA	GND	Boot from the carrier SPI BIOS

The standard module has no jumper at CN1, so BIOS settings are kept without an RTC coin battery. If you need to restore the BIOS to default settings, follow the steps below:

Table 1.13: CN1

CN1	BIOS Settings Restore default
Button	Function
1-X	Keep BIOS Settings [Default]



1. Remove the coin battery.
2. Press the button at SW1.
3. Turn on the power supply.
4. The system will boot up a few times.
5. The BIOS will load the default settings.

1.3.8 Power Management

1.3.8.1 Power Supply

Supports both ATX and AT power modes. VSB is for suspended power and can be optional if not required by standby (suspend-to-RAM) support. An RTC battery is optional if date/timekeeping is not required.

- Vin: 12V +/- 5%
- VSB: 5V +/- 5% (Suspend power)
- RTC Battery Power: 2.0V - 3.3V

1.3.8.2 PWROK

Power-good from the main power supply. A high value indicates the power level is good. This signal can be used to postpone module startup allowing carrier-based FPGAs or other configurable devices time to be programmed.

1.3.8.3 Power Sequence

According to PICMG COM-HPC Server R1.10 specifications.

1.3.8.4 Wake Event

Various wake event support allows users to apply different scenarios.

- Wake-on-LAN (WOL): Wake to S0 from S5
- USB Wake: N/A
- PCIe Device Wake: depends on user inquiry and may need customized BIOS.

1.3.9 Advantech S5 ECO Mode (Deep Sleep Mode)

Advantech iManager provides additional features allowing the system to enter a very low suspended power mode - S5 ECO mode. In this mode, the module will cut all power, including suspended and active power to the chipset, and keep an on-module controller active. Only power under 50 mW will be consumed, meaning user battery packs can last longer. While this mode is enabled in the BIOS, the system (or module) only allows power button boot instead of other methods such as WOL.

1.3.10 Environmental Specifications

1.3.10.1 Temperature

- **Operating:** 0 ~ 50°C (32 ~ 122°F)
- **Storage:** -40 ~ 85°C (-40 ~ 185°F)

1.3.10.2 Humidity

- **Operating:** 40°C @ 95% relative humidity, non-condensing
- **Storage:** 60°C @ 95% relative humidity, non-condensing

1.3.10.3 Vibrations

IEC60068-2-64: Random vibration test under non-operation mode, 3.5 Grms. For operation, please contact Advantech sales or FAE for more details.

1.3.10.4 Drop Test (Shock)

Federal Standard 101 Method 5007 test procedure with standard packing.

1.3.10.5 EMC

CE EN55032 Class B and FCC Certifications: validate with standard development boards in the Advantech chassis.

1.3.11 MTBF

Please refer to the Advantech SOM-E781 Refresh Series Reliability Prediction report on the website: http://com.advantech.com

1.3.12 OS Support

The mission of Advantech Embedded Software Services is to "Enhance the quality of life with Advantech platforms and Microsoft Windows Embedded technology." We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows Embedded software solutions easily and widely available to the embedded computing community.

To install drivers, please navigate to the website http://support.advantech.com.tw to download the setup file.

1.3.13 Advantech iManager

Advantech iManager supports APIs for GPIO, smart fan control, multi-stage watchdog timer, temperature sensor, and hardware monitoring. It follows PICMG EAPI 1.0 specifications with backward compatibility.

1.3.14 Power Consumption

Table 1.14: Power Consumption Table (Watts)						
VCC=12V, VSB=5V	**Active Power Domain**			**Suspend Power Domain**		**Mechanical Off**
Power State	S0 Max. Load	S0 Burn-in	S0 Idle	S5	S5 Deep Sleep	RTC (µA)
SOM-E781S64-U3A1	199.61	199.70	32.46	3.36	0.46	5.65

1.3.15 Hardware Configuration:

- **MB:** SOM-E781S64-U3A1
- **DRAM:** 96GB DDR5 4800MHz x 6 pcs
- **Carrier board:** SOM-DH7000-00A2

1.3.16 Test Conditions:

1. **Test temperature:** room temperature (about 25°C)
2. **Test voltage:** rated voltage DC +12V
3. **Test loading:**
   - Maximum load mode: According to Intel thermal/power test tools.
   - Burn-in mode: Burn-in test V8.1 Pro (1023) for 64-bit Windows. (CPU, RAM, 2D&3D Graphics, and Disk with 100%)
   - Idle mode: DUT power management off and not running any program.

1.3.17 Performance

To compare performance or benchmark data with other modules, please refer to the "Advantech COM Performance & Power Consumption Table."

1.3.18 Pin Description

Advantech provides useful checklists for schematic design and layout routing. The schematic checklist will specify details about each pin's electrical properties and how to connect them in different scenarios. The layout checklist will specify the layout constraints and recommendations for trace length, impedance, and other necessary information during design.

Please contact your nearest Advantech branch office or call to obtain the design documents and more advanced support.

Chapter 2

Mechanical Information

This chapter gives mechanical information on the SOM-E781 CPU Computer on Module.

Sections include:

- Board Information
- Mechanical Drawing
- Assembly Drawing

2.1 Board Information

The figures below indicate the main chips on the SOM-E781 Computer-on-Module. Please be aware of these positions while designing your own carrier board to avoid mechanical issues and ensure thermal solution contact points for best thermal dissipation performance.

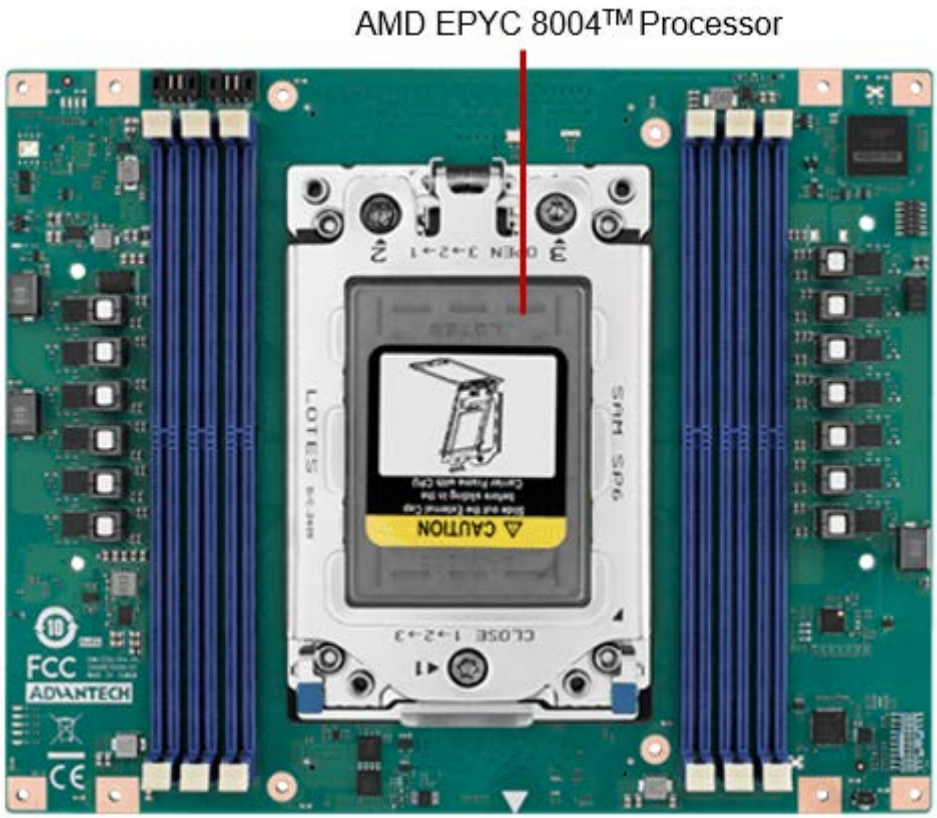


Figure 2.1 Board Chips ID – Front

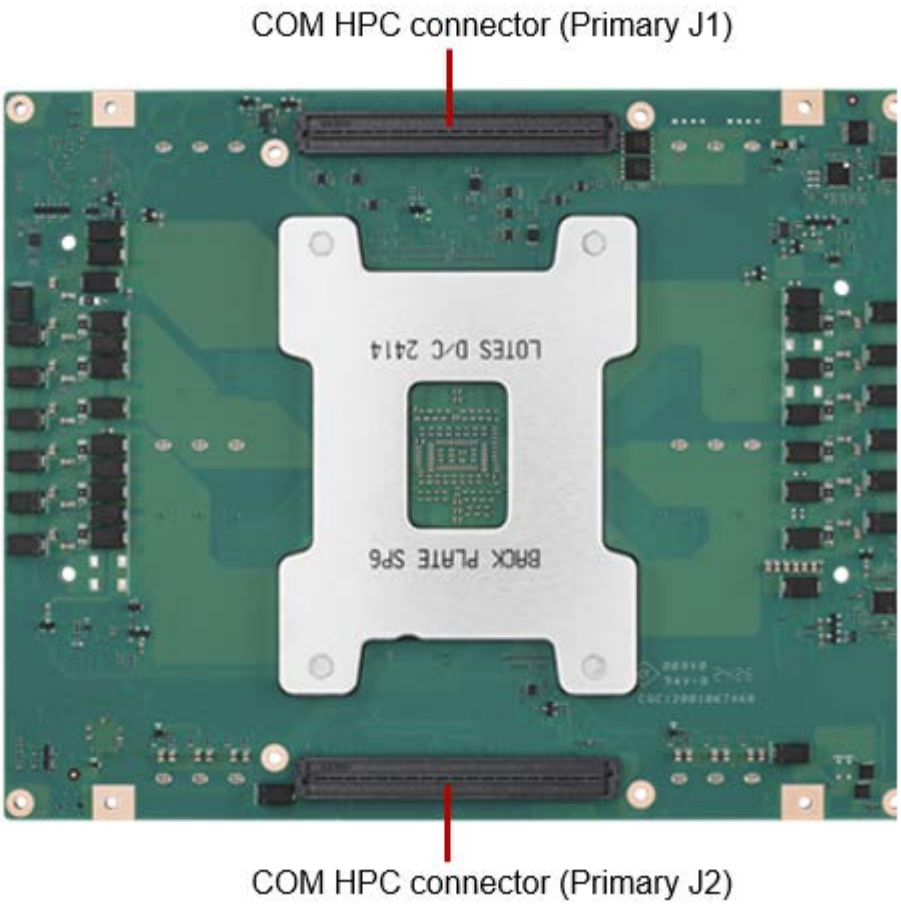


Figure 2.2 Board Chips ID – Rear

2.2 Mechanical Diagram

For more details about 2D/3D models, please check the Advantech COM support service website at http://com.advantech.com.

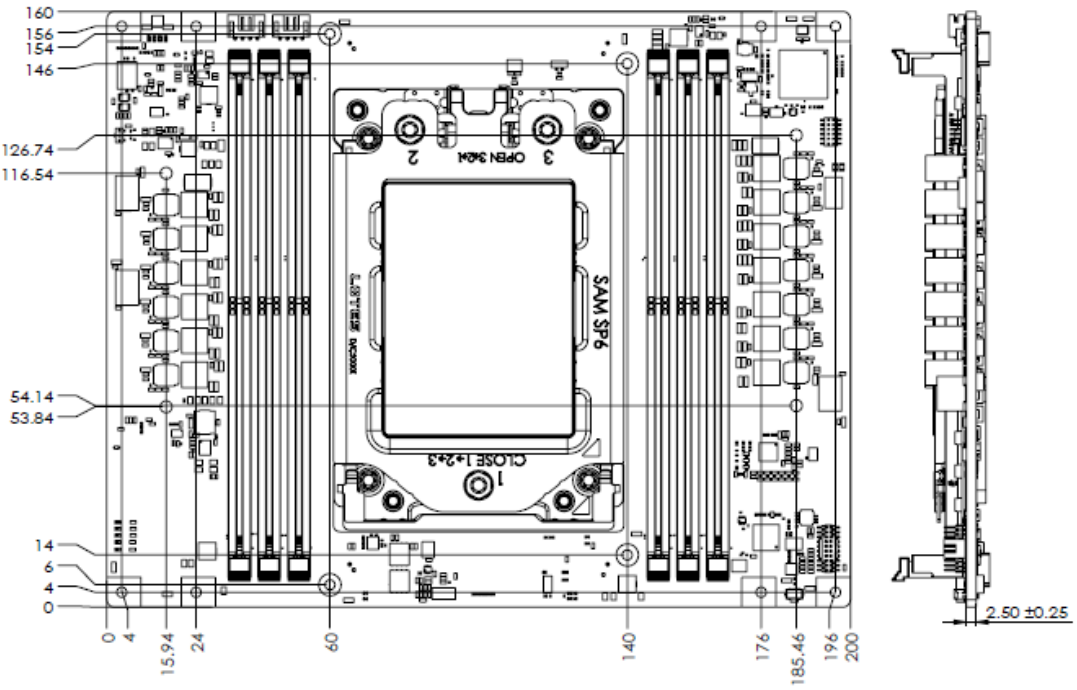


Figure 2.3 Board Mechanical Diagram - Front

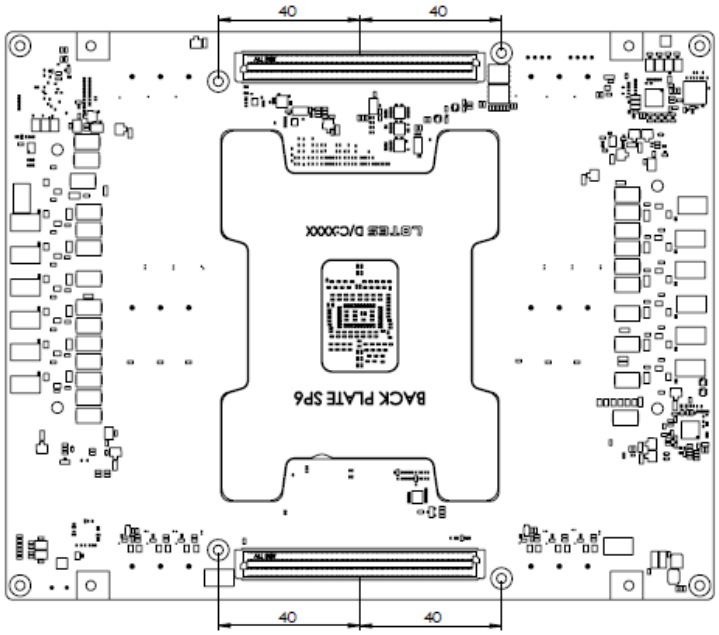


Figure 2.4 Board Mechanical Diagram - Rear

Figure 2.5 Board Mechanical Diagram – Side

2.3 Assembly Diagram

These figures demonstrate the assembly order from the thermal module, to the COM module, to the carrier board.

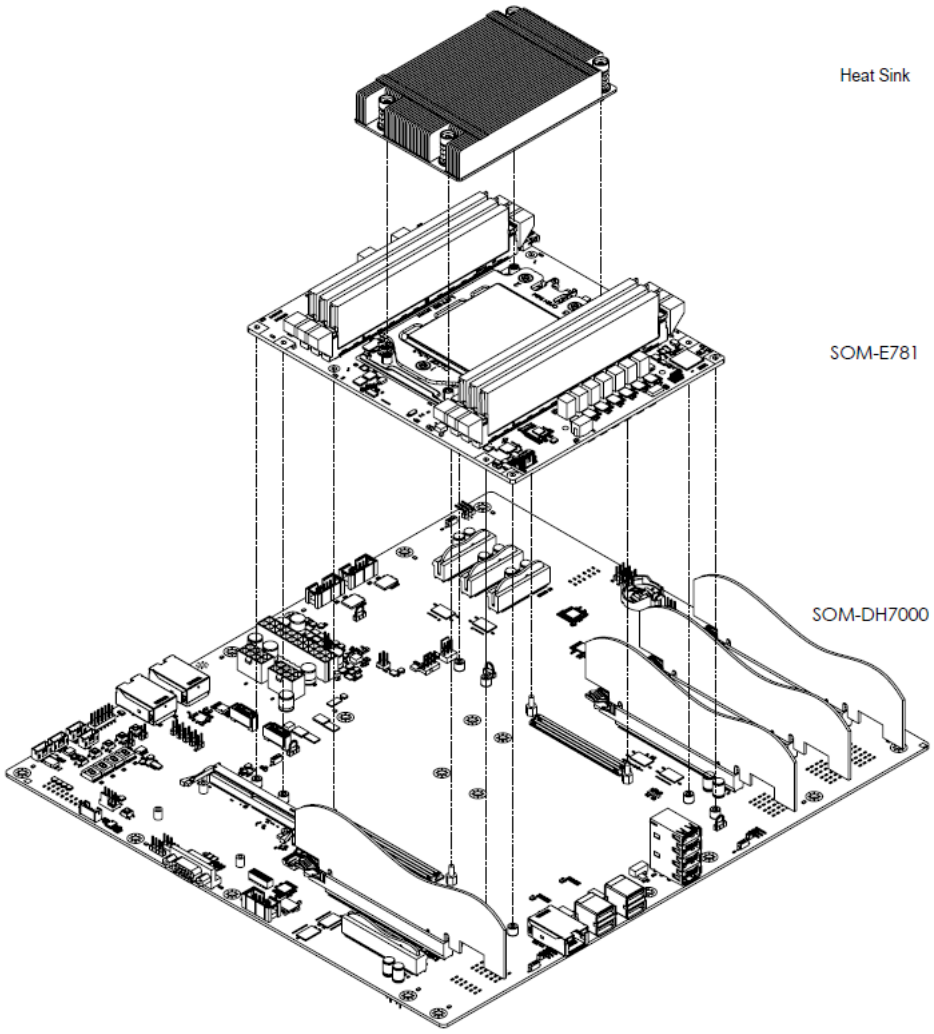


Figure 2.6 Assembly Diagram

There are 6 reserved screw holes for the SOM-E781 to be pre-assembled with a heat spreader.

2.4 Assembly Diagram

As the board to board connector of the COM-HPC is a 400-pin connector, please vertically assemble the module and carrier board and follow the allowable angle of the board to board connector as demonstrated in the following figures to avoid damage.

Mating Angle Requirements:

2.4.1 Allowable Initial Angular Misalignment

Table 2.1: Allowable Initial Angular Misalignment (1)

ROW	“A”=DEG
4	9.05
6	5.84
8	4.63
10	3.56
16	2.22

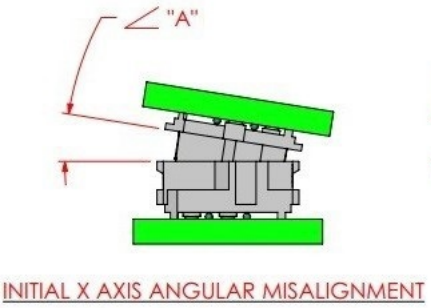


Figure 2.7 Initial Angular Misalignment (1)

Table 2.2: Allowable Initial Angular Misalignment (2)

No. of Pos.	“B”=DEG	No. of Pos.	“B”=DEG
10	11.97	60	2.37
20	6.88	70	2.00
30	4.82	80	1.71
40	3.63	90	1.49
50	2.88	100	1.31

Figure 2.8 Initial Angular Misalignment (2)

Table 2.3: Allowable Initial Angular Misalignment (3)			
No. of Pos.	**“C”=DEG**	**No. of Pos.**	**“C”=DEG**
10	3.69	60	1.46
20	2.82	70	1.30
30	2.29	80	1.17
40	1.92	90	1.07
50	1.66	100	0.98

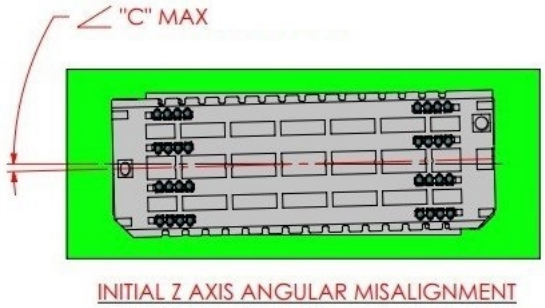


Figure 2.9 Initial Angular Misalignment (3)

2.4.2 Allowable Final Angular Misalignment

Table 2.4: Allowable Final Angular Misalignment (1)	
ROW	**“A”=DEG**
4	3.95
6	2.56
8	1.89
10	1.5
16	0.92

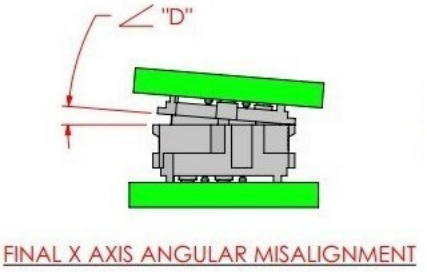


Figure 2.10 Final Angular Misalignment (1)

Table 2.5: Allowable Final Angular Misalignment (2)			
No. of Pos.	**“E”=DEG**	**No. of Pos.**	**“E”=DEG**
10	3.30	60	0.79
20	2.02	70	0.69
30	1.46	80	0.61
40	1.14	90	0.54
50	0.93	100	0.49

Figure 2.11 Final Angular Misalignment (2)

Table 2.6: Allowable Final Angular Misalignment (3)			
No. of Pos.	**“F”=DEG**	**No. of Pos.**	**“F”=DEG**
10	1.12	60	0.27
20	0.69	70	0.23
30	0.50	80	0.21
40	0.39	90	0.19
50	0.32	100	0.17

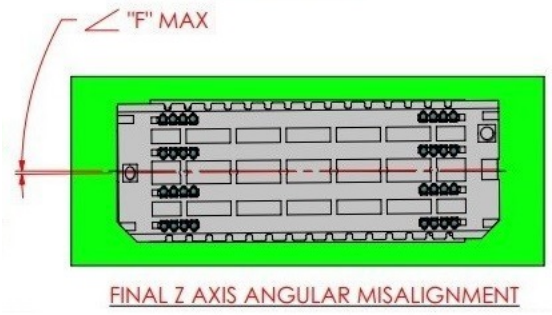


Figure 2.12 Final Angular Misalignment (3)

2.5 CPU Package Design

Please consider the CPU and chip height tolerance when designing your thermal solution.

Table 2.7: CPU Package Design	
Item	LGA
IHS to MB Height (validated range)	8.6 ~ 7.8 mm

Figure 2.9 CPU and CPU Socket Height and Tolerance

Chapter 3

AMI BIOS

This chapter gives BIOS setup information for the SOM-E781 CPU Computer on Module.

Sections include:

- Introduction
- Entering Setup
- Hot/Operation Key
- Exit BIOS Setup Utility

3.1 Introduction

AMI BIOS has been integrated into many motherboards for over a decade. With the AMI BIOS Setup Utility, users can modify BIOS settings and control various system features. This chapter describes the basic navigation of the BIOS Setup Utility.

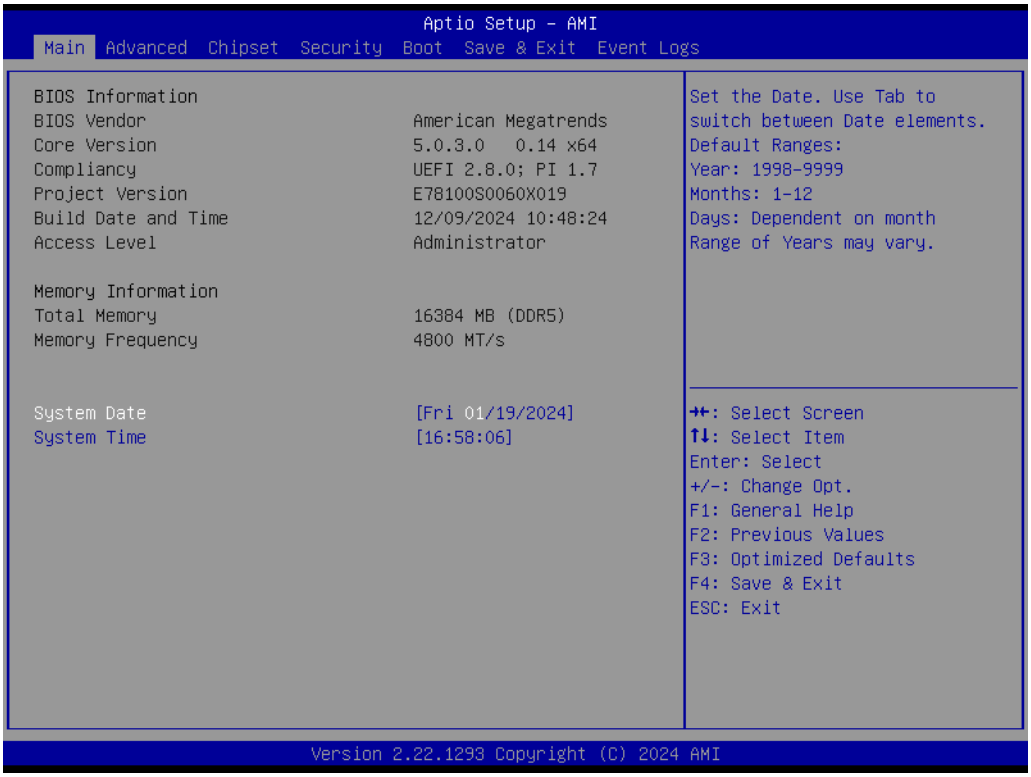


Figure 3.1 Setup Program Initial Screen

AMI's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in flash ROM so it retains the Setup information when the power is turned off.

3.2 Entering Setup

Turn on the computer and then press <DEL> or <ESC> to enter the Setup menu.

3.2.1 Main Setup

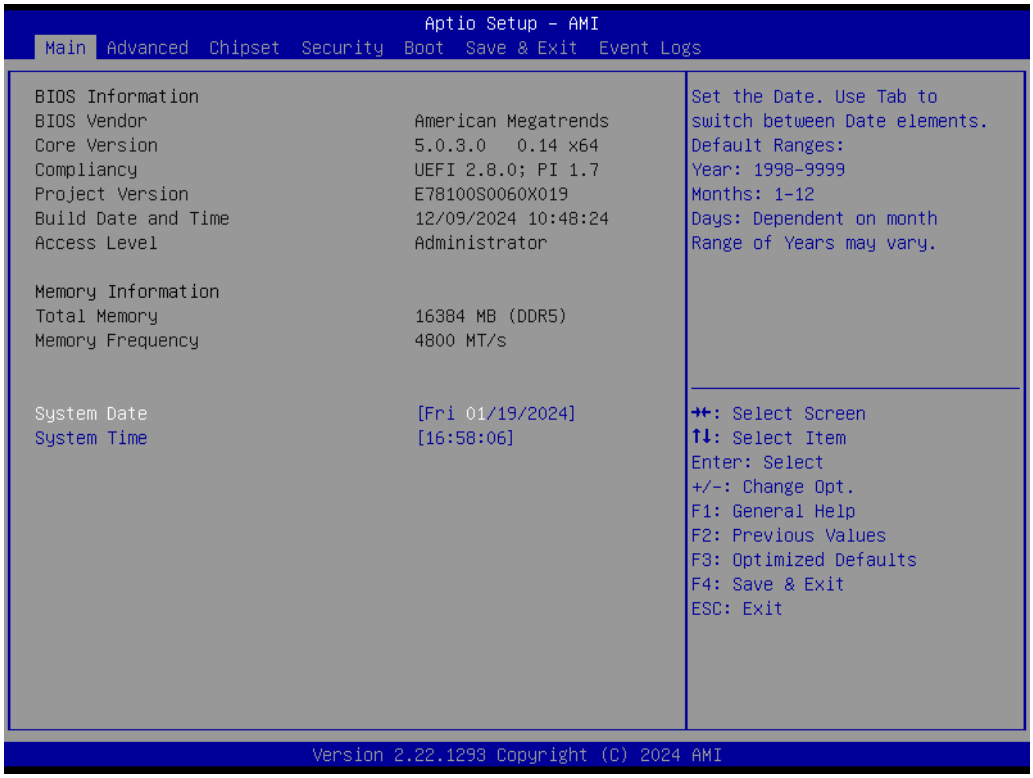


Figure 3.2 Main Setup Screen

- **System Date**
  Set the Date. Use Tab to switch between Date elements.
  Default Ranges:
  Year: 1998-9999
  Months: 1-12
  Days: Dependent on the month; the Range of Years may vary.
- **System Time**
  Set the Time. Use Tab to switch between Time elements.

3.2.2 Advanced BIOS Features Setup

Figure 3.3 Advanced Features Setup Screen

3.2.2.1 Trusted Computing

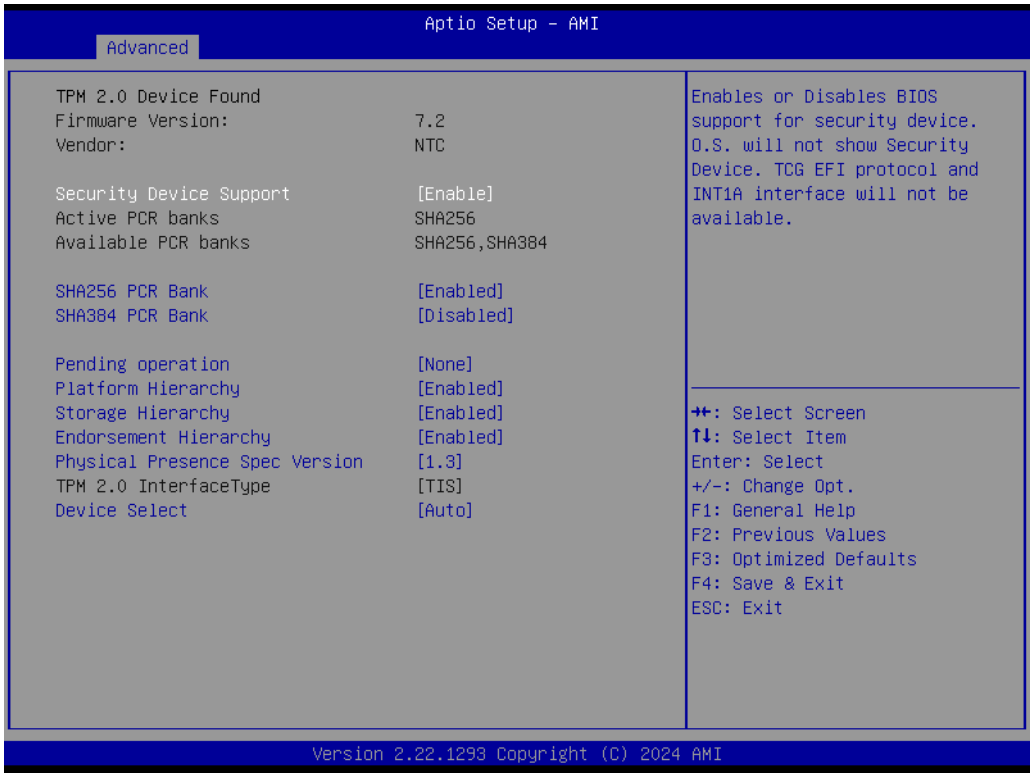


Figure 3.4 Trusted Computing

- **Security Device Support**
  Enable or Disable BIOS support for a security device. The OS will not show the Security Device. The TCG EFI protocol and INT1A interface will not be available.
- **SHA256 PCR Bank**
  Enable or Disable SHA256 PCR Bank.
- **SHA384 PCR Bank**
  Enable or Disable SHA384 PCR Bank.
- **Pending operation**
  Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change the State of Security Device.
- **Platform Hierarchy**
  Enable or Disable Platform Hierarchy.
- **Storage Hierarchy**
  Enable or Disable Storage Hierarchy.
- **Endorsement Hierarchy**
  Enable or Disable Endorsement Hierarchy.
- **Physical Presence Spec Version**
  Select to tell the OS to support PPI Spec Version 1.2 or 1.3. Note: some HCK tests might not support 1.3.
- **Device Select**
  TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support for TPM 2.0 devices. Auto will support both with the default set to TPM 2.0 devices if not found, and TPM 1.2 devices will be enumerated.

3.2.2.2 PSP Firmware Versions

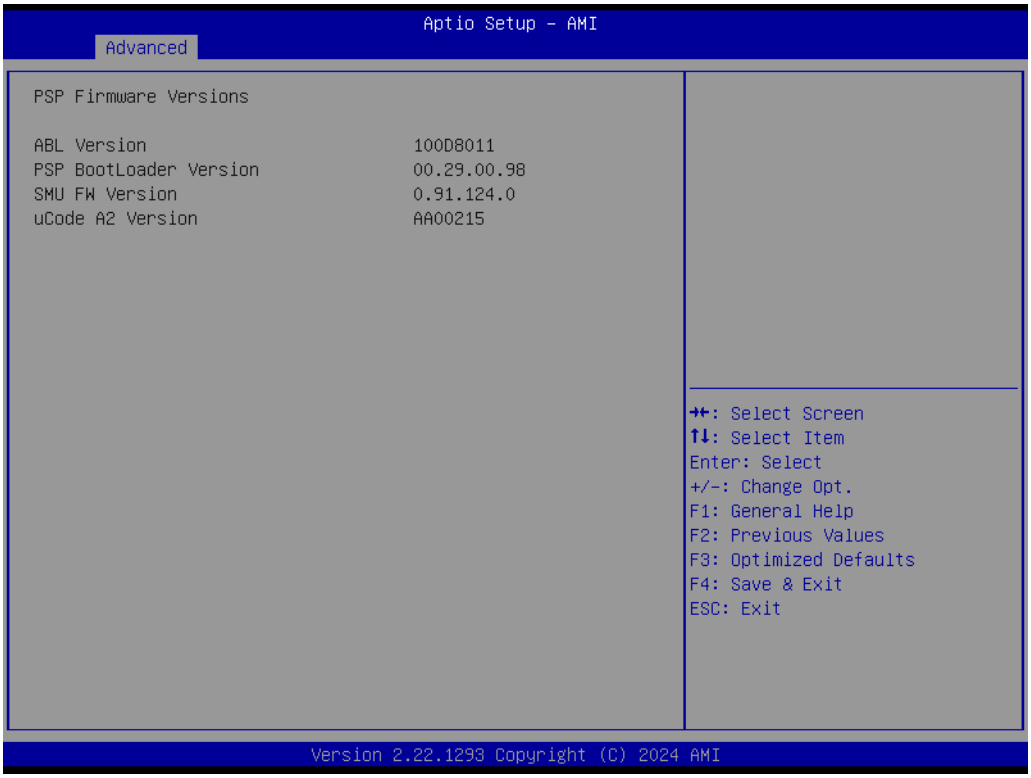


Figure 3.5 PSP Firmware Versions

3.2.2.3 ACPI Settings

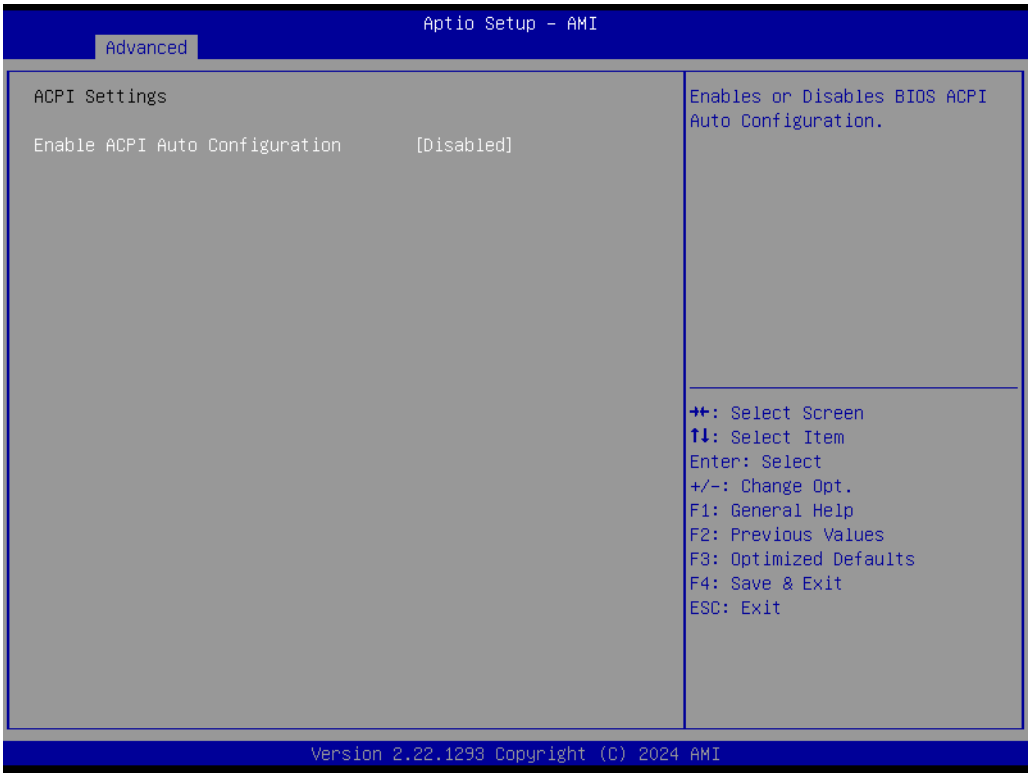


Figure 3.6 ACPI Settings

- **Enable ACPI Auto Configuration**
  Enable or Disable BIOS ACPI Auto Configuration.

3.2.2.4 Embedded Controller

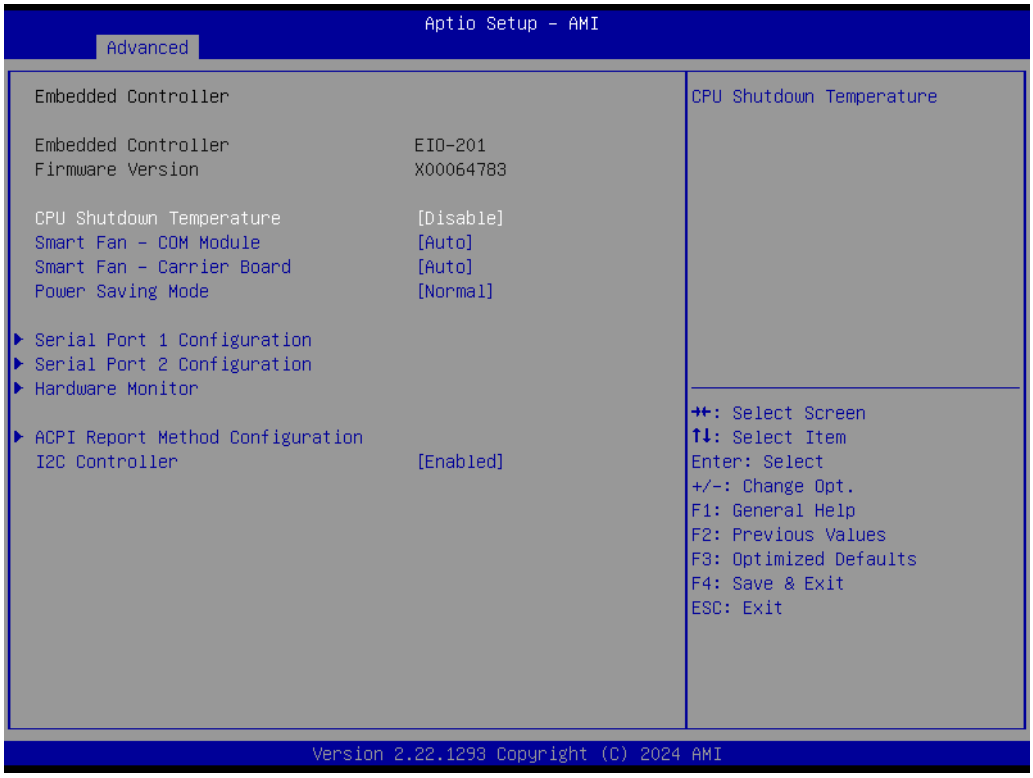


Figure 3.7 Embedded Controller

- **CPU Shutdown Temperature**
  CPU Shutdown Temperature.
- **Smart Fan - COM Module**
  Control COM Module Smart FAN function. Get the value from EC and only set the value when you Saves Changes.
- **Smart Fan - Carrier Board**
  Control Carrier Board Smart FAN function. Get the value from EC and only set the value when you Save Changes.
- **Power Saving Mode**
  Select Power Saving Mode.
- **Serial Port 1 Configuration**
  Set Parameters of Serial Port 1 (COMA).
- **Serial Port 2 Configuration**
  Set Parameters of Serial Port 2 (COMB).
- **Hardware Monitor**
  Monitor hardware status.
- **ACPI Report Method Configuration**
  Select ACPI Reporting Method for EC Devices.
- **I^2C Controller**
  Enable/Disable I2C controller on RDC-IS200.

Serial Port 1 Configuration

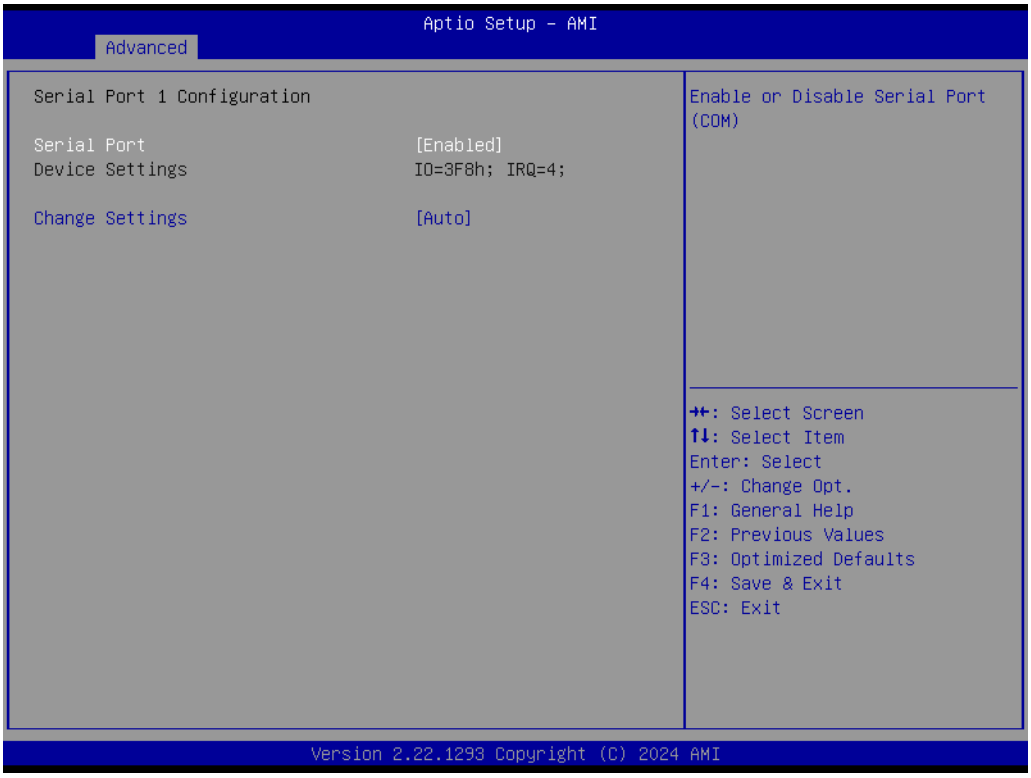


Figure 3.8 Serial Port 1 Configuration

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select optimal settings for a Super IO Device.

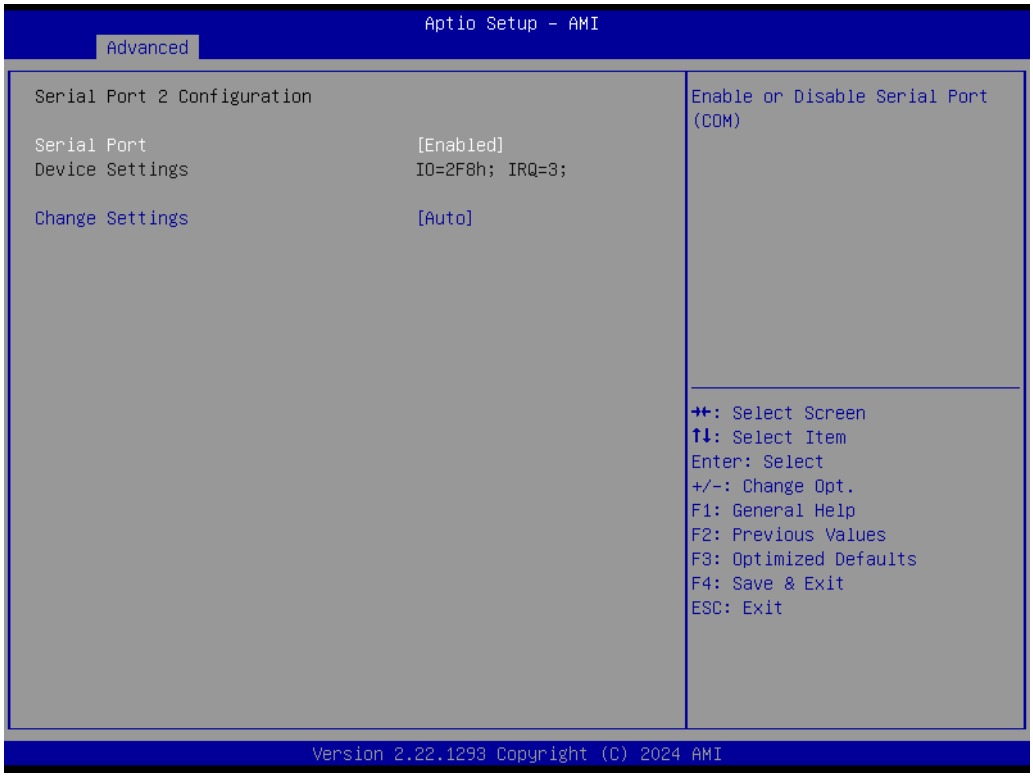


Figure 3.9 Serial Port 2 Configuration

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for Super IO Device.

Hardware Monitor

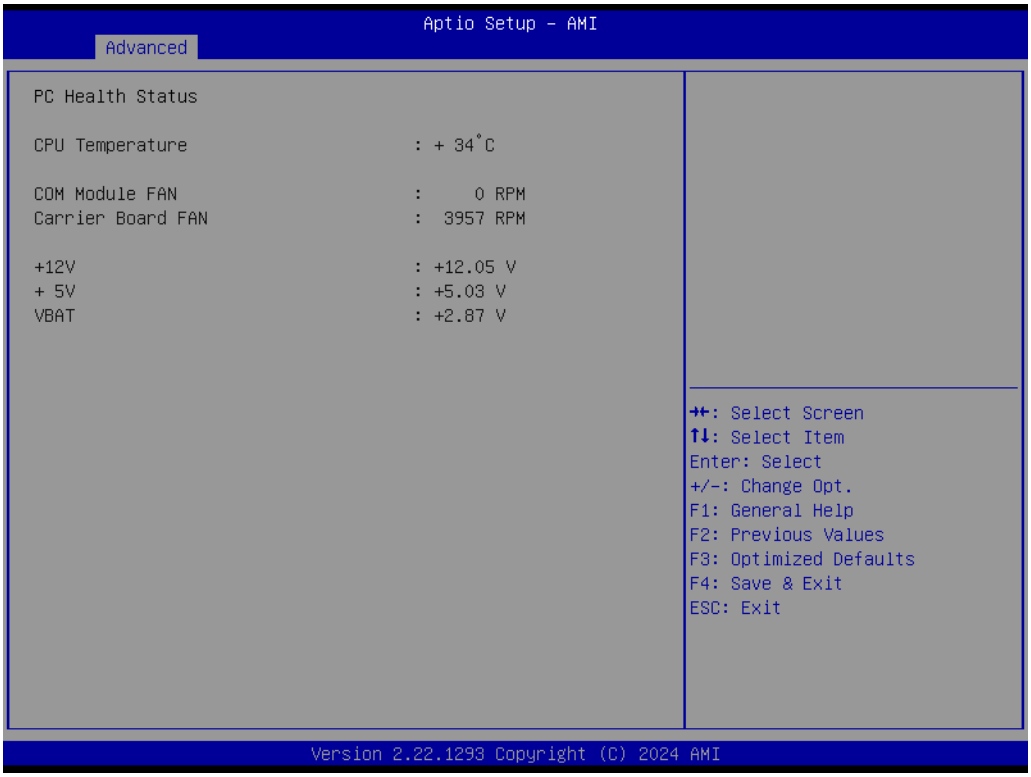


Figure 3.10 Hardware Monitor

ACPI Report Method Configuration

Figure 3.11 ACPI Report Method Configuration

- **Active High-Speed VOM Port**
  Standard -> Standard COM Port. High Speed -> High Speed COM Port. (Driver installation is necessary.)
- **ACPI Report Method for I2C Bus**
  Select the ACPI reporting method for EC I2C Bus.
  Hidden -> Reported as reserved motherboard resource.
  Exposed -> Reported vensor_HID. (Driver installation is necessary.)

3.2.2.5 Serial Port Console Redirection

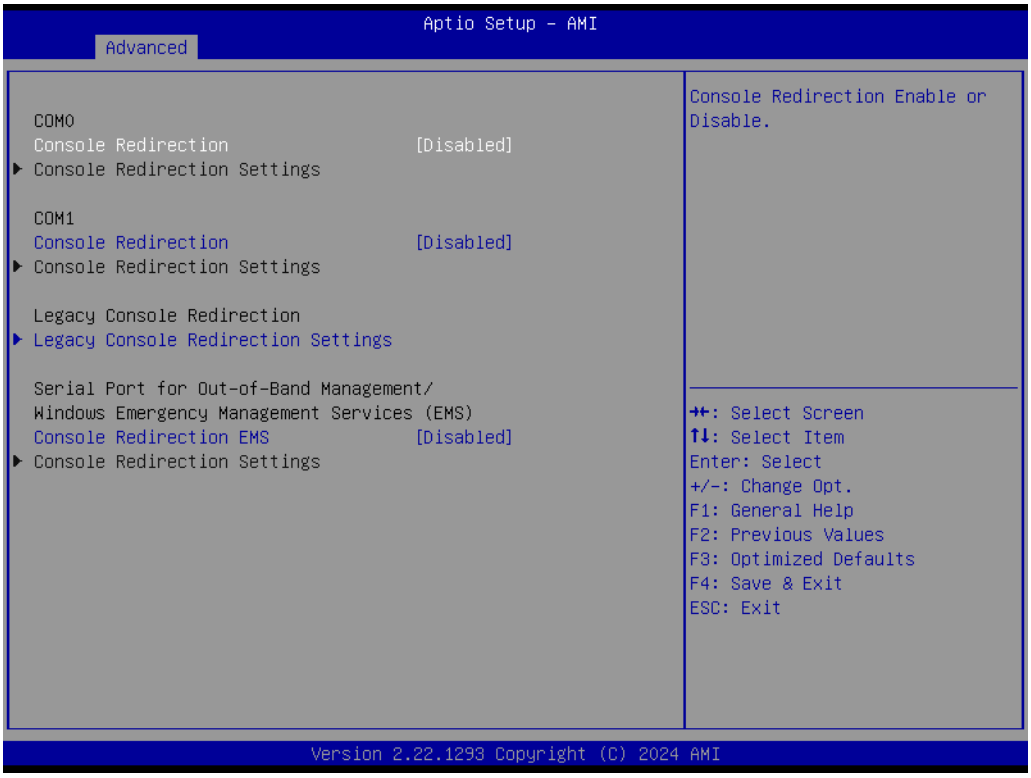


Figure 3.12 Serial Port Console Redirection

- **Legacy Console Redirection Settings**
  Legacy Console Redirection Settings.
- **Console Redirection EMS**
  Console Redirection Enable or Disable.

3.2.2.6 CPU Configuration

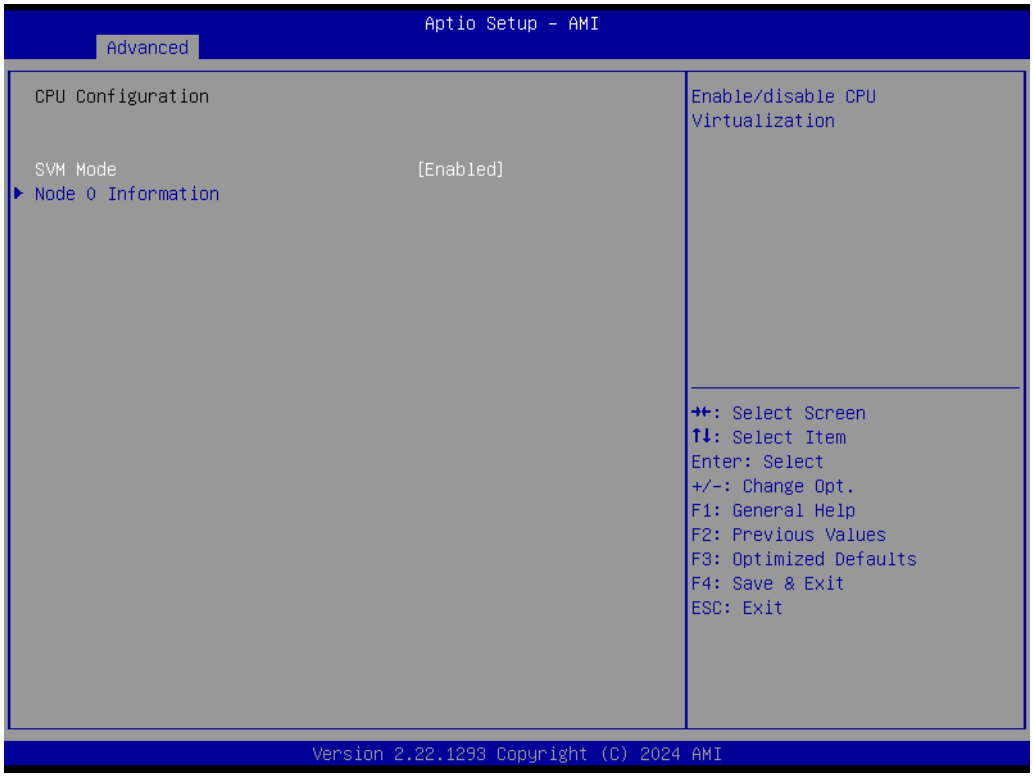


Figure 3.13 CPU Configuration

- **SVM Mode**
  Enable/Disable CPU Virtualization.
- **Nude 0 Information**
  View Memory Information related to Nude 0.

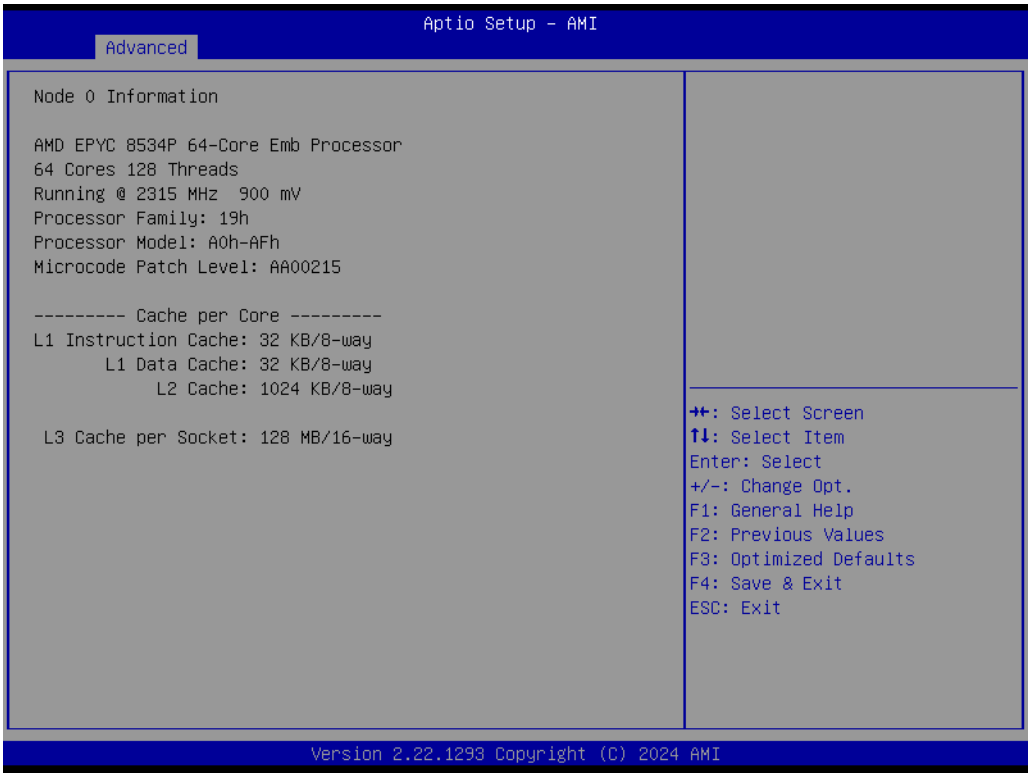


Figure 3.14 Nude 0 Information

3.2.2.7 Debug Port Table Configuration

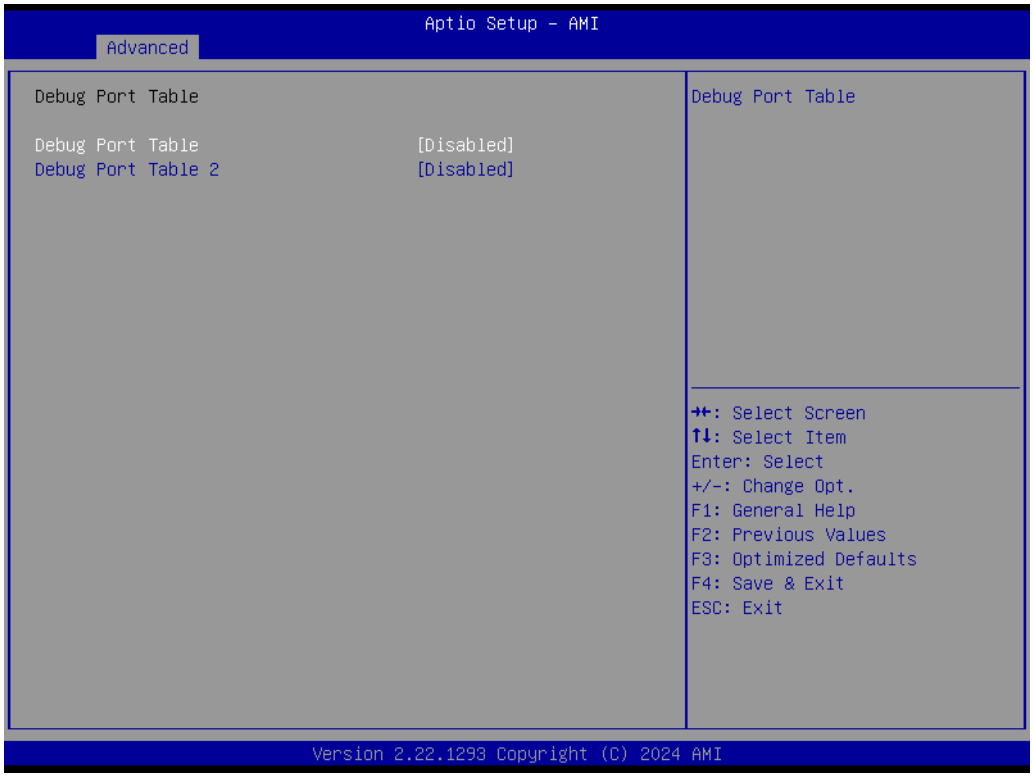


Figure 3.15 Debug Port Table Configuration

- **Debug Port Table**
  Debug Port Table.
- **Debug Port Table 2**
  Debug Port Table 2.

3.2.2.8 SI0 Common Setting

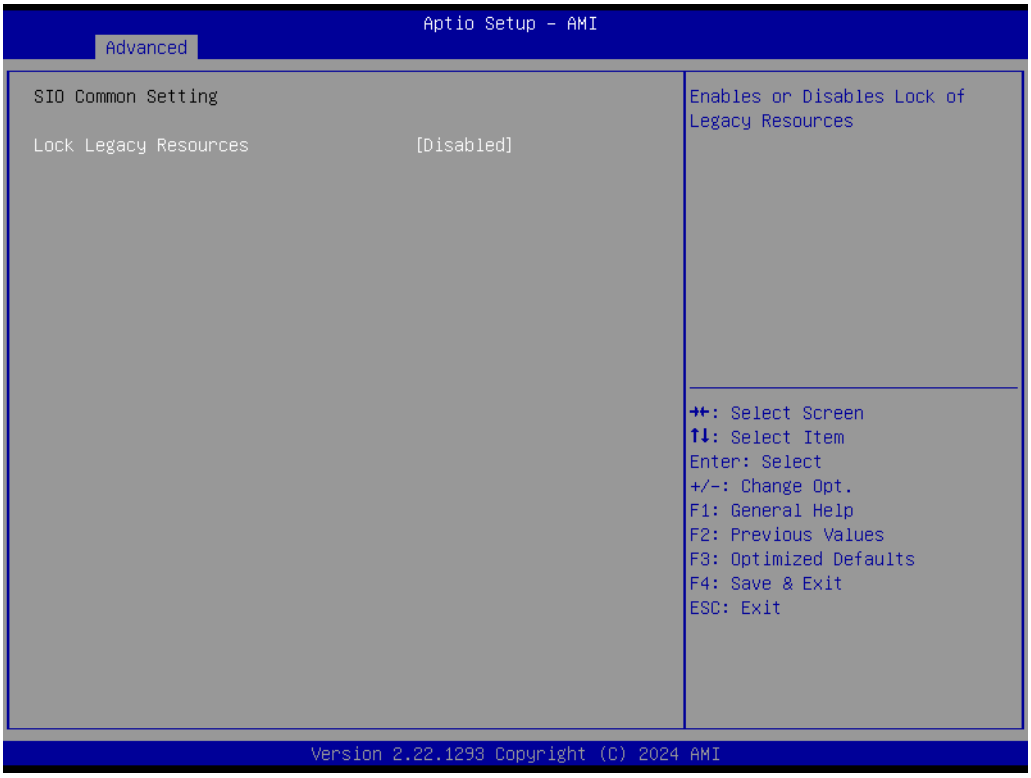


Figure 3.16 SI0 Common Setting

- **Lock Legacy Resource**
  Enable or Disable Lock of Legacy Resources.

3.2.2.9 PCI Subsystem Settings

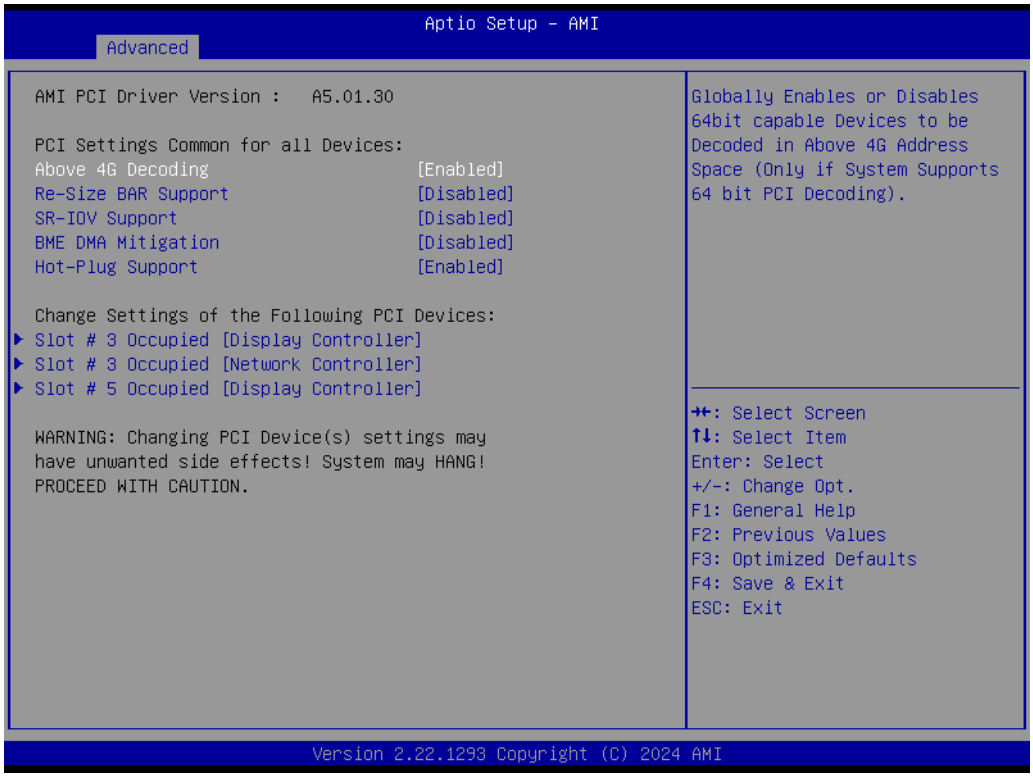


Figure 3.17 PCI Subsystem Settings

- **Above 4G Decoding**
  Globally Enables or Disables 64-bit capable Devices to be Decoded Above 4G. Address Space (Only if System Supports 64-bit PCI Decoding).
- **Re-Size BAR Support**
  If the system has Resizable BAR capable PCIe Devices, this option Enables or Disables Resizable BAR Support.
- **SR-IOV Support**
  If the system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.
- **BME DMA Mitigation**
  Re-enable Bus Master Attribute if disabled during Pci enumeration for PCI Bridges after SMM Locked.
- **Hot-Plug Support**
  Globally Enables or Disables Hot-Plug for the entire System. If the System has Hot- Plug capable Slots and this option is set to Enabled, it provides a Setup Screen for selecting PCI resource padding for Hot-Plug.
- **Slot # 3 Occupied [Display Controller]**
  Change on-board PCI Device or PCI Slot Settings.
- **Slot # 3 Occupied [Network Controller]**
  Change on-board PCI Device or PCI Slot Settings.
- **Slot # 5 Occupied [Display Controller]**
  Change on-board PCI Device or PCI Slot Settings.

3.2.2.10 USB Configuration

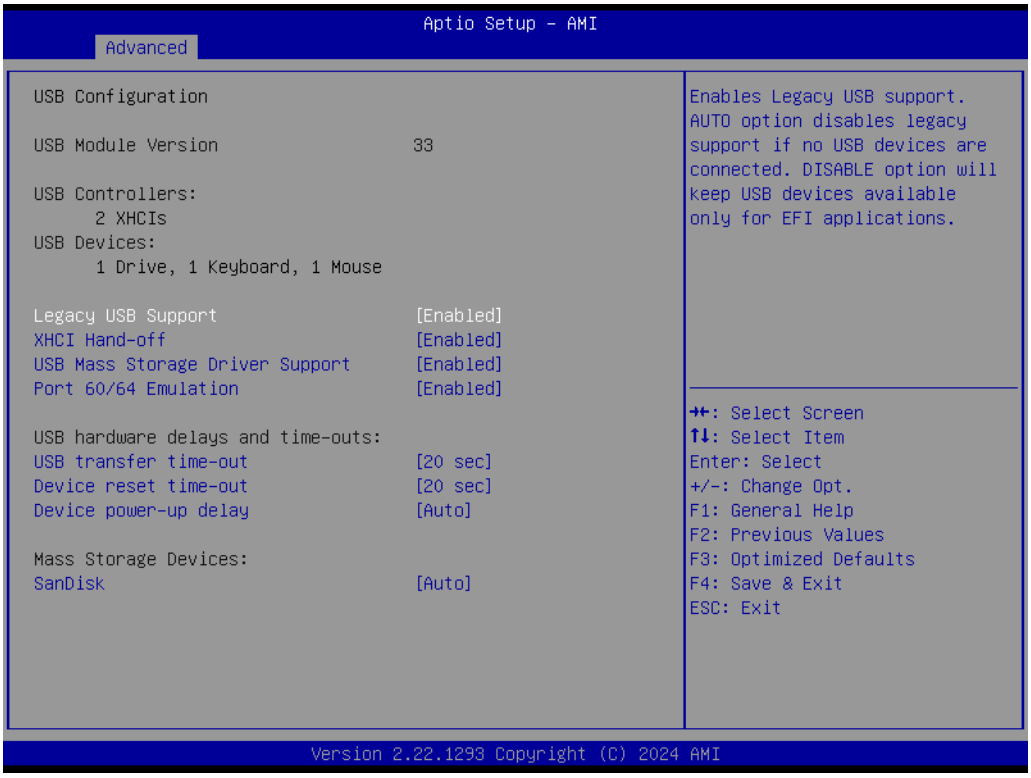


Figure 3.18 USB Configuration

- **Legacy USB Support**
  Enables Legacy USB support. The AUTO option disables legacy support if no USB devices are connected. The DISABLE option will keep USB devices available only for EFI applications.
- **XHCI Hand-off**
  This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI driver.
- **USB Mass Storage Driver Support**
  Enable/Disable USB Mass Storage Driver Support.
- **Port 60/64 Emulation**
  Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OS.
- **USB transfer time-out**
  The time-out value for Control, Bulk, and Interrupt transfers.
- **Device reset time-out**
  USB mass storage device Start Unit command time-out.
- **Device power-up delay**
  Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses the default value: for a Root port it is 100 ms, for a Hub port the delay is taken from the Hub descriptor.

3.2.2.11 Network Stack Configuration

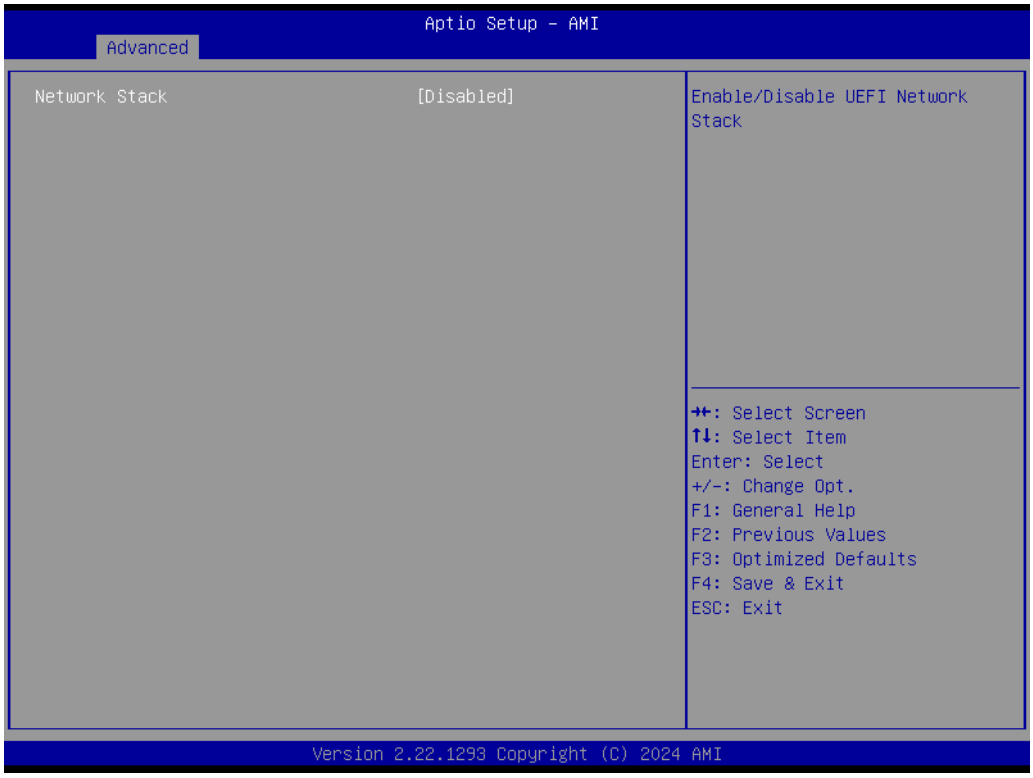


Figure 3.19 Network Stack Configuration

- **Network Stack**
  Enable/Disable UEFI Network Stack.

3.2.2.12 NVMe Configuration

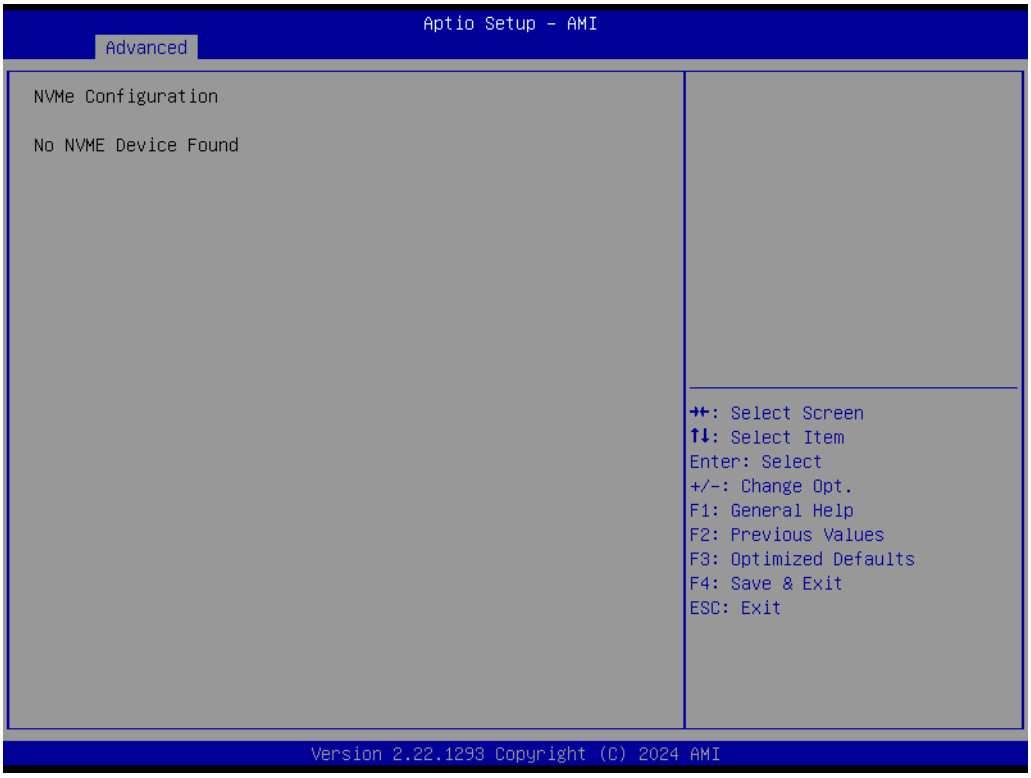


Figure 3.20 NVMe Configuration

3.2.2.13 SATA Configuration

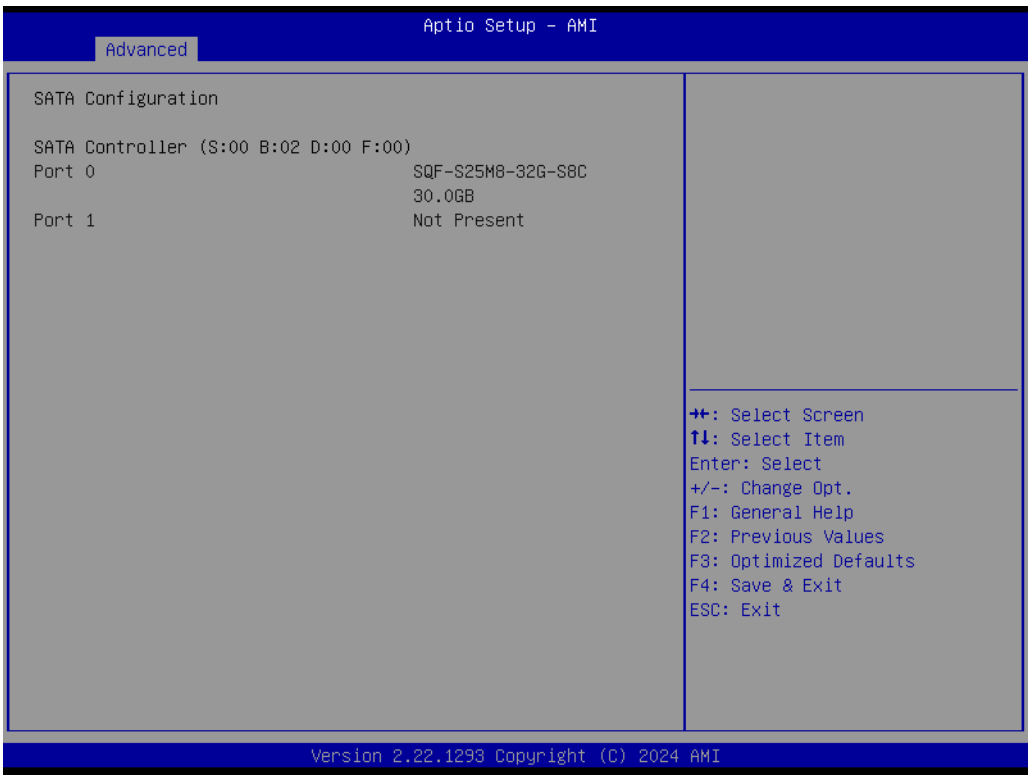


Figure 3.21 SATA Configuration

3.2.2.14 Option ROM Dispatch Policy

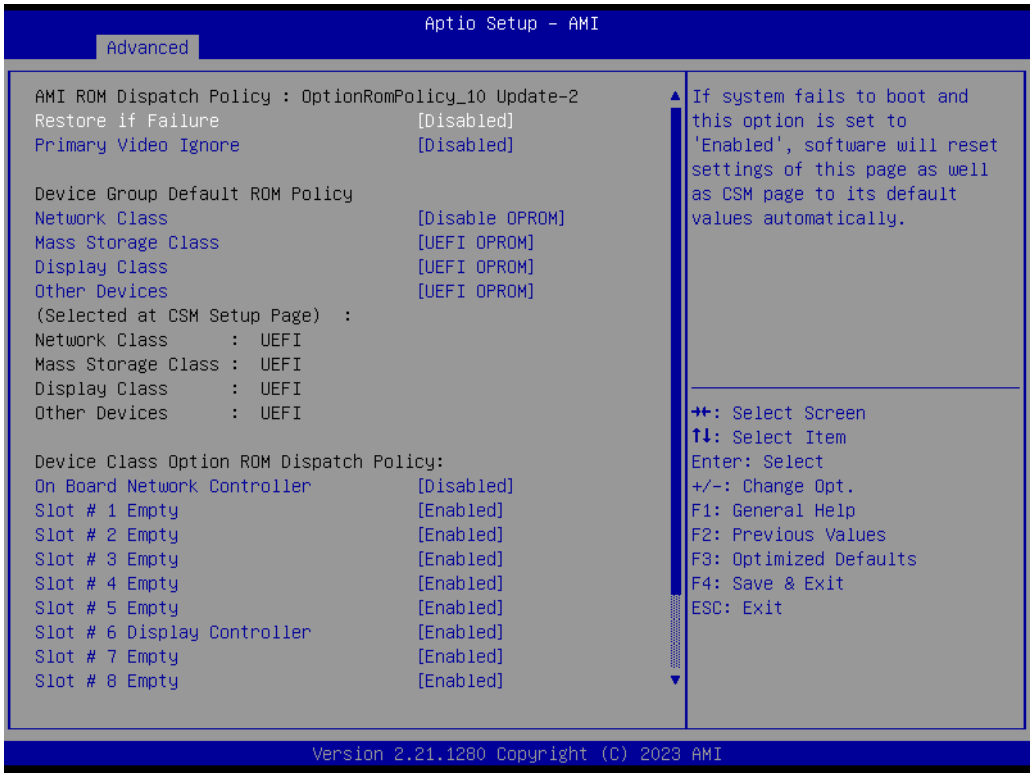


Figure 3.22 Option ROM Dispatch Policy

- **On Board NOT FOUND**
  Option Rom Devices 0 Help:
- **Slot #1 Empty**
  Option Rom Device 1 Help:
- **Slot #2 Empty**
  Option Rom Device 2 Help:
- **Slot #3 Empty**
  Option Rom Device 3 Help:
- **Slot #3 Empty**
  Option Rom Device 3 Help:
- **Slot #4 Empty**
  Option Rom Device 4 Help:
- **Slot #4 Empty**
  Option Rom Device 4 Help:
- **Slot #5 Empty**
  Option Rom Device 5 Help:
- **Slot #6 Empty**
  Option Rom Device 6 Help:
- **Slot #7 Empty**
  Option Rom Device 7 Help:
- **Slot #8 Empty**
  Option Rom Device 8 Help:
- **Slot #9 Empty**
  Option Rom Device 9 Help:
- **Slot #11 Empty**
  Option Rom Device 11 Help:

- **Slot #41 Empty**
  Option Rom Device 41 Help:
- **Slot #42 Empty**
  Option Rom Device 42 Help:
- **Slot #43 Empty**
  Option Rom Device 43 Help:
- **Slot #51 Empty**
  Option Rom Device 51 Help:
- **Slot #52 Empty**
  Option Rom Device 52 Help:
- **Slot #53 Empty**
  Option Rom Device 53 Help:
- **Slot #61 Empty**
  Option Rom Device 61 Help:
- **Slot #62 Empty**
  Option Rom Device 62 Help:
- **Slot #63 Empty**
  Option Rom Device 63 Help:
- **Slot #71 Empty**
  Option Rom Device 71 Help:
- **Slot #72 Empty**
  Option Rom Device 72 Help:
- **Slot #73 Empty**
  Option Rom Device 73 Help:

3.2.2.15 AMD Mem Configuration Status

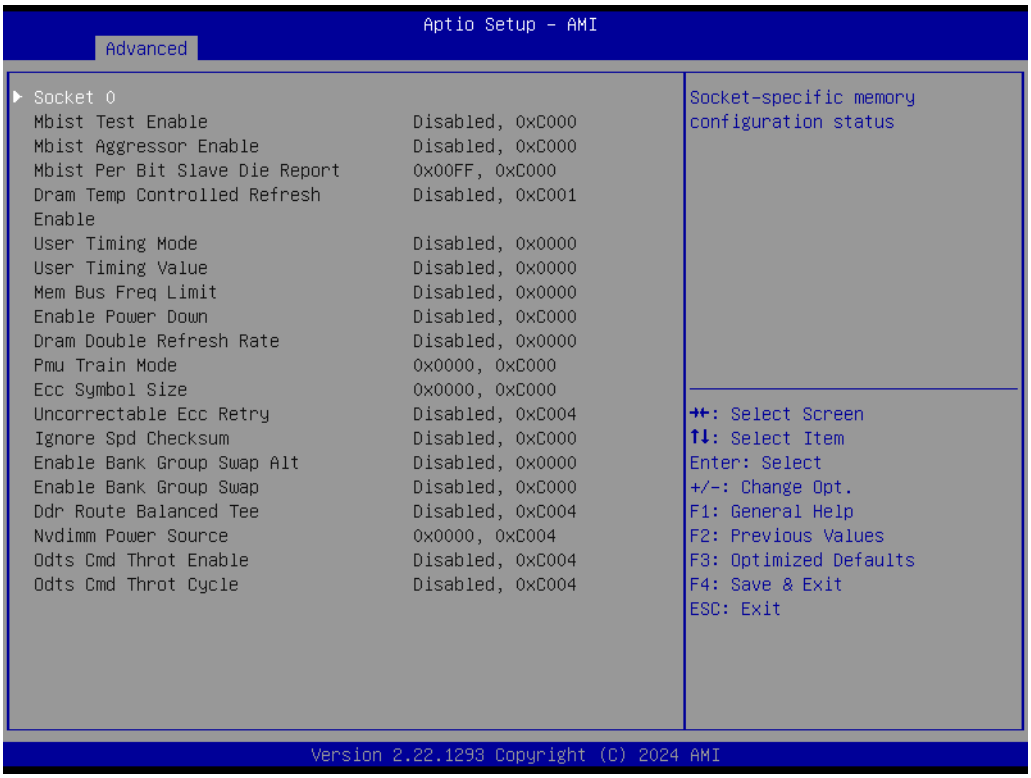


Figure 3.23 AMD Mem Configuration Status

- **Socket 0**
  Socket-specific memory configuration status.

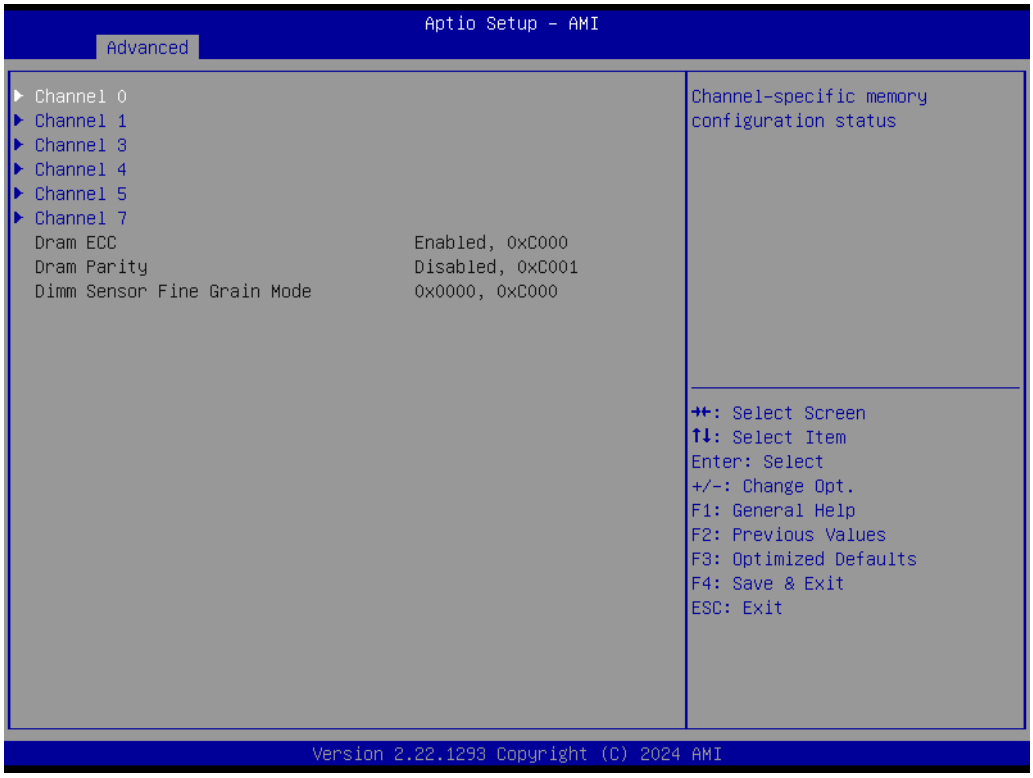


Figure 3.24 Socket 0

- **Channel 0**
  Channel-specific memory configuration status.
- **Channel 1**
  Channel-specific memory configuration status.
- **Channel 3**
  Channel-specific memory configuration status.
- **Channel 4**
  Channel-specific memory configuration status.
- **Channel 5**
  Channel-specific memory configuration status.
- **Channel 7**
  Channel-specific memory configuration status.

3.2.2.16 Tls Auth Configuration

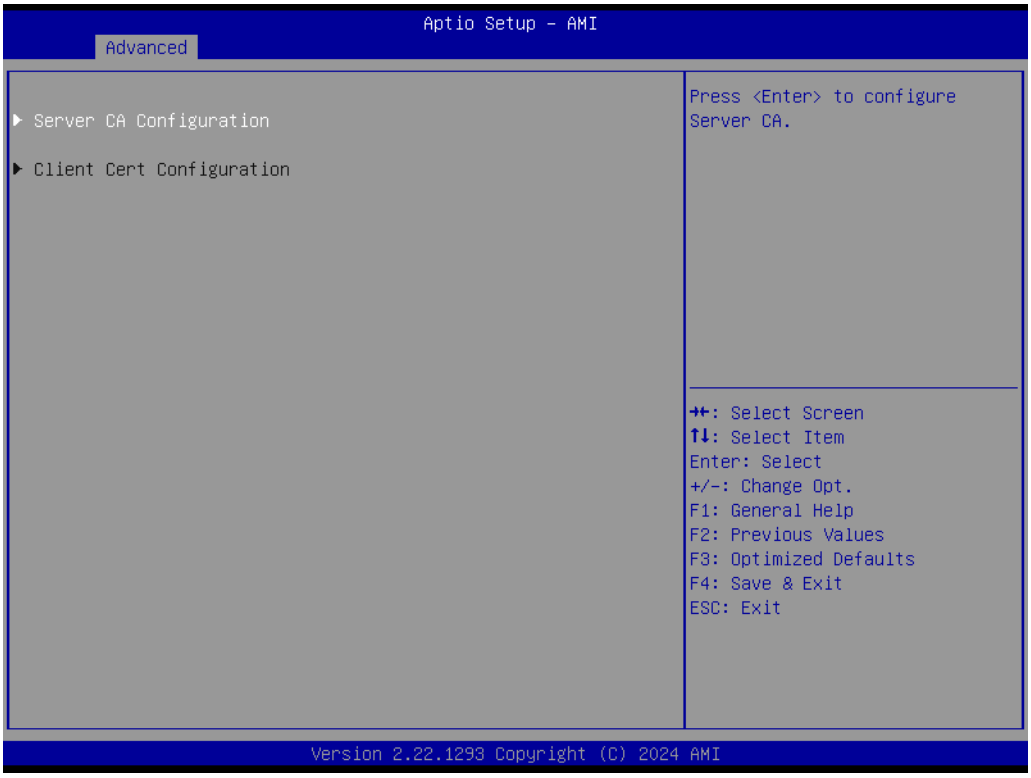


Figure 3.25 Tls Auth Configuration

- **Server CA Configuration**
  Press <Enter> to configure Server CA.

3.2.2.17 RAM Disk Configuration

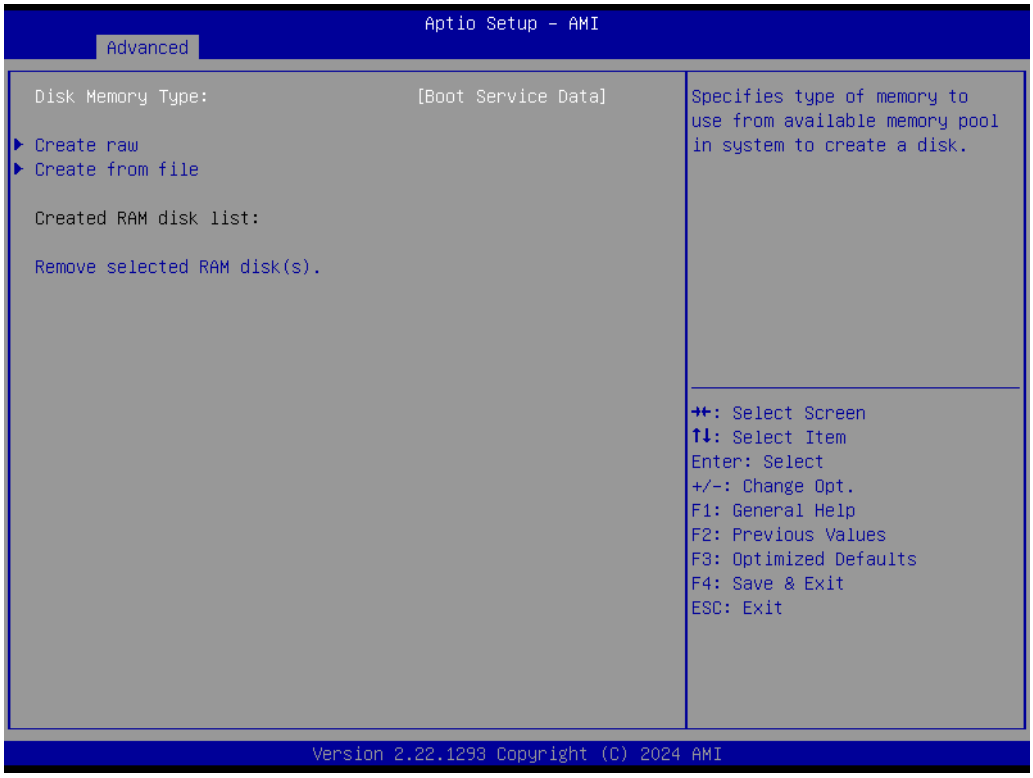


Figure 3.26 RAM Disk Configuration

- **Disk Memory Type**
  Specifies the type of memory to use from the available memory pool in the system to create a disk.
- **Create raw**
  Create a raw RAM disk.
- **Create from file**
  Create a RAM disk from a given file.
- **Remove selected RAM disk(s).**
  Remove selected RAM disk(s).

3.2.2.18 Intel® Ethernet Controller I226-LM-74:FE:48:97:81:B5

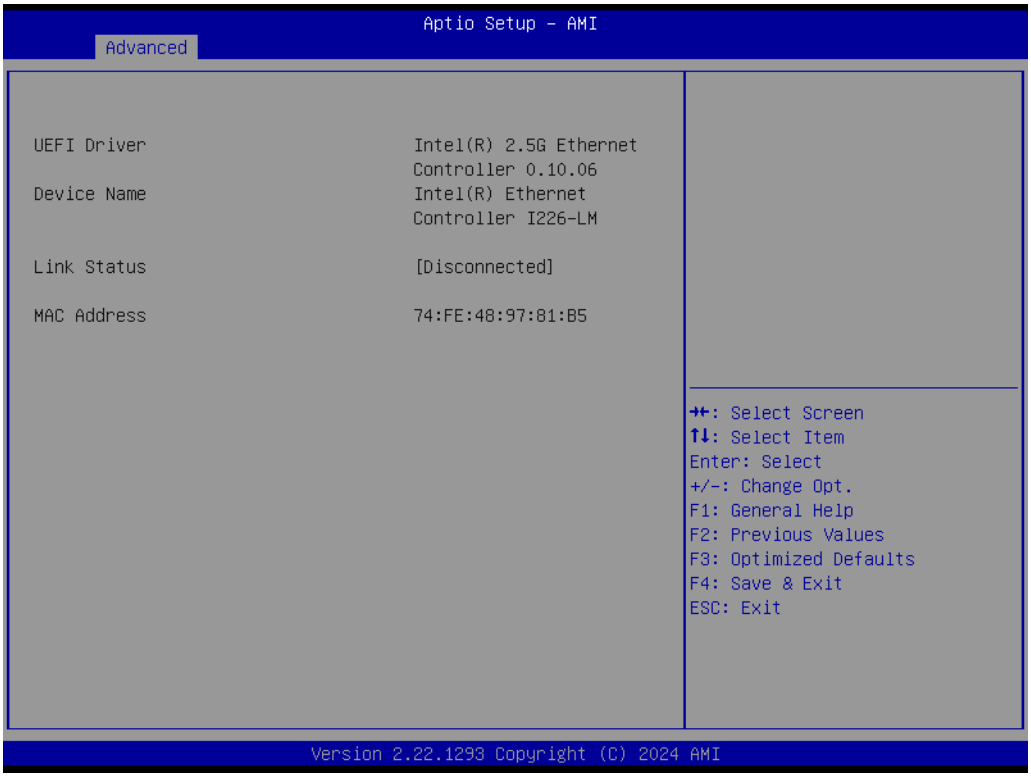


Figure 3.27 Intel® Ethernet Controller

3.2.3 Chipset Setup

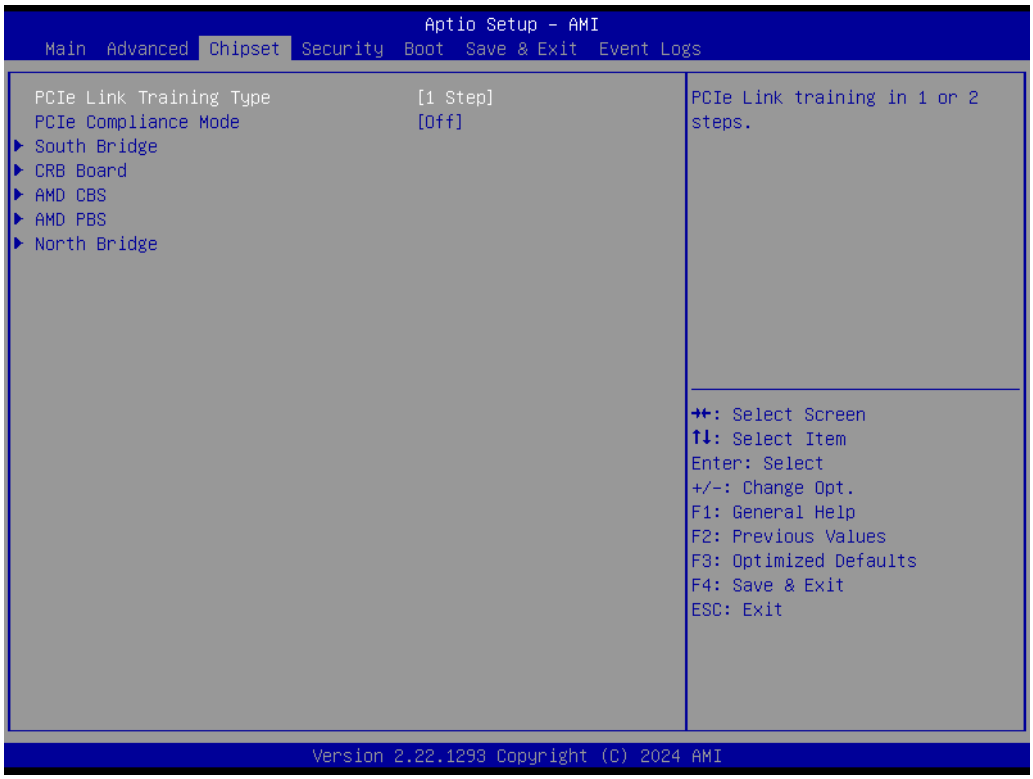


Figure 3.28 Chipset Setup

- **PCIe Link Training Type**
  PCIe Link training in 1 or 2 steps.
- **PCIe Compliance Mode**
  PCIe Link Compliance Mode.
- **South Bridge**
  South Bridge Parameters.
- **CRB Board**
  CRB Board Parameters.
- **AMD CBS**
  AMD CBS Setup Page.
- **AMD PBS**
  AMD PBS Setup Page.
- **North Bridge**
  North Bridge Parameters.

3.2.3.1 South Bridge

Figure 3.29 South Bridge

- **SB Debug Configuration**
  Options For SB Debug Features.

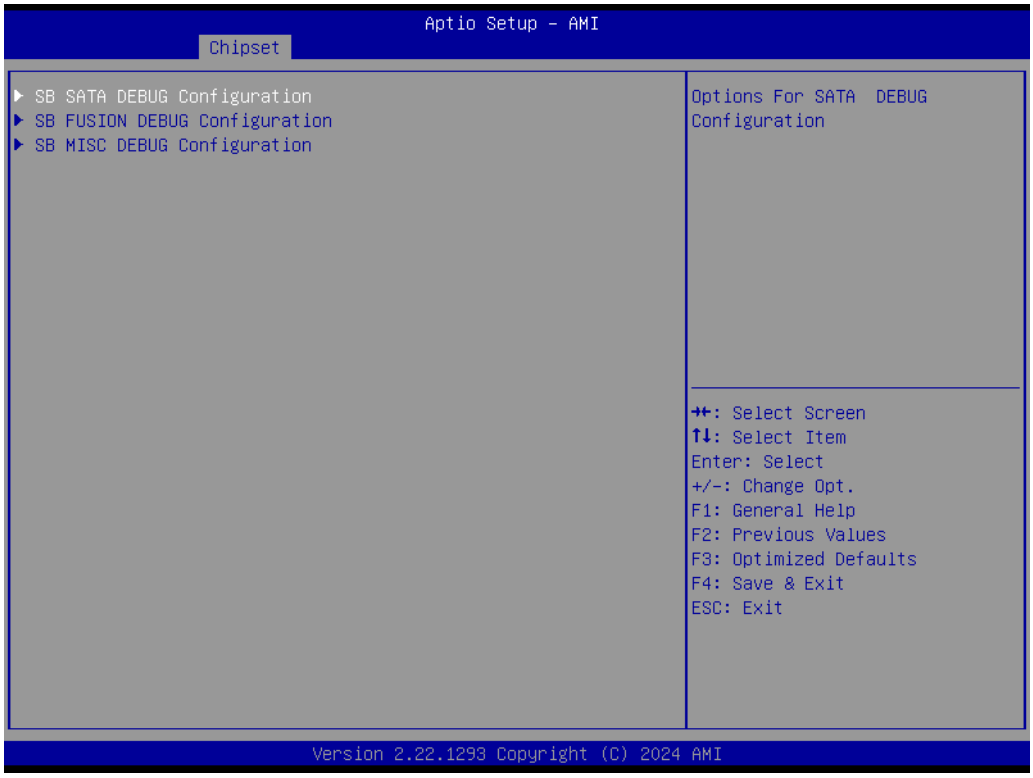


Figure 3.30 SB Debug Configuration

- **SB SATA DEBUG Configuration**
  Options For SATA DEBUG Configuration.
- **SB FUSION DEBUG Configuration**
  Options For SB FUSION DEBUG Configuration.
- **SB MISC DEBUG Configuration**
  Options For SB DEBUG Configuration.

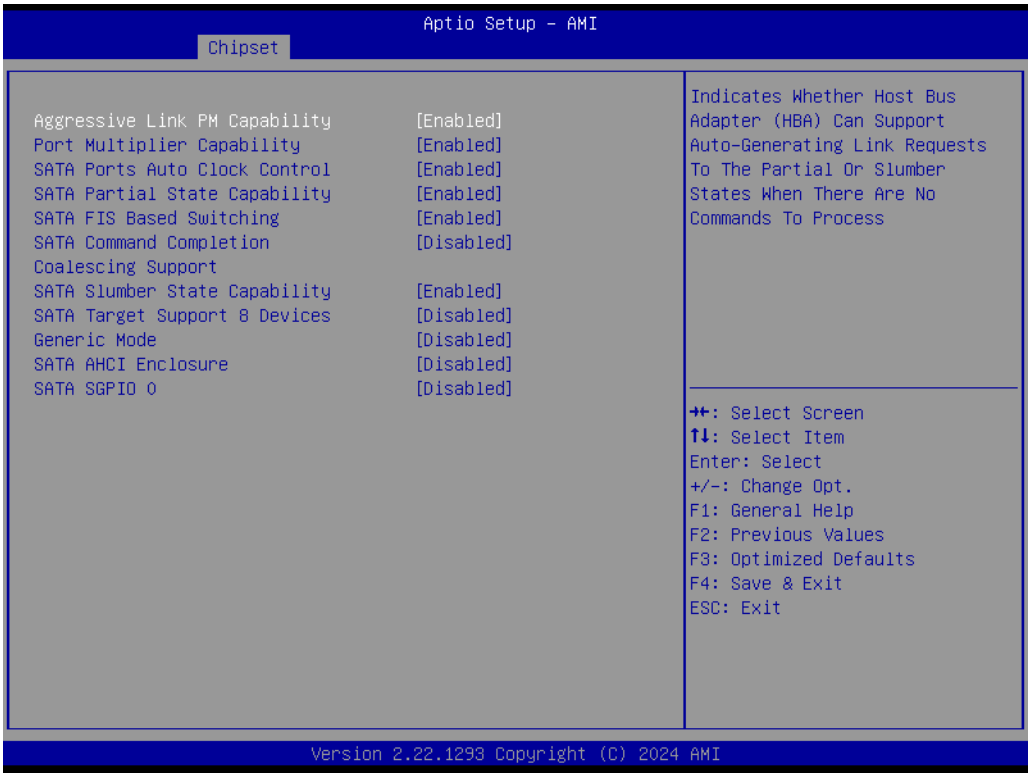


Figure 3.31 SB SATA DEBUG Configuration

- **Aggressive Link PM Capability**
  Indicates whether the Host Bus Adapter (HBA) Can Support Auto-Generating Link Requests To The Partial Or Slumber States when There Are No Commands To Process.
- **Port Multiplier Capability**
  Indicates whether the Host Bus Adapter (HBA) Can Support A Port Multiplier.
- **SATA Ports Auto Clock Control**
  Enable/Disable SATA Ports Auto Clock Control.
- **SATA Partial State Capability**
  Indicates whether the SATA Host BUS Adapter (HBA) Can Support Transitions To The Partial State.
- **SATA FIS Based Switching**
  Indicates whether the SATA Host BUS Adapter (HBA) Can Support Port Multiplier FIS-Based Switching.
- **SATA Command Completion Coalescing Support**
  Indicates whether the SATA Host BUS Adapter (HBA) Can Support Command Completion Coalescing.
- **SATA Slumber State Capability**
  Indicates whether the SATA Host BUS Adapter (HBA) Can Support Transitions To The Slumber State.
- **SATA Target Support 8 Devices**
  Indicates whether the SATA Target Support 8 Devices Functions.
- **Generic Mode**
  SATA Disable Generic Mode.
- **SATA AHCI Enclosure**
  SATA AHCI Enclosure Management.
- **SATA SGPIO 0**
  Enable/Disable SATA Serial General Purpose Input/Output (SGPIO) 0.

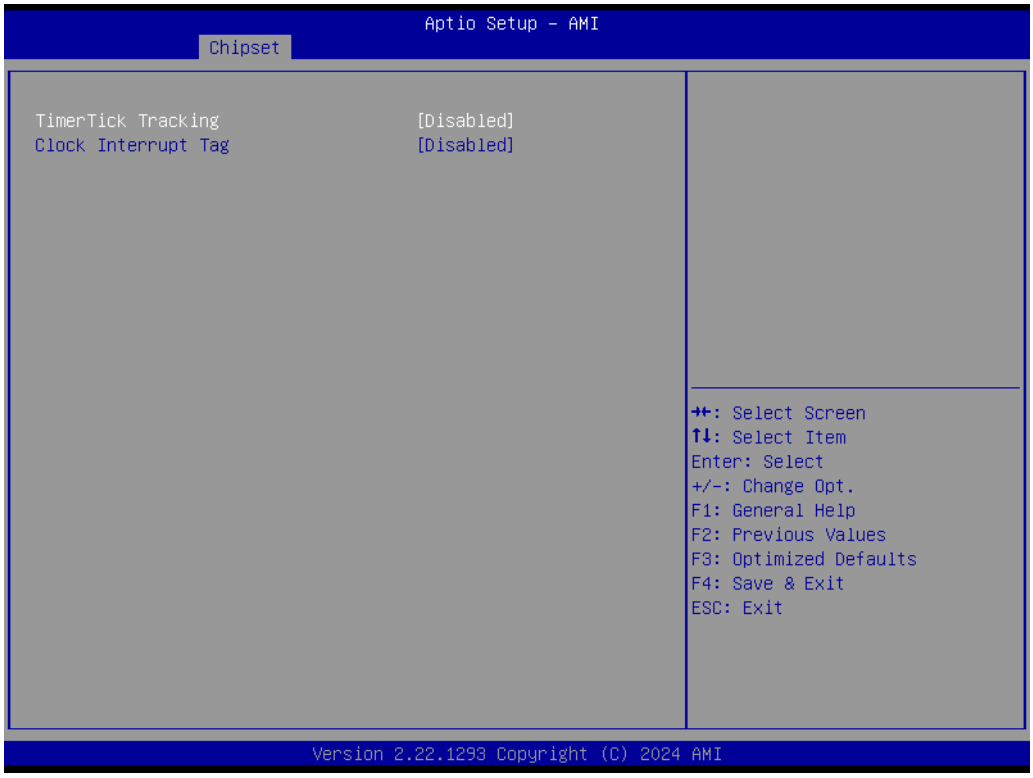


Figure 3.32 SB FUSION DEBUG Configuration

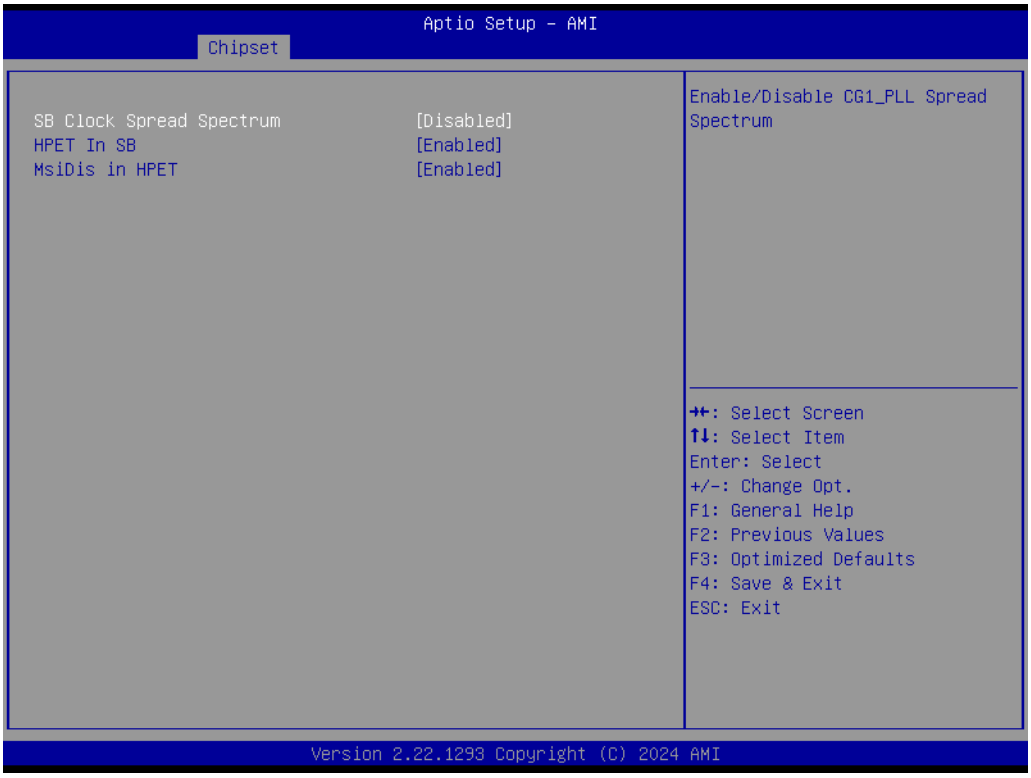


Figure 3.33 SB MISC DEBUG Configuration

- **SB Clock Spread Spectrum**
  Enable/Disable CG1_PLL Spread Spectrum.
- **HPET In SB**
  PET Function Switch.
- **MsiDis in HPET**
  Expose MSI capability in the HPET Capability register.

3.2.3.2 CRB Board

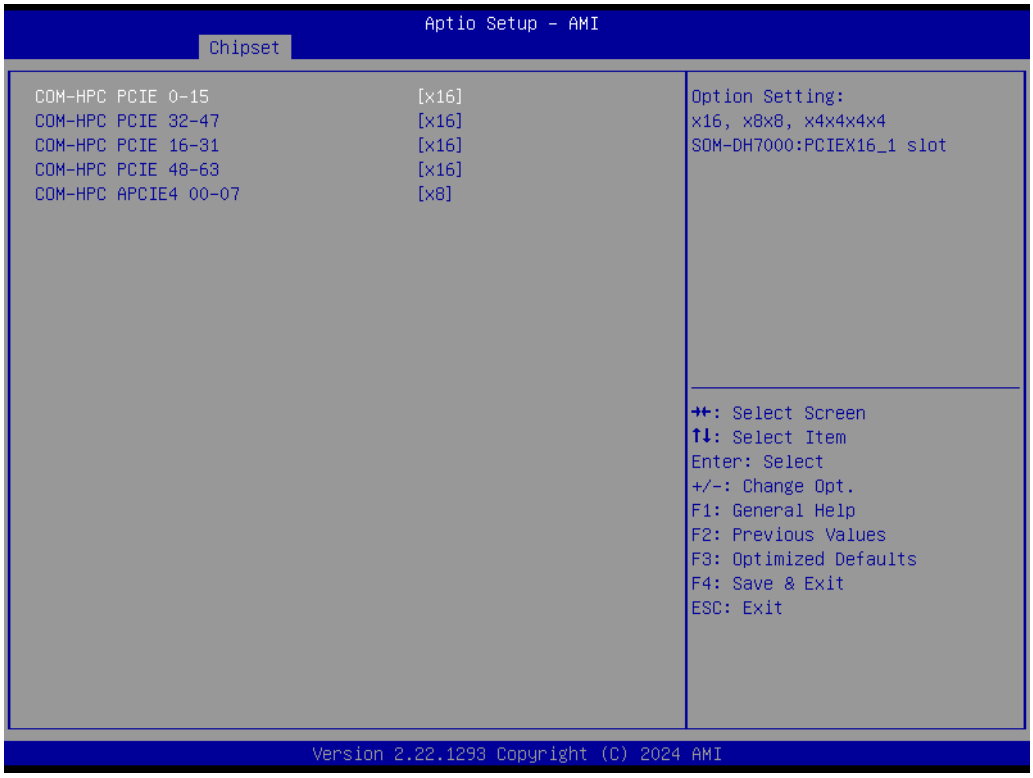


Figure 3.34 CRB Board

- **COM-HPC PCIE 0-15**
  Option Setting: x16, x8x8, x4x4x4x4
  SOM-DH7000: PCIEX16_1 slot.
- **COM-HPC PCIE 32-47**
  Option Setting: x16, x8x8, x4x4x4x4
  SOM-DH7000: PCIEX16_2 slot.
- **COM-HPC PCIE 16-31**
  Option Setting: x16, x8x8, x4x4x4x4
  SOM-DH7000: PCIEX16_3 slot
- **COM-HPC PCIE 48-63**
  Option Setting: x16, x8x8, x4x4x4x4
  SOM-DH7000: PCIEX16_4 slot.
- **COM-HPC APCIE4 00-07**
  Option Setting: x4x4
  SOM-DH7000: PCIEX8 slot.

3.2.3.3 AMD CBS

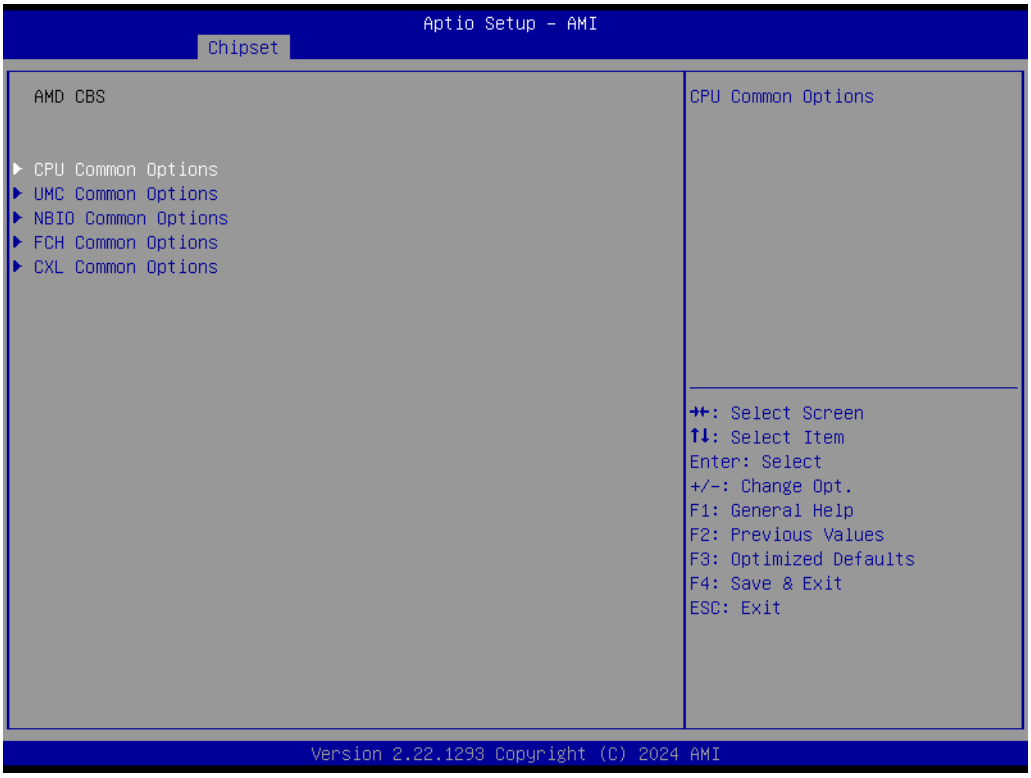


Figure 3.35 AMD CBS

- **CPU Common Options**
  CPU Common Options.
- **UMC Common Options**
  UMC Common Options.
- **NBIO Common Options**
  NBIO Common Options.
- **FCH Common Options**
  FCH Common Options.
- **CXL Common Options**
  CXL Common Options.

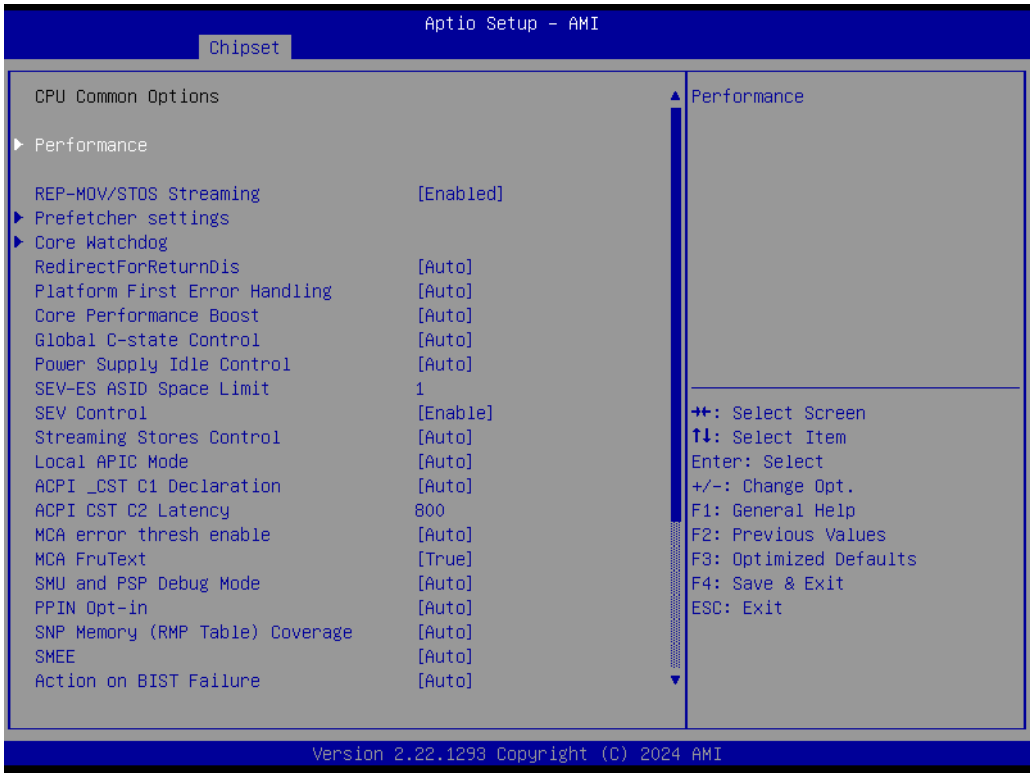


Figure 3.36 CPU Common Options

- **Performance**
  Performance.
- **REP-MOV/STOS Streaming**
  Allow REP-MOVS/STOS to use non-caching streaming stores for large sizes.
- **Prefetcher settings**
  Prefetcher settings.
- **Core Watchdog**
  Core Watchdog.
- **RedirectForReturnDis**
  From a workaround for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrctForReturns] to 1.
- **Platform First Error Handling**
  Enable/disable PFEH, cloak individual banks, and mask deferred error interrupts from each bank.
- **Core Performance Boost**
  Disable CPB.
- **Global C-state Control**
  Controls IO-based C-state generation and DF C-states.
- **Power Supply Idle Control**
  Power Supply Idle Control.
- **SEV-ES ASID Space Limit**
  Customize SEV-ES ASID space limit.
- **SEV Control**
  Can be used to disable SEV. To re-enable SEV, a POWER CYCLE is needed after selecting the ‘Enable’ option.
- **Streaming Stores Control**
  Enables or disables the streaming stores functionality.

- **Local APIC Mode**
  Select local APIC mode: Compatibility, xAPIC or x2APIC.
- **ACPI_CST C1 Declaration**
  Determines whether or not to declare the C1 state to the OS.
- **ACPI CST C2 Latency**
  Enter in microseconds (decimal value). Larger C2 latency values will reduce the number of C2 transitions and reduce C2 residency. Fewer transitions can help when performance is sensitive to the latency of C2 entry and exit. Higher residency can improve performance by allowing higher frequency boost and reduce idle core power. With Linux kernel 6.0 or later, the C2 transition cost is significantly reduced. The best value will be dependent on kernel version, use case, and workload.
- **MCA error thresh enable**
  Enable MCA error thresholding.
- **MCA FruText**
  Enable MCA FruText.
- **SMU and PSP Debug Mode**
  When this option is enabled, specific uncorrected errors detected by the PSP FW or SMU FW will hang and not reset the system.
- **PPIN Opt-in**
  Turn on the PPIN feature.
- **SNP Memory (RMP Table) Coverage**
  Enabled = ENTIRE system memory is covered.
- **SMEE**
  Control secure memory encryption enable.
- **Action on BIST Failure**
  Action to take when a CCD BIST failure is detected.
- **Fast Short REP MOVSB (FSRM)**
  Can be disabled for analysis purposes as long as the OS supports it.
- **Enhanced REP MOVSB/STOSB (ERSM)**
  Default is 1, and can be set to zero for analysis purpose as long as the OS supports it.
- **Log Transparent Errors**
  Log transparent errors in MCA in addition to debug registers.
- **AVX512**
  Enable/Disable AVX512.
- **MONITOR and MWAIT disable**
  The MONITOR, MWAIT, MONITORX, and MWAITX opcodes become invalid, when Enabled.
- **Small Hammer Configuration**
  Enabled:
  LS_CFG:: DisSpecWReq=0
  LS_CFG3:: DisSpecWcNonStrmLd=1
  LS_CFG3:: EnLockNeedProgressForSpecNC=1
  Disabled:
  LS_CFG:: DisSpecWcReq=0
  LS_CFG3:: DisSpecWcNonStrmLd=0
  LS_CFG3:: EnLockNeedProgressForSpecNC=0
- **Corrector Branch Predictor**
  Enabling for branch heavy codes may reduce conditional branch mispredicts.
- **PAUSE Delay**
  Number a cycle thread will be idle after a PAUSE instruction.

- **CPU Speculative Store Modes**
  Balanced:
  Store instructions may delay sending out their invalidations to remote cacheline copies when the cacheline is present but not in a writable state in the local cache. More Speculative:
  Store instructions will send out invalidations to remote cacheline copies as soon as possible.
  Less Speculative:
  Store instructions may delay sending our their invalidations to remote cacheline copies when the cacheline is not present in the local cache or not in a writable state in the local cache.
- **Prefetch/Request Throttle**
  Enable XI logic which calculates average latency, updates throttle level, and sends throttle level messages to L2.

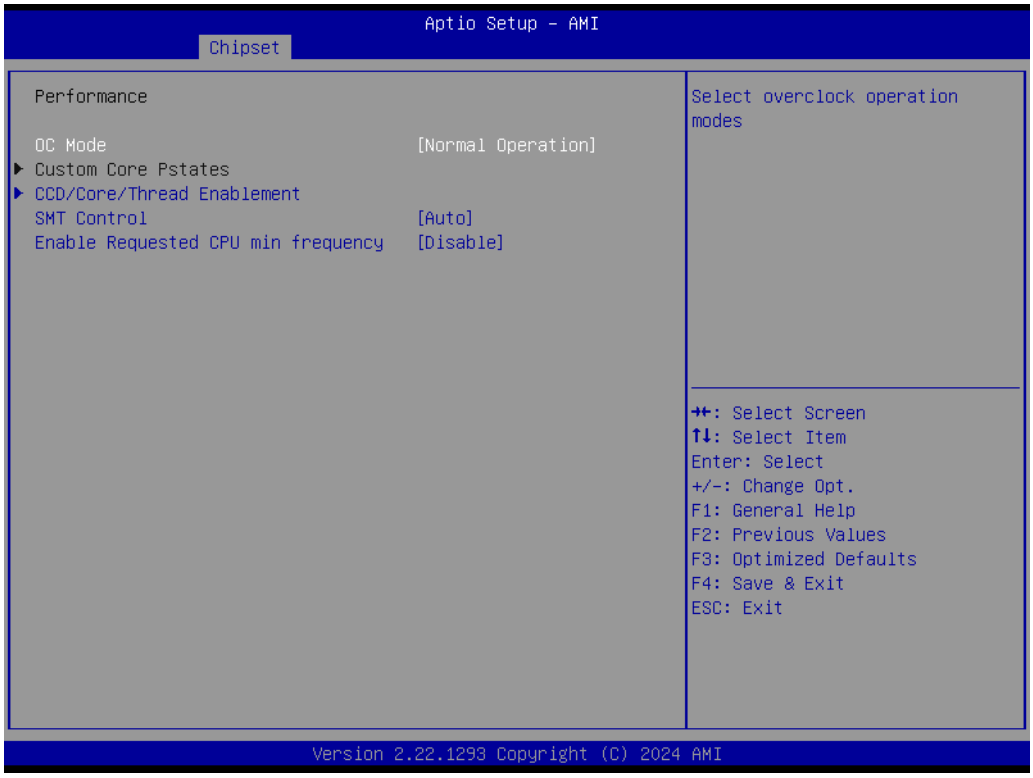


Figure 3.37 Performance

- **OC Mode**
  Select overclock operation modes.
- **CCD/Core/Thread Enablement**
  CCD/Core/Thread Enablement.
- **SMT Control**
  Can be used to disable symmetric multi-threading. To re-enable SMT, a POWER CYCLE is needed after selecting the ‘Enable’ option.Select ‘Auto’ base on BIOS PCD(PcdAmdSmtMode) default setting. WARNING-S3 is NOT SUPPORTED on systems where SMT is disabled.
- **Enable Requested CPU min frequency**
  This allows for minimum requested CPU frequency to be used.

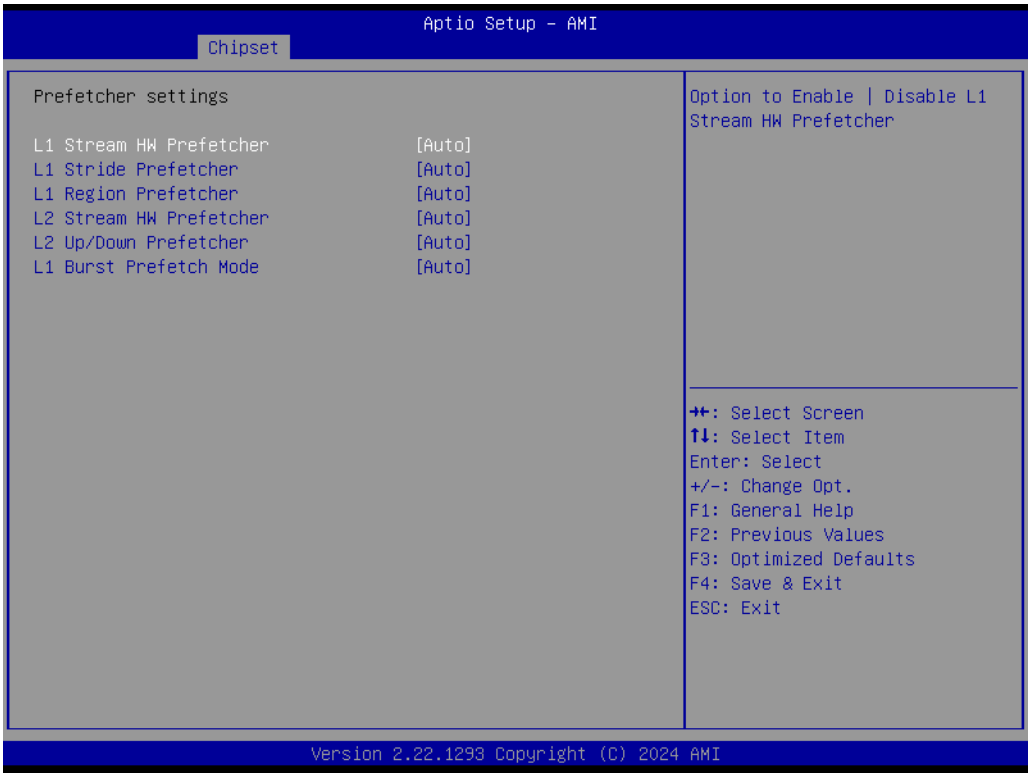


Figure 3.38 Prefetcher Settings

- **L1 Stream HW Prefetcher**
  Options to Enable | Disable L1 Stream HW Prefetcher.
- **L1 Stride Prefetcher**
  Uses memory access history of individual instructions to fetch additional lines when each access is a constant distance from the previous.
- **L1 Region Prefetcher**
  Uses memory access history to fetch additional lines when the data access for a given instruction tends to be followed by other data accesses.
- **L2 Stream HW Prefetcher**
  Option to Enable | Disable L2 Stream HW Prefetcher.
- **L2 Up/Down Prefetcher**
  Uses memory access history to determine whether to fetch the next or previous line for all memory accesses.
- **L1 Burst Prefetch Mode**
  Option to Enable | Disable L1 Burst Prefetch Mode.

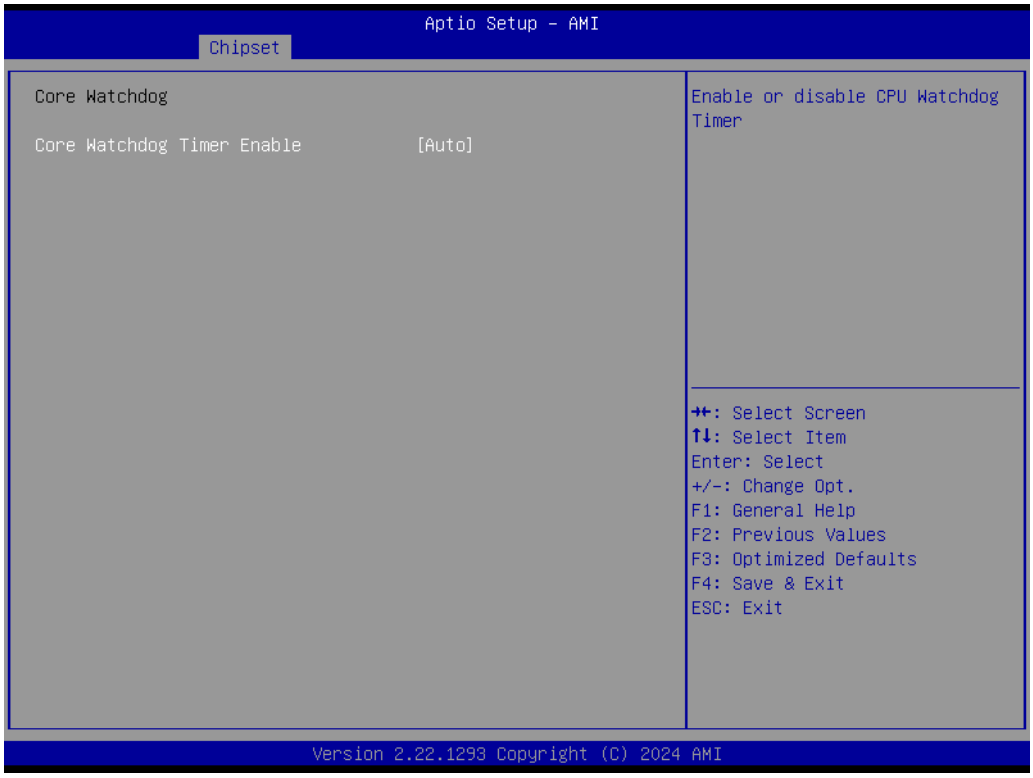


Figure 3.39 Core Watchdog

- **Core Watchdog Timer Enable**
  Enable or disable the CPU watchdog Timer.

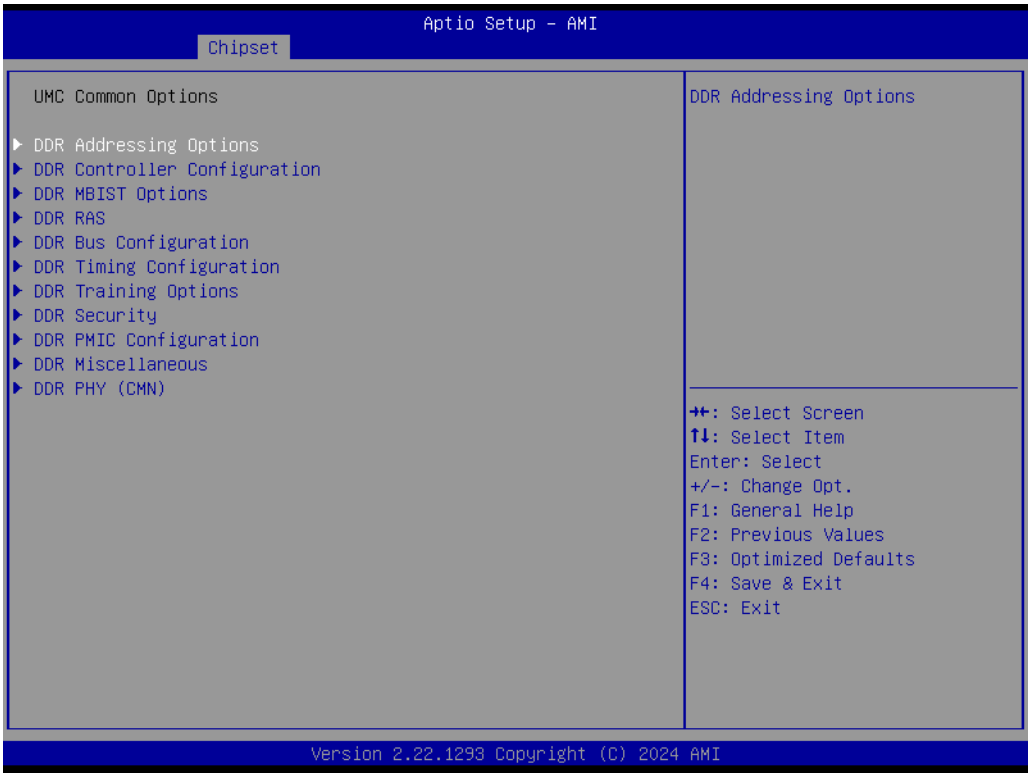


Figure 3.40 UMC Common Options

- **DDR Addressing Options**
  DDR Addressing Options.
- **DDR Controller Configuration**
  DDR Controller Configuration.
- **DDR MBIST Options**
  DDR MBIST Options.
- **DDR RAS**
  DDR RAS.
- **DDR Bus Configuration**
  DDR Bus Configuration.
- **DDR Timing Configuration**
  DDR Timing Configuration.
- **DDR Training Options**
  DDR Training Options.
- **DDR Security**
  DDR Security.
- **DDR PMIC Configuration**
  DDR PMIC Configuration.
- **DDR Miscellaneous**
  DDR Miscellaneous.
- **DDR PHY (CMN)**
  DDR PHY (CMN).

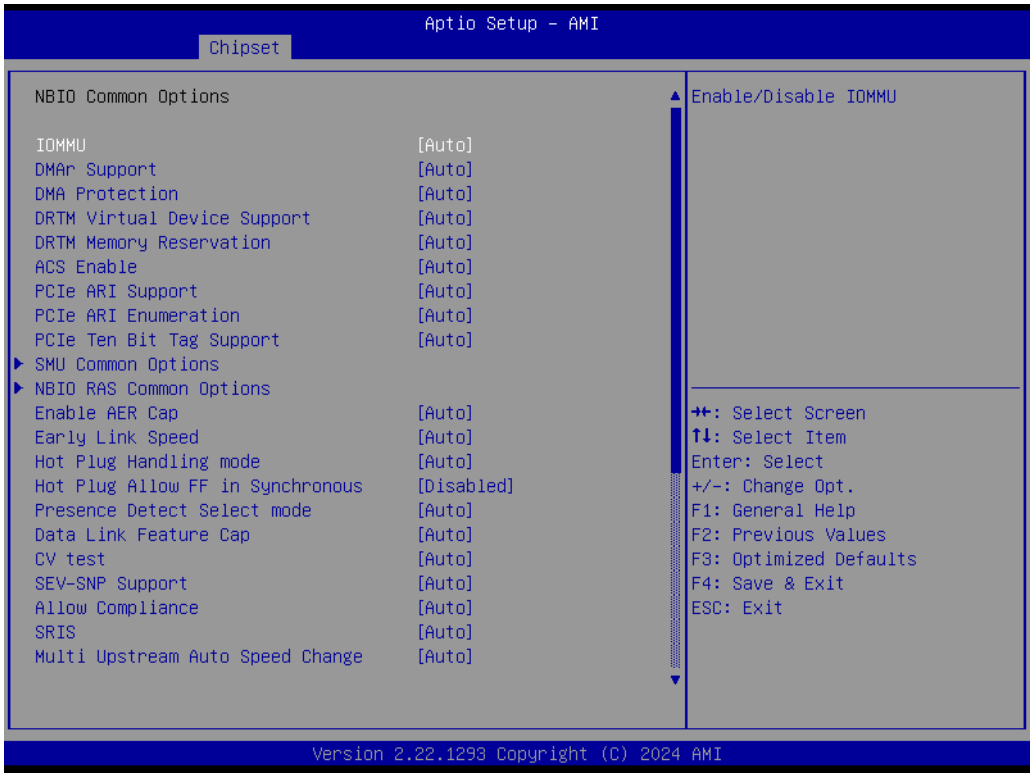


Figure 3.41 NBIO Common Options

- **IOMMU**
  Enable/Disable IOMMU.
- **DMAr Support**
  Enable DMAr system protection during POST.
- **DMA Protection**
  Enable DMA remap support in IVRS IVinfo Field.
- **DRTM Virtual Device Support**
  Enable DRTM ACPI virtual device.
- **DRTM Memory Reservation**
  Reserve 128MB memory below Bottom IO for DRTM. It is required to be enabled for Secured-Core Server function.
- **ACS Enable**
  AER must be enabled for ACS enable to work.
- **PCIe ARI Support**
  Enables Alternative Routing-ID Interpretation.
- **PCIe ARI Enumeration**
  ARI Forwarding Enable for each downstream port.
- **PCIe Ten Bit Tag Support**
  Enables PCIe ten bit tags for supported devices.
- **SMU Common Options**
  SMU Common Options.
- **NBIO RAS Common Options**
  NBIO RAS Common Options.
- **Enable AER Cap**
  Enables Advanced Error Reporting Capability.
- **Early Link Speed**
  Early Link Speed.

- **Hot Plug Handling mode**
  Control the Hot Plug Handling mode.
  Note: 'Firmware First but allow OS First' is a development mode and not to be used until operating systems with this support are available. SFI mode REQUIRES an operating system that supports DPC. (Most recent Linux operating system support/enable this).
- **Hot Plug Allow FF in Synchronous**
  Allows firmware first hot plug handling mode to operate in mode A and mode B synchronous mappings.
- **Presence Detect Select mode**
  Control the Presence Detect Select mode.
- **Data Link Feature Cap**
  Data Link Feature Capability.
- **CV test**
  Set this to Enabled to support running PCIECV tool. Auto – preserve h/w defaults.
- **SEV-SNP Support**
  Enables support for Secure Encrypted Virtualization and Secure Nested Paging.
- **Allow Compliance**
  When enabled, allows the PCIe RP to enter Polling. Compliance state.
- **SRIS**
  SRIS
- **Multi Upstream Auto Speed Change**
  Defines the setting of this feature for all PCIe devices. 'Auto' uses the DXIO default setting of 0 for Gen1 and 1 for Gen2/3.
- **Multi Auto Speed Change On Last Rate**
  Force PCIe link training speed to last advertised for all ports. Disabled=Use highest data rate ever advertised. Enabled=Use last data rate advertised.
- **PCIE Link Speed Capability**
  Set all PCIe port speed capability.
- **RTM Margining Support**
  RTM Margining Support.
- **EQ Bypass To Highest Rate**
  Controls the ability to advertise Equalization Bypass to Highest Rate Support in TSxs sent prior to LinkUp=1.
- **Non-PCIe Compliant Support**
  Enable this setting to send command to disable Extended EIEOS, DLF, and Gen5 Support on training failure for non-pcie compliant devices.
- **PCIE Idle Power Setting**
  Modify PCIE Power Savings Feature that Can Impact Lightly Loaded Latency.
- **nBif Common Options**
  nBif Common Options.
- **Link EQ Preset Options**
  Link EQ Preset Options.
- **Enable 2 SPC (Gen4)**
  Enable this setting to use 2 symbols per clock for devices at Gen 4 speed.
- **Safe recovery upon a BERExceeded Error**
  No help string.
- **Periodic Calibration**
  No help string.
- **Enable PCIe SFI Config via OOB**
  Enable PCIe SFI Config via OOB support.

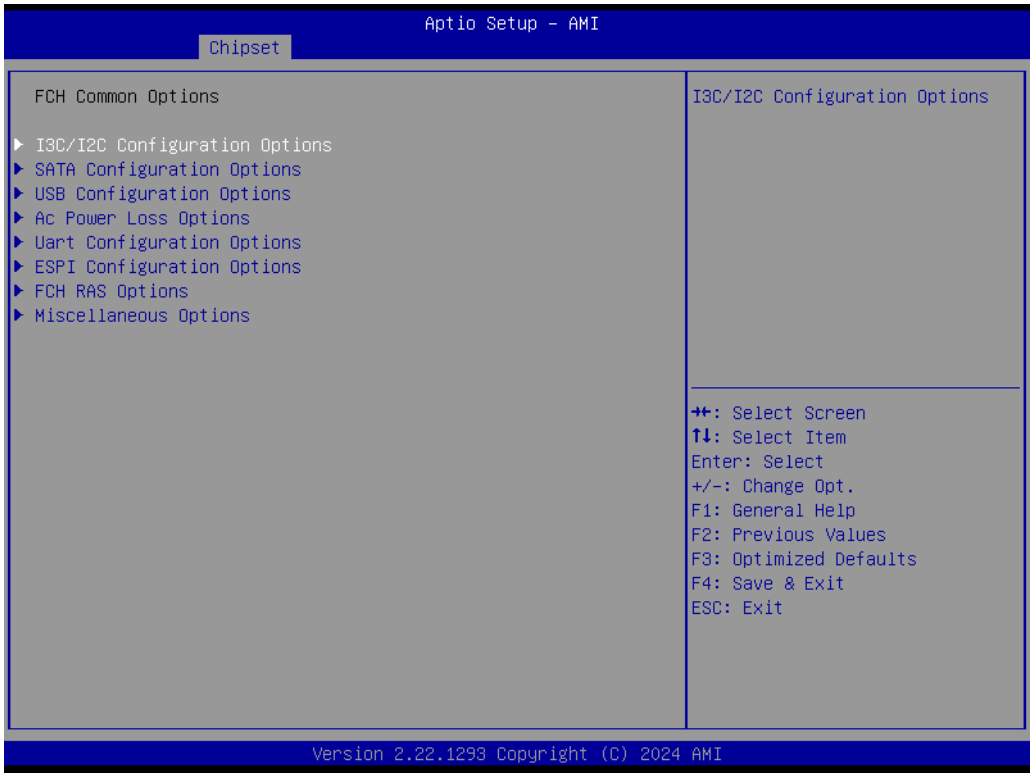


Figure 3.42 FCH Common Options

- **I3C/I2C Configuration Options**
  I3C/I2C Configuration Options
- **SATA Configuration Options.**
  SATA Configuration Options.
- **USB Configuration Options.**
  USB Configuration Options.
- **Ac Power Loss Options**
  Ac Power Loss Options.
- **Uart Configuration Options**
  Uart Configuration Options.
- **ESPI Configuration Options**
  ESPI Configuration Options.
- **FCH RAS Options**
  FCH RAS Options.
- **Miscellaneous Options**
  Miscellaneous Options.

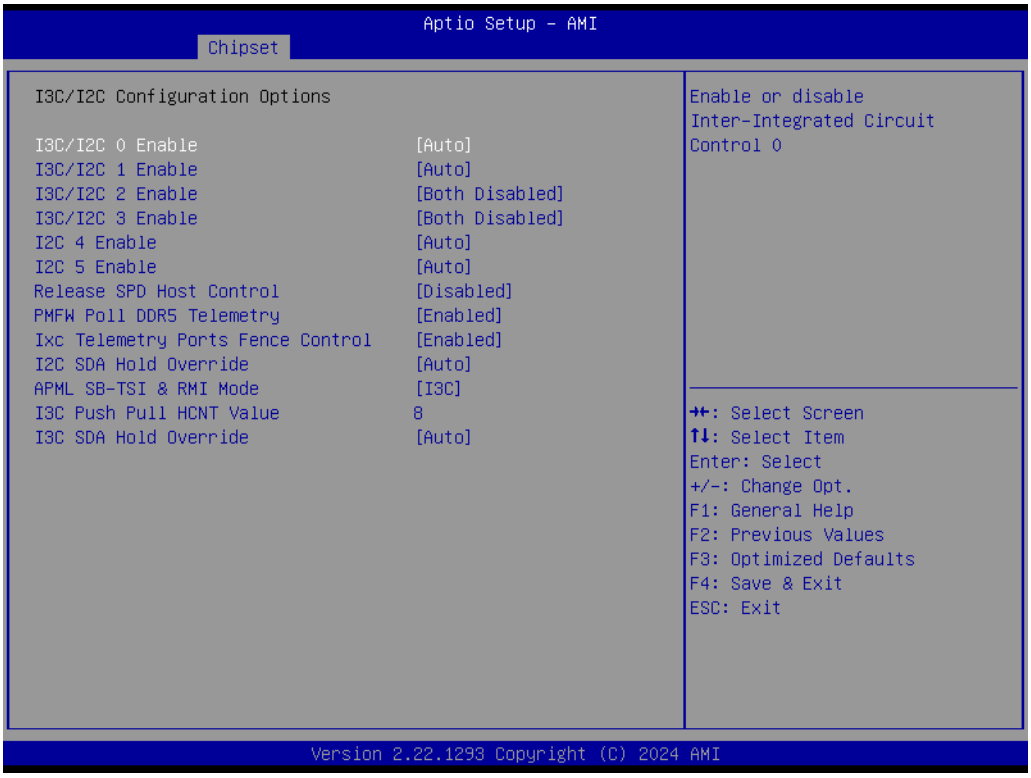


Figure 3.43 I3C/I2C Configuration Options

- **I3C/I2C 0 Enable**
  Enable or disable Inter-Integrated Circuit Control 0.
- **I3C/I2C 1 Enable**
  Enable or disable Inter-Integrated Circuit Control 1.
- **I3C/I2C 2 Enable**
  Enable or disable Inter-Integrated Circuit Control 2.
- **I3C/I2C 3 Enable**
  Enable or disable Inter-Integrated Circuit Control 3.
- **I2C 4 Enable**
  Enable or disable Inter-Integrated Circuit Controller4.
- **I2C 5 Enable**
  Enable or disable Inter-Integrated Circuit Controller5.
- **Release SPD Host Control**
  Release SPD Host Control, so that BMC can take over the ownership of I2C/I3C bus.
- **PMFW Poll DDR5 Telemetry**
  Send message to PMFW for polling DDR5 telemetry at the end of POST.
- **Ixc Telemetry Ports Fence Control**
  Controls the Fencing off for I2C/I3C ports which are involved in DDR Telemetry. If this option is enabled, then the associated Ixc ports registers will be put in the secure region.
  Note: If this option is disabled, there is a risk of collision happening between x86 accessing IxC and PMFW running DDR Telemetry which can cause undefined behavior.
- **I2C SDA Hold Override**
  Override I2C SDA_TX_HOLD and SDA_RX_HOLD.

- **APML SB-TSI & RMI Mode**
  Select APML_SB-TSI over I3C or I2C. In I3C mode, the secondary controller can support both I3C and I2C (Adaptive mode).
- **I3C Push Pull HCNT Value**
  SCL push-pull High count for I3C transfers targeted to I3C devices.
- **I3C SDA Hold Override**
  Override I3C SDA HOLD VALUE.

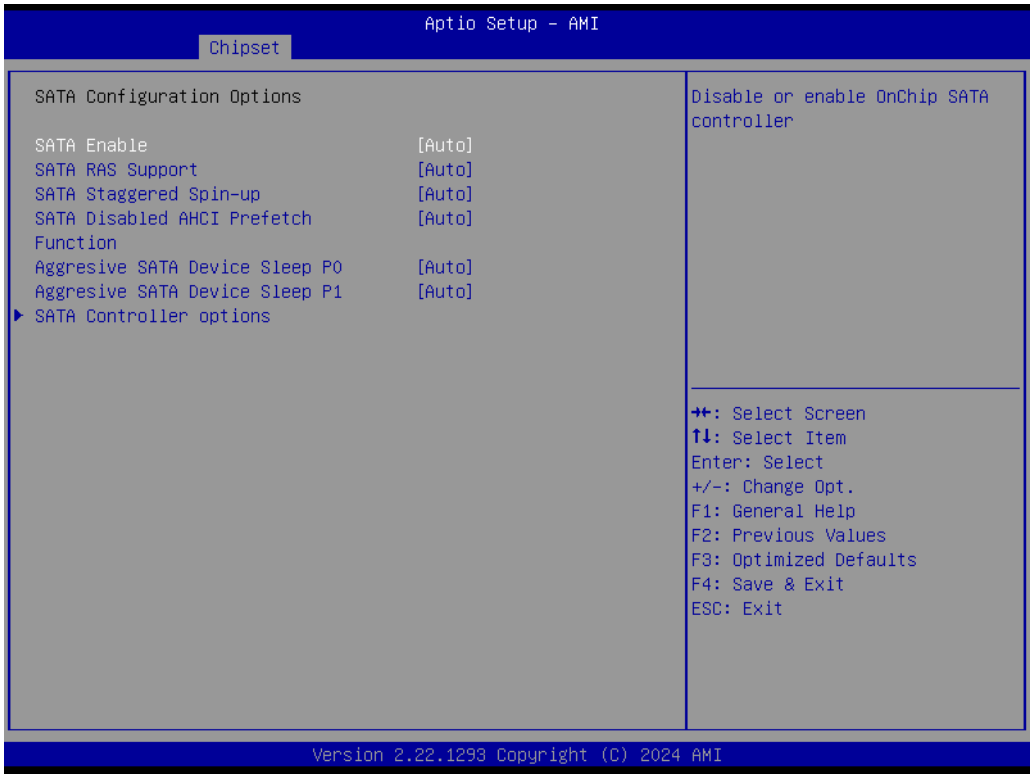


Figure 3.44 SATA Configuration Options

- **SATA Enable**
  Disable or enable OnChip SATA controller.
- **SATA RAS Support**
  Disable or enable Sata RAS Support.
- **SATA Staggered Spin-up**
  Enable or disable SATA staggered spin-up.
- **SATA Disabled AHCI Prefetch Function**
  Disable or enable Sata Disabled AHCI Prefetch Function.
- **Aggressive SATA Device Sleep Port 0**
  Enable or disable aggressive SATA device sleep on port 0.
- **Aggressive SATA Device Sleep Port 1**
  Enable or disable aggressive SATA device sleep on port 1.
- **SATA Controller options**
  SATA Controller options.

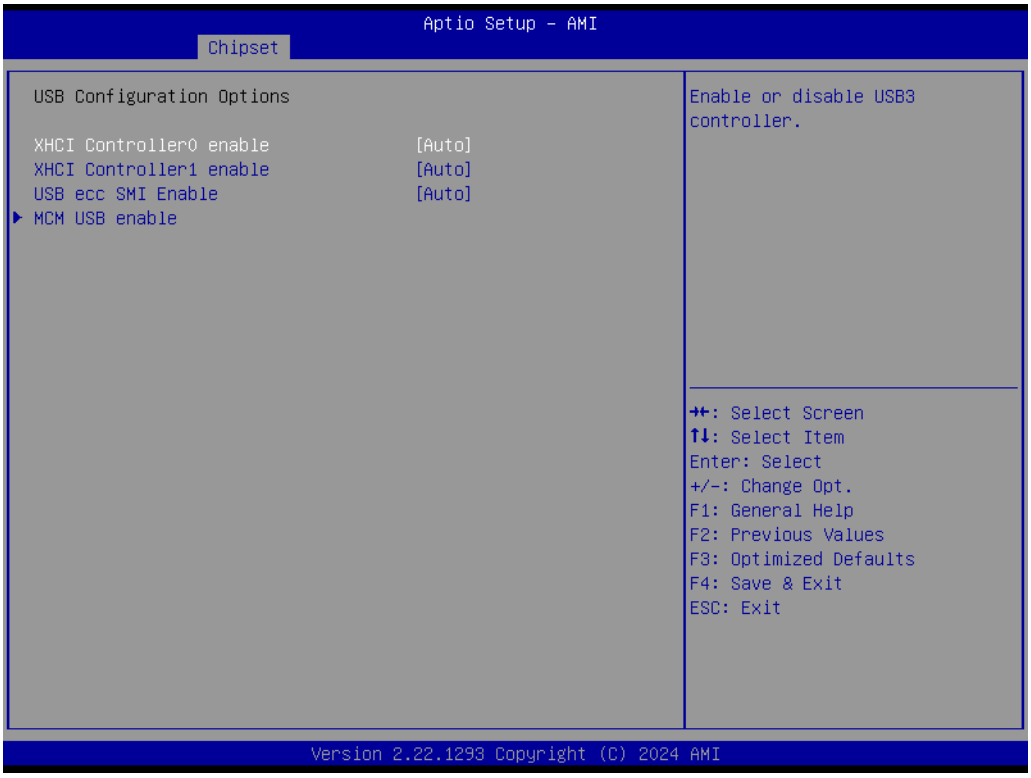


Figure 3.45 USB Configuration Options

- **XHCI Controller0 enable**
  Enable or disable USB3 controller.
- **XHCI Controller1 enable**
  Enable or disable USB3 controller.
- **USB ecc SMI Enable**
  Enable or disable USB ecc SMI.
- **MCM USB enable**
  MCM USB enable.

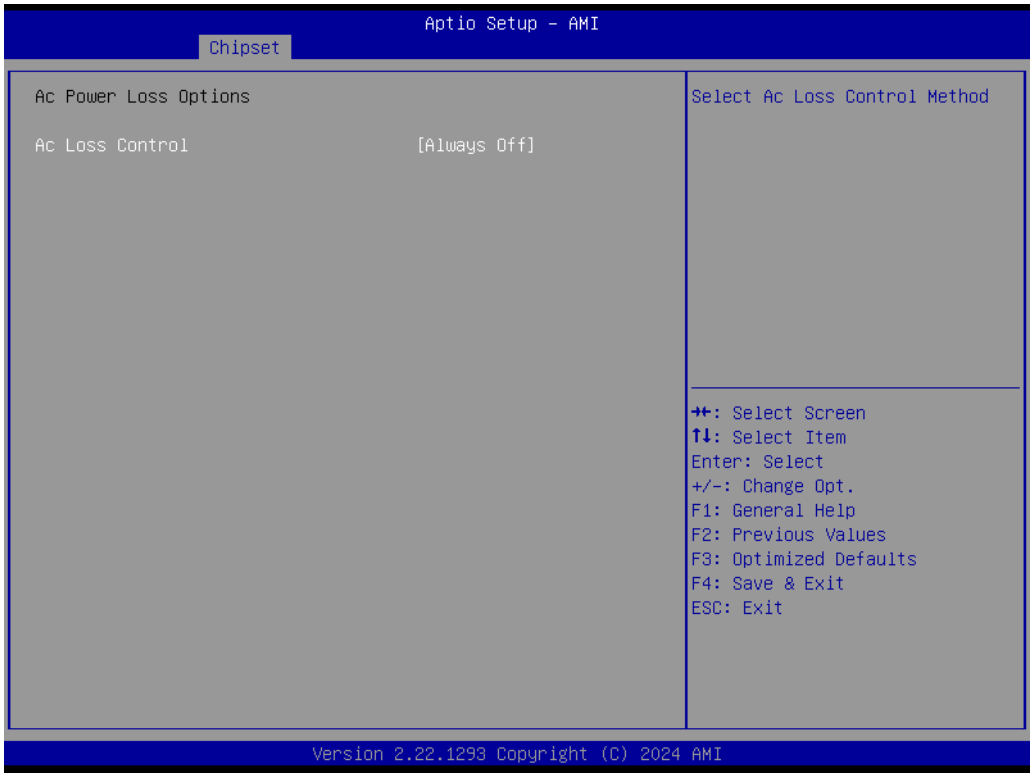


Figure 3.46 Ac Power Loss Options

- **Ac Loss Control**
  Select Ac Loss Control Method.

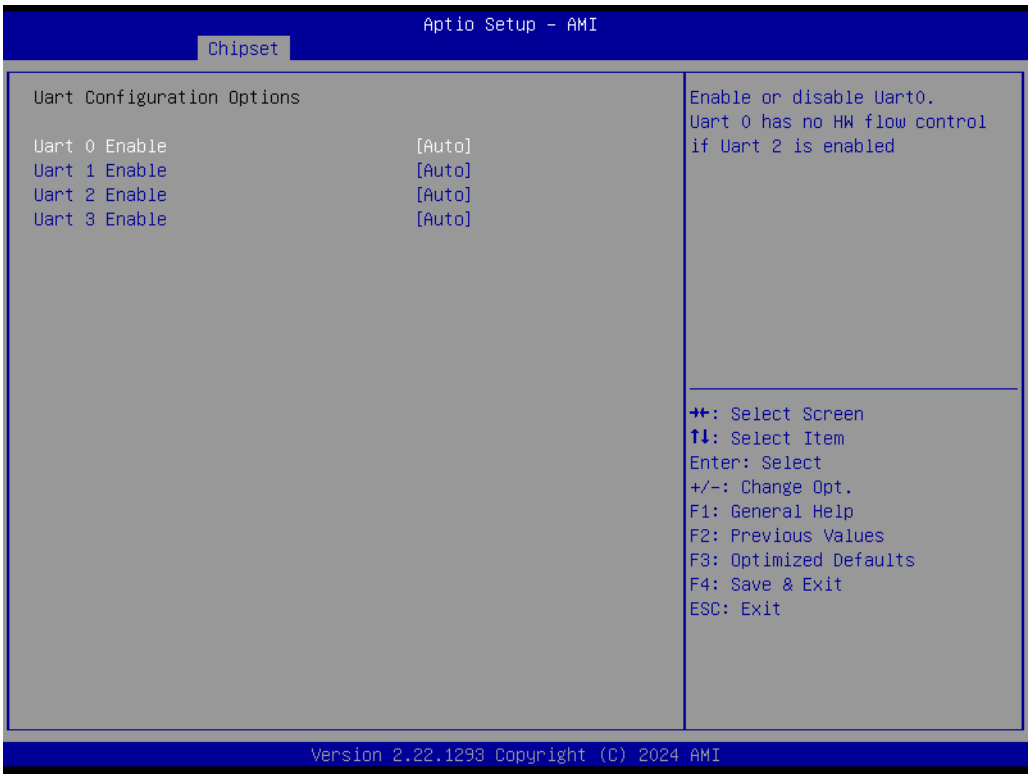


Figure 3.47 Uart Configuration Options

- **Uart 0 Enable**
  Enable or disable Uart0.
  Uart 0 has no HW flow control if Uart 2 is enabled.
- **Uart 1 Enable**
  Enable or disable Uart1.
- **Uart 2 Enable (no HW FC)**
  Enable or disable Uart2. If Uart 2 is enable, Uart0 has no HW flow control.
- **Uart 3 Enable (no HW FC)**
  Enable or disable Uart3.

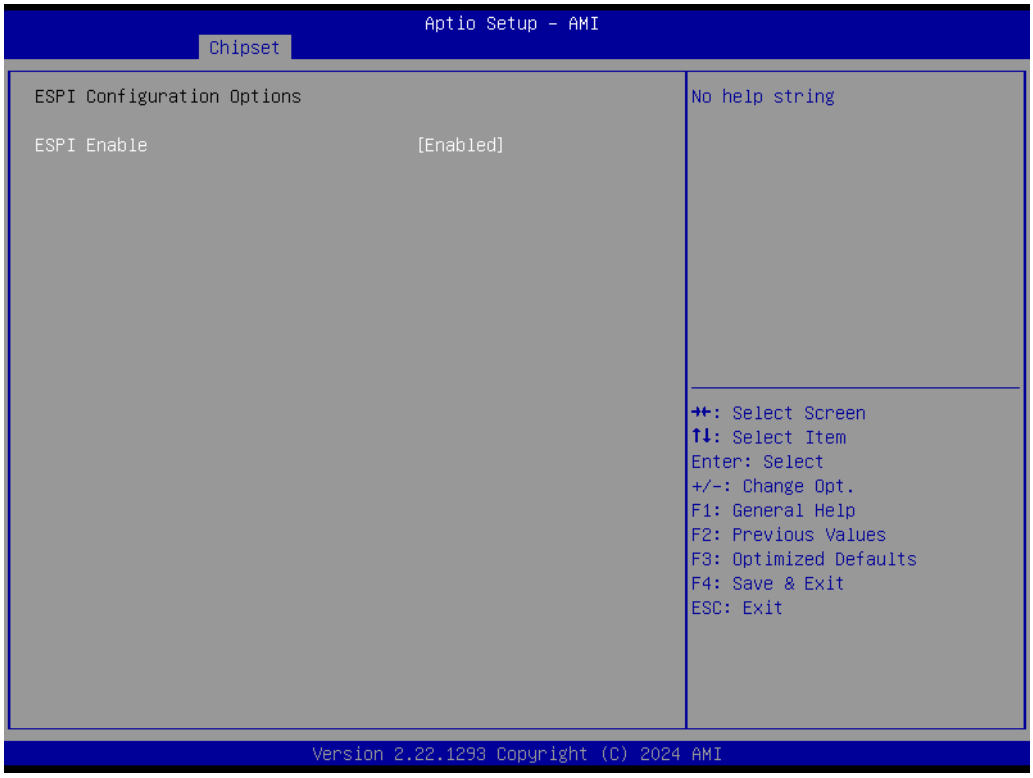


Figure 3.48 ESPI Configuration Options

- **ESPI Enable**
  No help string.

Figure 3.49 FCH RAS Options

- **ALink RAS Support**
  Enable FCH A-Link parity error.
- **Reset After Sync-Flood**
  Enable AB to forward downstream sync-flood message to system controller.

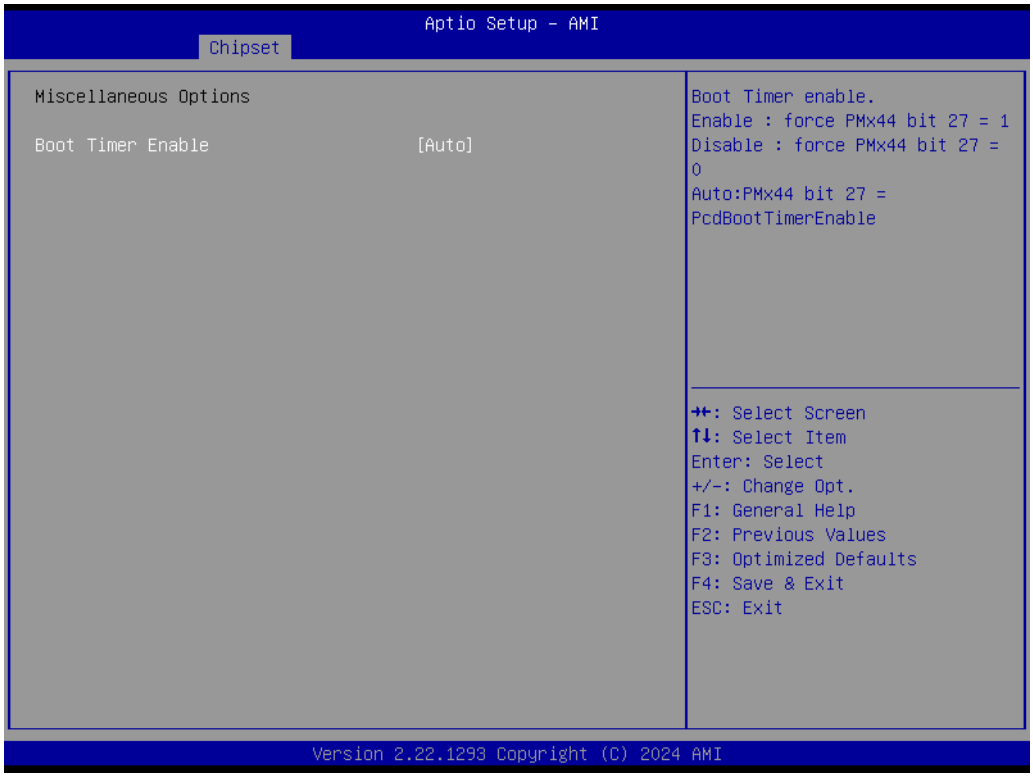


Figure 3.50 Miscellaneous Options

- **Boot Timer Enable**
  Boot Timer enable.
  Enable: force PMx44 bit 27 = 1 Disable: force PMx44 bit 27 = 0.
  Auto: PMx44 bit 27 = PcdBootTimerEnable.

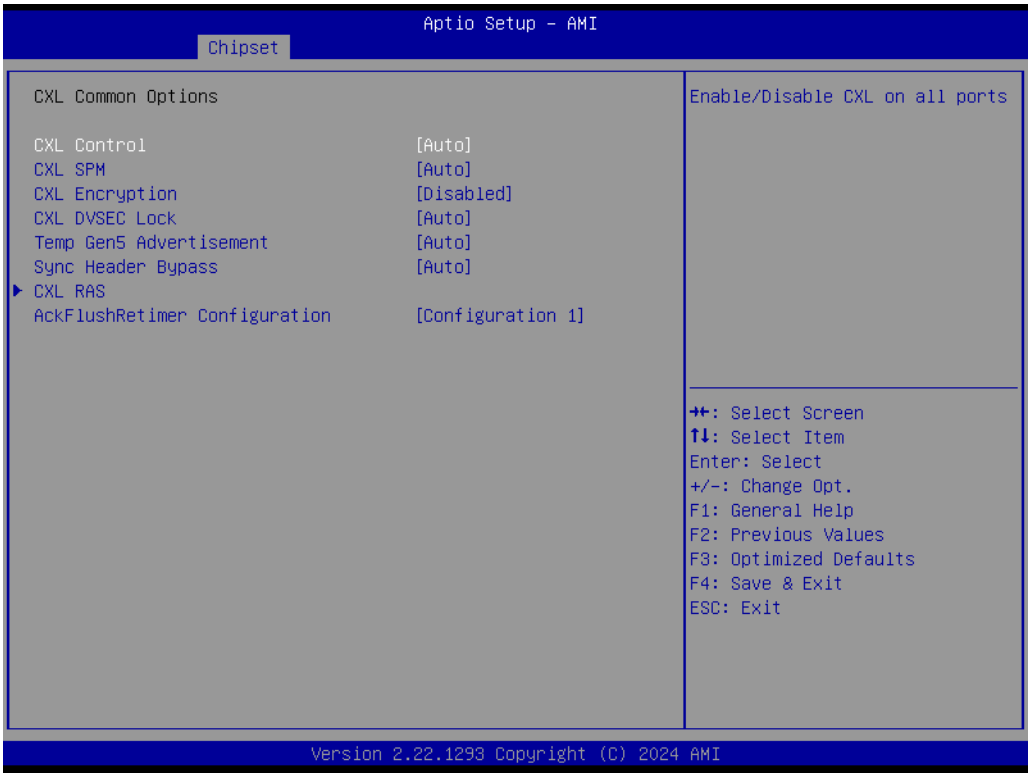


Figure 3.51 CXL Common Options

- **CXL Control**
  Enable/Disable CXL on all ports.
- **CXL SPM**
  Sets CXL memory as Special Purpose Memory.
- **CXL Encryption**
  CXL Encryption.
- **CXL DVSEC Lock**
  Locks the CXL DVSEC.
- **Temp Gen5 Advertisement**
  Temp Gen5 Advertisement for Alternative Protocol.
- **Sync Header Bypass**
  Enable/Disable CXL Sync Header Bypass support.
- **CXL RAS**
  CXL RAS.
- **AckFlushRetimer Configuration**
  Configure the AckFlushRetimer register to revert it back to the old value as backup Configuration 1 will have the register as default value 0x380?Configuration 2 will revert it back to old value 0x100.

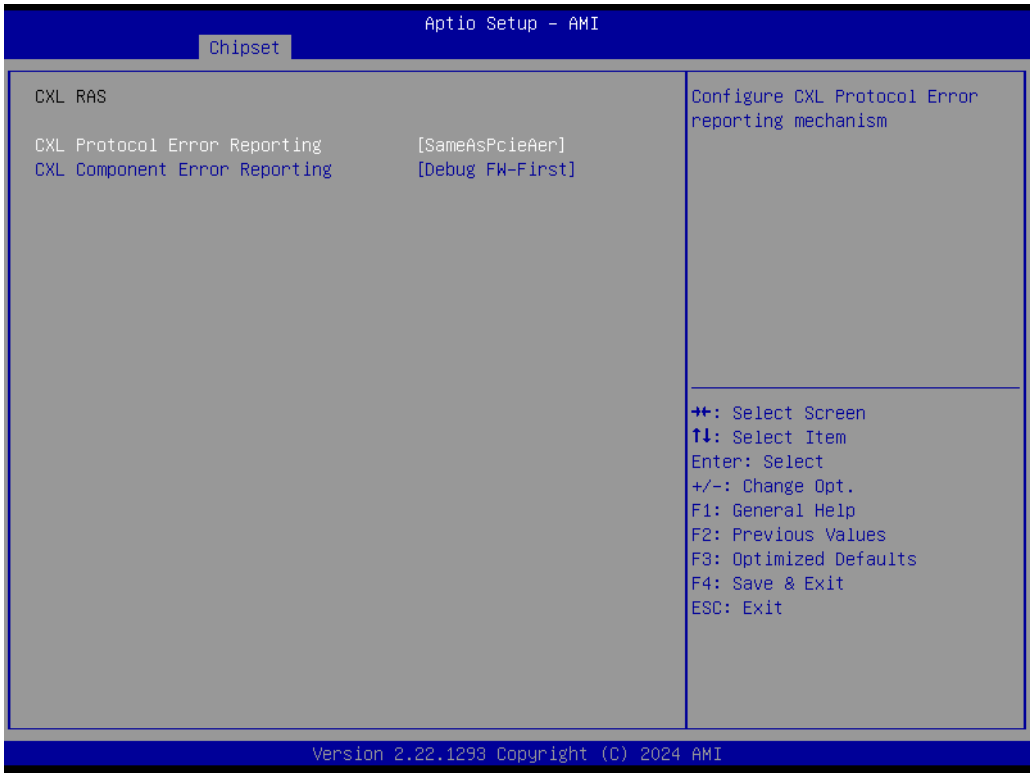


Figure 3.52 CXL RAS

- **CXL Protocol Error Reporting**
  Configure CXL Protocol Error reporting mechanism.
- **CXL Component Error Reporting**
  Configure CXL Component Error reporting mechanism.

3.2.3.4 AMD PBS

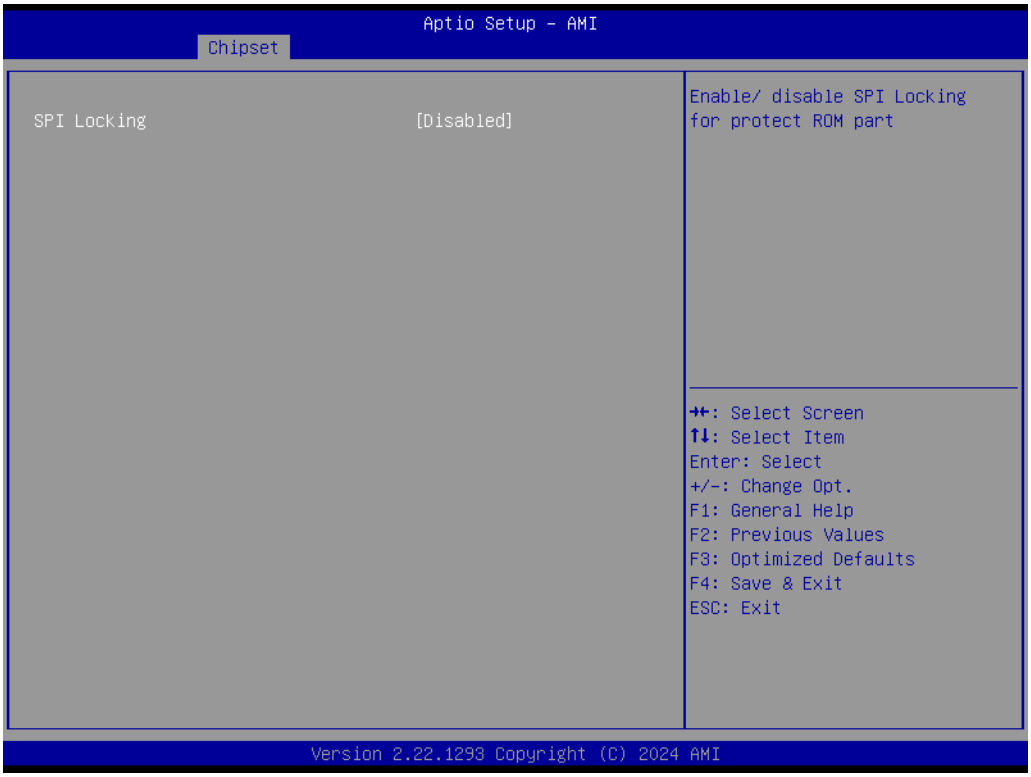


Figure 3.53 SPI Locking

- **SPI Locking**
  Enable/disable SPI Locking for protect ROM part.

3.2.3.5 North Bridge

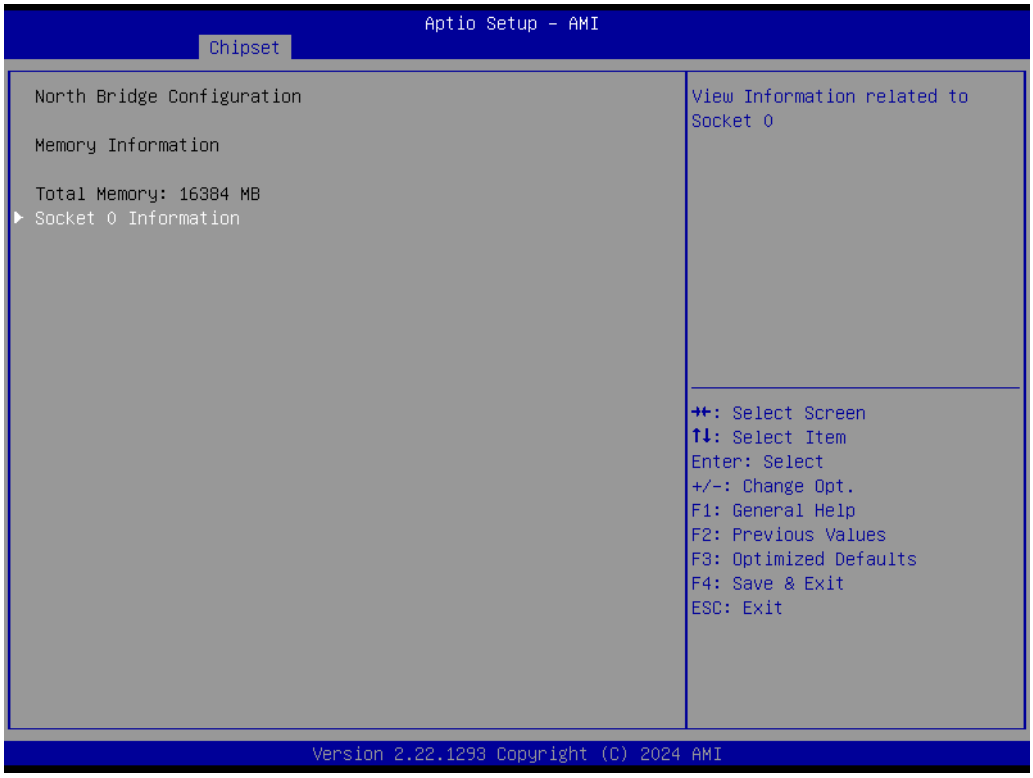


Figure 3.54 North Bridge

- **Socket 0 Information**
  View Information related to Socket 0.

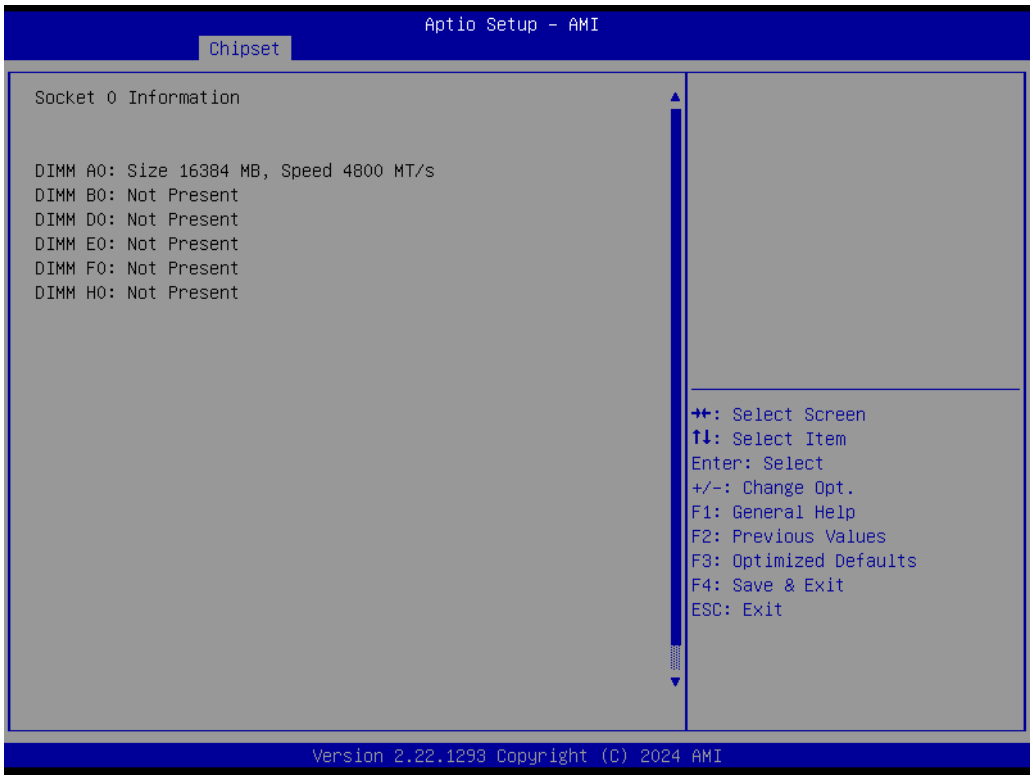


Figure 3.55 Socket 0 Information

3.2.4 Security Chipset

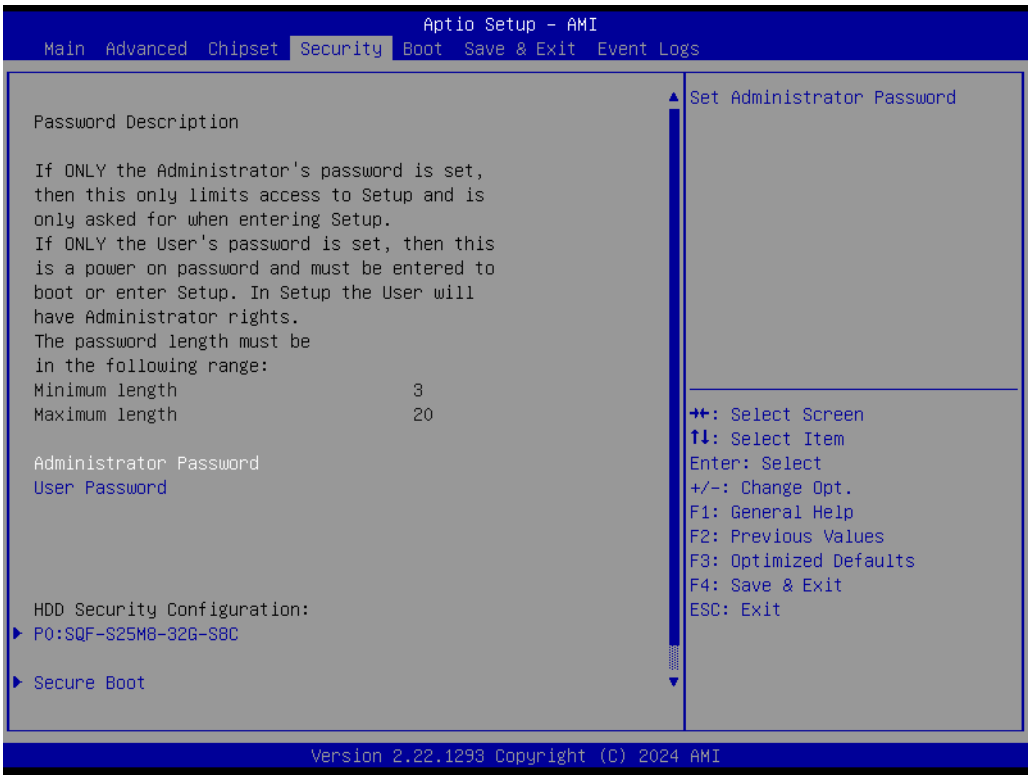


Figure 3.56 Security

- **Administrator Password**
  Set Administrator Password.
- **User Password**
  Set User Password.
- **P0: SQF-S25V2-256GCSBC**
  HDD Security Configuration for selected drive.
- **Secure Boot**
  Secure Boot configuration.

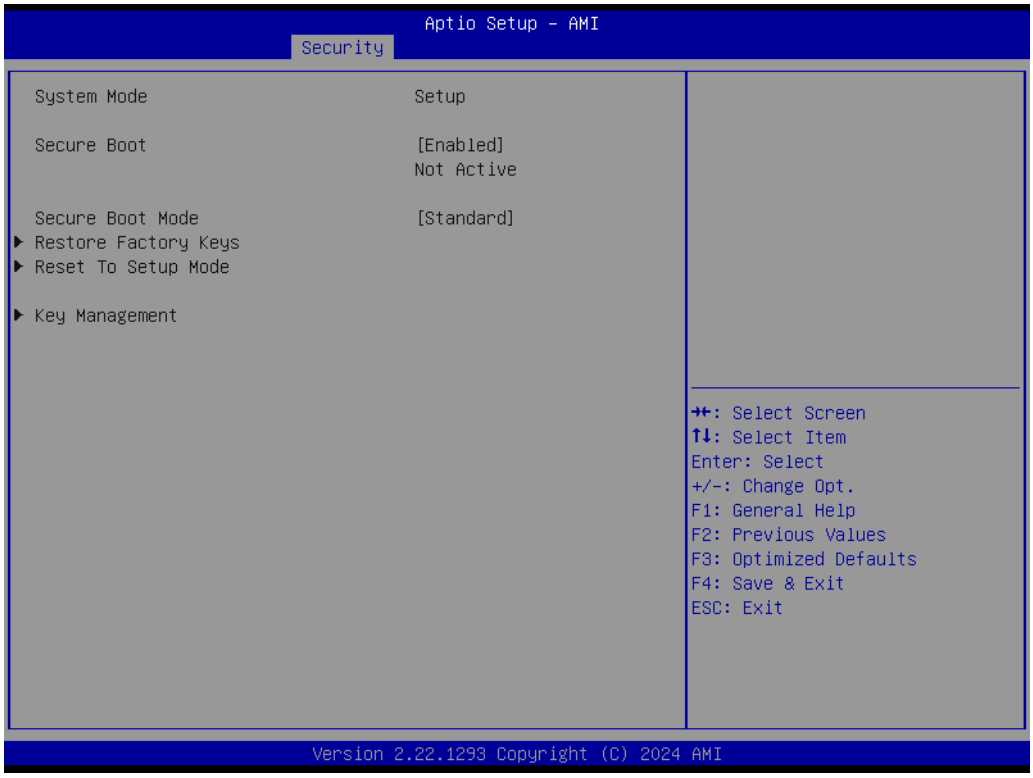


Figure 3.57 Secure Boot

- **Secure Boot**
  Secure Boot feature is Active if Secure Boot is Enabled. Platform Key (PK) is enrolled and the System is in User mode. The mode change requires a platform reset.
- **Secure Boot Mode**
  Secure Boot mode options:
  Standard or Custom.
  In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.

3.2.5 Boot Setup

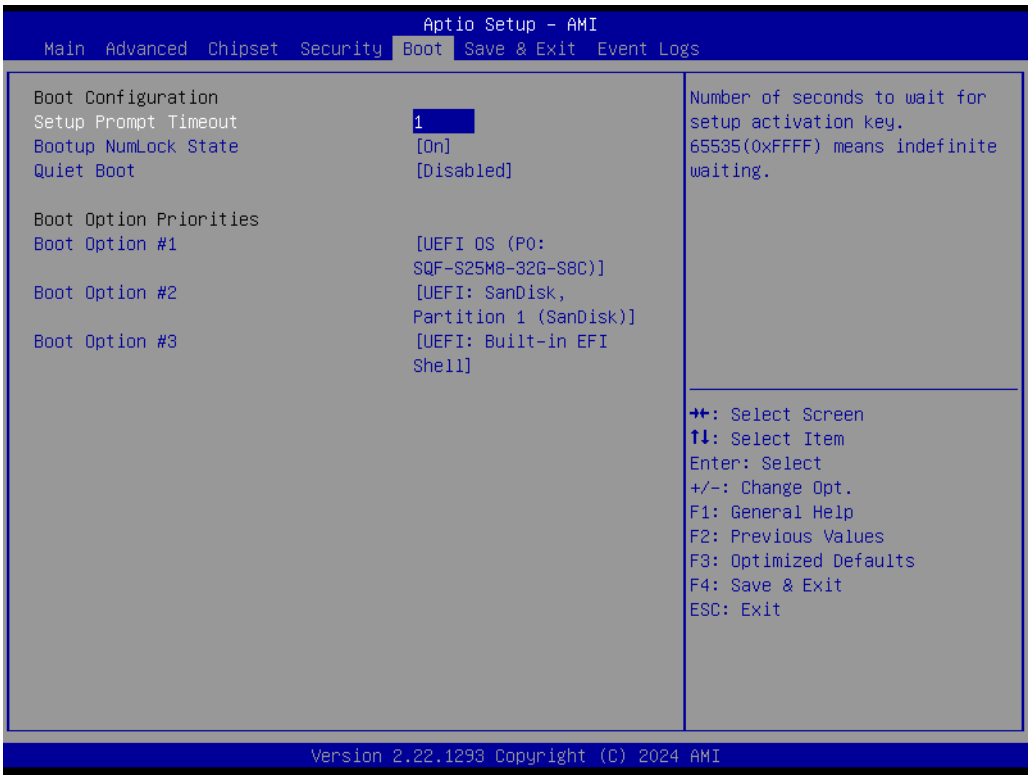


Figure 3.58 Boot

- **Setup Prompt Timeout**
  Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
- **Bootup NumLock State**
  Select the keyboard NumLock state.
- **Quiet Boot**
  Enables or disables Quiet Boot option.
- **Boot Option #1**
  Sets the system boot order.
- **Boot Option #2**
  Sets the system boot order.

3.2.6 Save & Exit

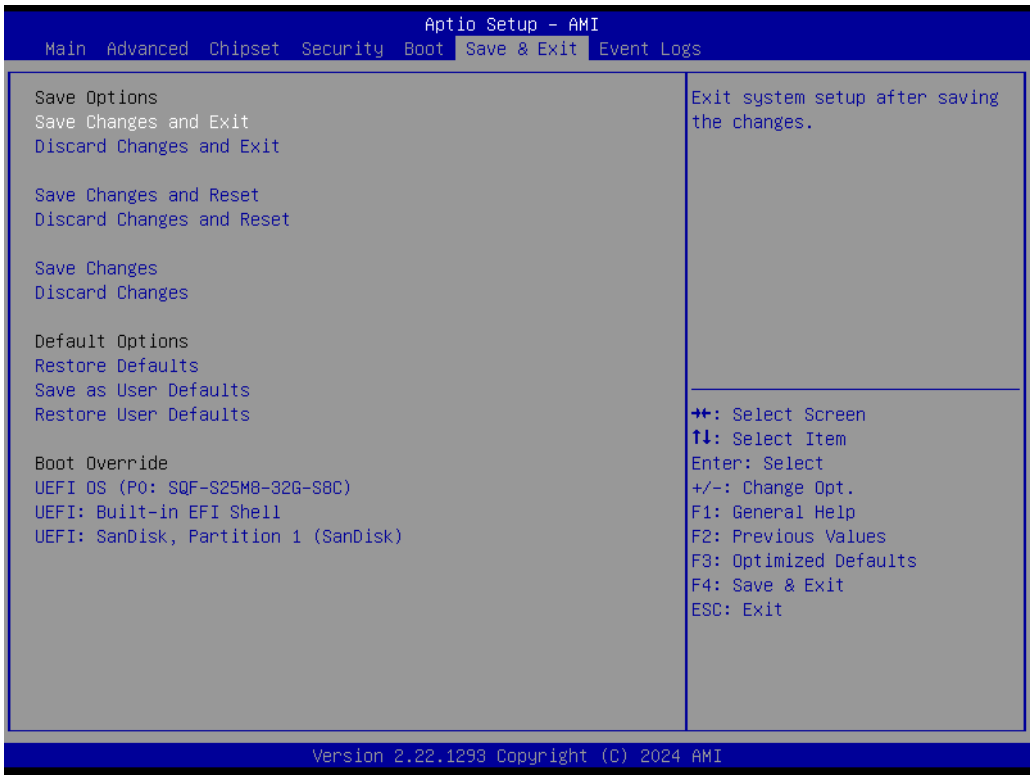


Figure 3.59 Save & Exit

- **Save Changes and Exit**
  Exit system setup after saving the changes.
- **Discard Changes and Exit**
  Exit system setup without saving any changes.
- **Save Changes and Reset**
  Reset the system after saving the changes.
- **Discard Changes and Reset**
  Reset system setup without saving any changes.
- **Save Changes**
  Save Changes done so far to any of the setup options.
- **Discard Changes**
  Discard Changes done so far to any of the setup options.
- **Restore Defaults**
  Restore/Load Default values for all the setup options.
- **Save as User Defaults**
  Save the changes done so far as User Defaults.
- **Restore User Defaults**
  Restore the User Defaults to all the setup options.
- **UEFI: Built-in EFI Shell**
  Ubuntu (P0: SQF-S25V2-256GCSBC).

3.2.7 Event Logs

Figure 3.60 Event Logs

- **Change Smbios Event Log Settings**
  Press <Enter> to change the Smbios Event Log configuration.
- **View Smbios Event Log**
  Press <Enter> to view the Smbios Event Log records.

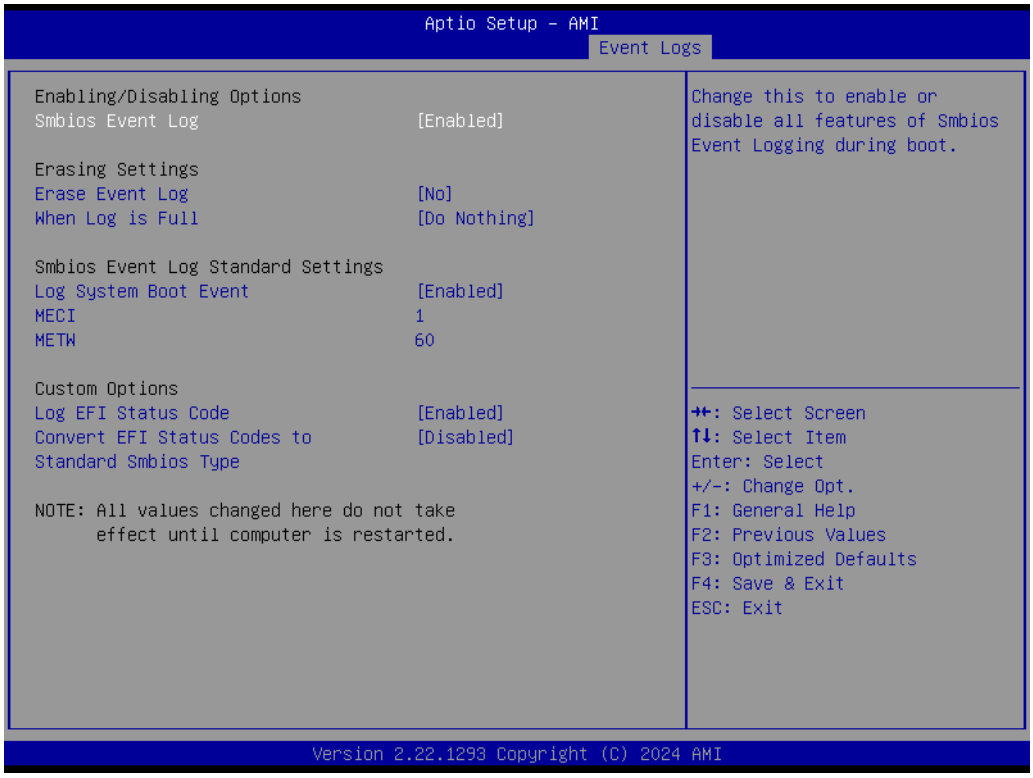


Figure 3.61 Change Smbios Event Log Settings

- **Smbios Event Log**
  Change this to enable or disable all features of Smbios Event Logging during boot.
- **Erase Event Log**
  Choose options for erasing Smbios Event Log. Erasing is done prior to any logging activation during reset.
- **When Log is Full**
  Choose options for reactions to a full Smbios Event Log.
- **Log System Boot Event**
  Choose option to enable/disable logging of System boot event.
- **MECI**
  Multiple Event Count Increment: The number of occurrences of a duplicate event that must pass before the multiple-event counter of log entry is updated.The value ranges from 1 to 255.
- **METW**
  Multiple Event Time Window: The number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes.
- **Log EFI Status Code**
  Enable or disable the logging of EFI Status Codes as OEM reserved type E0 (if not already converted to legacy).
- **Convert EFI Status Codes to Standard Smbios Type**
  Enable or disable the converting of EFI Status Codes to Standard Smbios Types (Not all may be translated).

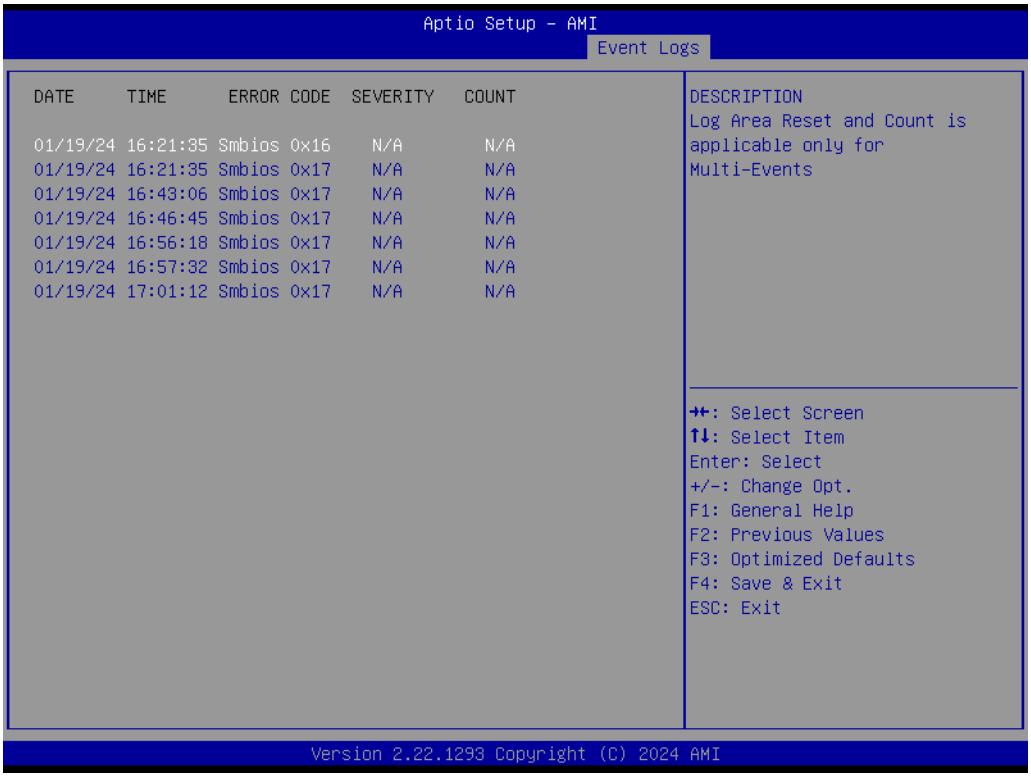


Figure 3.62 View Smbios Event Log

Chapter 4

S/W Introduction & Installation

- S/W Introduction
- Driver Installation
- Advantech iManager

4.1 S/W Introduction

The mission of Advantech Embedded Software Services is to “Enhance quality of life with Advantech platforms and Microsoft Windows embedded technology.” We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Driver Installation

The Intel Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured.

4.3 Windows Driver Setup

To install the drivers on a windows-based OS, please connect to the Internet and go to http://support.advantech.com.tw to download the drivers that you want to install and follow the Driver Setup instructions to complete the installation.

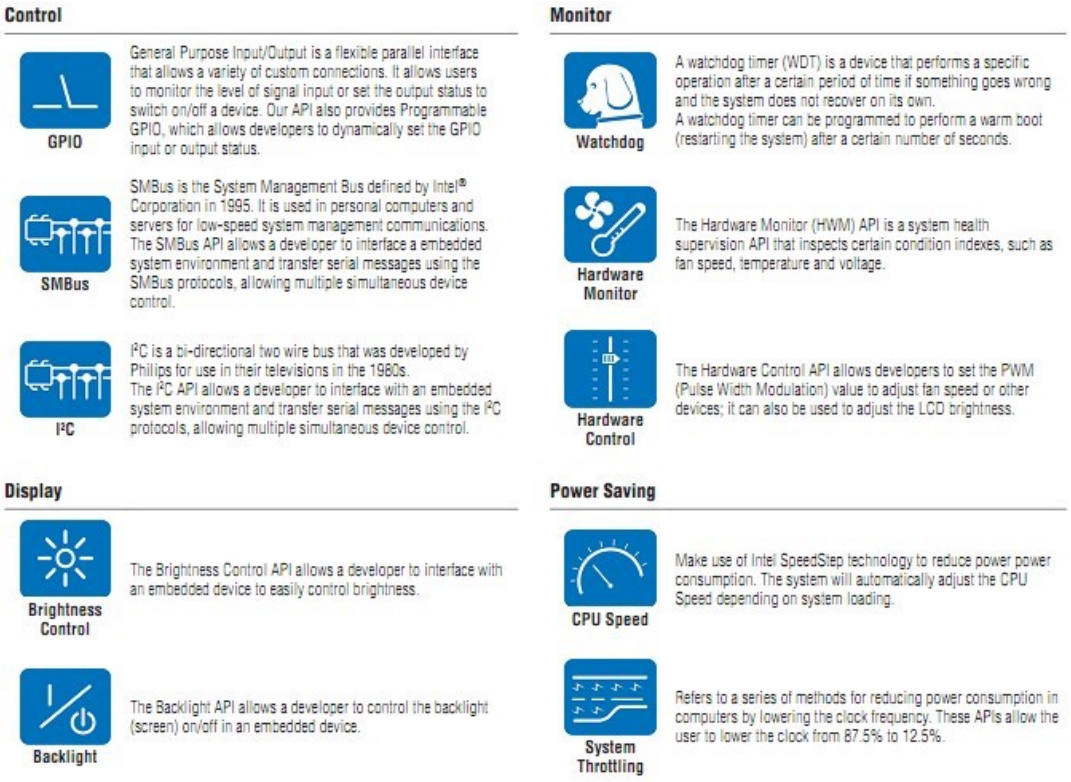
4.3.1 Other OS

Linux Ubuntu

4.4 Advantech iManager

Advantech's platforms come equipped with iManager, a micro-controller that provides embedded features for system integrators. Embedded features have been moved from the OS/BIOS level to the board level, to increase reliability and simplify integration.

iManager runs whether the operating system is running or not; it can count the boot times and running hours of the device, monitor device health, and provide an advanced watchdog to handle errors as they happen. iManager also comes with a secure & encrypted EEPROM for storing important security keys or other customer information. All the embedded functions are configured through the API and provide corresponding utilities to demonstrate. These APIs comply with PICMG EAPI (Embedded Application Programmable Interface) specifications and make these embedded features easier to integrate, speed development schedules, and provide customers with software continuity while upgrading hardware. For more details on how to use the APIs and utilities, please refer to the Advantech iManager 2.0 Software API User Manual.



Appendix A

Pin Assignment

This appendix details information about the hardware pin assignment for the SOM-E781 CPU System on Module.

Sections include:

- SOM-E781 Client Size Pin Assignment

A.1 SOM-E781 Pin Assignment

This section gives SOM-E781 pin assignment on the COM HPC connector which is compliant with COM-HPC Revision 1.10 Client Type pin-out definitions. For more details about how to use these pins and to obtain a design reference, please contact Advantech for a design guide, checklist, reference schematic, and other hardware/ software support.

Table A.1: J1 Connector Rows A and B

Pin#	Row A Description	SOM-E781 Difference	Pin#	Row B Description	SOM-E781 Difference
J1.A1	VCC		J1.B1	VCC	
J1.A2	VCC		J1.B2	PWRBTN#	
J1.A3	VCC		J1.B3	VCC	
J1.A4	VCC		J1.B4	THERMTRIP#	
J1.A5	VCC		J1.B5	VCC	
J1.A6	VCC		J1.B6	TAMPER#	
J1.A7	VCC		J1.B7	VCC	
J1.A8	VCC		J1.B8	SUS_S3#	
J1.A9	VCC		J1.B9	VCC	
J1.A10	GND		J1.B10	WD_STROBE#	
J1.A11	BATLOW#		J1.B11	WD_OUT	
J1.A12	PLTRST#		J1.B12	GND	
J1.A13	GND		J1.B13	USB5-	NA
J1.A14	USB7-	NA	J1.B14	USB5+	NA
J1.A15	USB7+	NA	J1.B15	GND	
J1.A16	GND		J1.B16	USB4-	NA
J1.A17	USB6-	NA	J1.B17	USB4+	NA
J1.A18	USB6+	NA	J1.B18	GND	
J1.A19	GND		J1.B19	RSVD	
J1.A20	ETH4_RX-	A_PCIe0_TX-	J1.B20	RSVD	
J1.A21	ETH4_RX+	A_PCIe0_TX+	J1.B21	RSVD	
J1.A22	GND		J1.B22	RSVD	VCC_5V_SBY
J1.A23	ETH5_RX-	A_PCIe1_TX-	J1.B23	RSVD	VCC_5V_SBY
J1.A24	ETH5_RX+	A_PCIe1_TX+	J1.B24	VCC_5V_SBY	
J1.A25	GND		J1.B25	USB67_OC#	NA
J1.A26	ETH6_RX-	A_PCIe2_TX-	J1.B26	USB45_OC#	NA
J1.A27	ETH6_RX+	A_PCIe2_TX+	J1.B27	USB23_OC#	
J1.A28	GND		J1.B28	USB01_OC#	
J1.A29	ETH7_RX-	A_PCIe3_TX-	J1.B29	SML1_CLK	NA
J1.A30	ETH7_RX+	A_PCIe3_TX+	J1.B30	SML1_DAT	NA
J1.A31	GND		J1.B31	PMCALERT#	NA
J1.A32	RSVD	EN_12V_CB	J1.B32	SML0_CLK	NA
J1.A33	RSVD		J1.B33	SML0_DAT	NA
J1.A34	GND		J1.B34	USB_P- D_ALERT#	NA
J1.A35	ETH4_TX-	A_PCIe4_TX-	J1.B35	USB_PD_I2C_- CLK	NA
J1.A36	ETH4_TX+	A_PCIe4_TX+	J1.B36	USB_PD_I2C_- DAT	NA
J1.A37	GND		J1.B37	USB_RT_ENA	NA
J1.A38	ETH5_TX-	A_PCIe5_TX-	J1.B38	USB1_LSRX	NA
J1.A39	ETH5_TX+	A_PCIe5_TX+	J1.B39	USB1_LSTX	NA
J1.A40	GND		J1.B40	USB0_LSRX	NA

Table A.1: J1 Connector Rows A and B					
J1.A41	ETH6_TX-	A_PCIe6_TX-	J1.B41	USB0_LSTX	NA
J1.A42	ETH6_TX+	A_PCIe6_TX+	J1.B42	GND	
J1.A43	GND		J1.B43	USB0_AUX-	NA
J1.A44	ETH7_TX-	A_PCIe7_TX-	J1.B44	USB0_AUX+	NA
J1.A45	ETH7_TX+	A_PCIe7_TX+	J1.B45	RSVD	
J1.A46	GND		J1.B46	RSVD	
J1.A47	USB1_AUX-	NA	J1.B47	VCC_BOOT_SPI	
J1.A48	USB1_AUX+	NA	J1.B48	BOOT_SPI_CS#	
J1.A49	GND		J1.B49	BSEL0	
J1.A50	eSPI_IO0	LPC_LAD0	J1.B50	BSEL1	
J1.A51	eSPI_IO1	LPC_LAD1	J1.B51	BSEL2	
J1.A52	eSPI_IO2	LPC_LAD2	J1.B52	eSPI_ALERT0#	LPC_SERIRQ
J1.A53	eSPI_IO3	LPC_LAD3	J1.B53	eSPI_ALERT1#	NA
J1.A54	eSPI_CLK	P0_LPCCLK1	J1.B54	eSPI_CS0#	LPC_LFRAM E
J1.A55	GND		J1.B55	eSPI_CS1#	NA
J1.A56	PCIe_- CLKREQ0_LO#	NA	J1.B56	eSPI_RST#	LPC_RST
J1.A57	PCIe_- CLKREQ0_HI#	NA	J1.B57	GND	
J1.A58	GND		J1.B58	PCIe_BMC_RX-	
J1.A59	PCIe_BMC_TX-		J1.B59	PCIe_BMC_RX+	
J1.A60	PCIe_BMC_TX+		J1.B60	GND	
J1.A61	GND		J1.B61	PCIe08_RX-	
J1.A62	PCIe08_TX-		J1.B62	PCIe08_RX+	
J1.A63	PCIe08_TX+		J1.B63	GND	
J1.A64	GND		J1.B64	PCIe09_RX-	
J1.A65	PCIe09_TX-		J1.B65	PCIe09_RX+	
J1.A66	PCIe09_TX+		J1.B66	GND	
J1.A67	GND		J1.B67	PCIe10_RX-	
J1.A68	PCIe10_TX-		J1.B68	PCIe10_RX+	
J1.A69	PCIe10_TX+		J1.B69	GND	
J1.A70	GND		J1.B70	PCIe11_RX-	
J1.A71	PCIe11_TX-		J1.B71	PCIe11_RX+	
J1.A72	PCIe11_TX+		J1.B72	GND	
J1.A73	GND		J1.B73	PCIe12_RX-	
J1.A74	PCIe12_TX-		J1.B74	PCIe12_RX+	
J1.A75	PCIe12_TX+		J1.B75	GND	
J1.A76	GND		J1.B76	PCIe13_RX-	
J1.A77	PCIe13_TX-		J1.B77	PCIe13_RX+	
J1.A78	PCIe13_TX+		J1.B78	GND	
J1.A79	GND		J1.B79	PCIe14_RX-	
J1.A80	PCIe14_TX-		J1.B80	PCIe14_RX+	
J1.A81	PCIe14_TX+		J1.B81	GND	
J1.A82	GND		J1.B82	PCIe15_RX-	
J1.A83	PCIe15_TX-		J1.B83	PCIe15_RX+	
J1.A84	PCIe15_TX+		J1.B84	GND	
J1.A85	GND		J1.B85	TEST#	NA
J1.A86	VCC_RTC		J1.B86	RSMRST_OUT#	
J1.A87	SUS_CLK	NA	J1.B87	UART1_TX	

Table A.1: J1 Connector Rows A and B				
J1.A88	GPIO_00	J1.B88	UART1_RX	
J1.A89	GPIO_01	J1.B89	UART1_RTS#	
J1.A90	GPIO_02	J1.B90	UART1_CTS#	
J1.A91	GPIO_03	J1.B91	IPMB_CLK	
J1.A92	GPIO_04	J1.B92	IPMB_DAT	
J1.A93	GPIO_05	J1.B93	GP_SPI_MOSI	NA
J1.A94	GPIO_06	J1.B94	GP_SPI_MISO	NA
J1.A95	GPIO_07	J1.B95	GP_SPI_CS0#	NA
J1.A96	GPIO_08	J1.B96	GP_SPI_CS1#	NA
J1.A97	GPIO_09	J1.B97	GP_SPI_CS2#	NA
J1.A98	GPIO_10	J1.B98	GP_SPI_CS3#	NA
J1.A99	GPIO_11	J1.B99	GP_SPI_CLK	NA
J1.A100	TYPE0	J1.B100	GP_SPI_ALERT#	NA

Table A.2: J1 Connector Rows C and D					
Pin#	**Row C Description**	**SOM-E781 Difference**	**Pin#**	**Row D Description**	**SOM-E781 Difference**
J1.C1	VCC		J1.D1	VCC	
J1.C2	RSTBTN#		J1.D2	VCC	
J1.C3	VCC		J1.D3	VCC	
J1.C4	CARRIER_HOT#		J1.D4	VCC	
J1.C5	VCC		J1.D5	VCC	
J1.C6	VIN_PWROK		J1.D6	VCC	
J1.C7	VCC		J1.D7	VCC	
J1.C8	SUS_S4_S5#		J1.D8	VCC	
J1.C9	VCC		J1.D9	VCC	
J1.C10	GND		J1.D10	WAKE0#	
J1.C11	FAN_PWMOUT		J1.D11	WAKE1#	
J1.C12	FAN_TACHIN		J1.D12	GND	
J1.C13	GND		J1.D13	USB1-	
J1.C14	USB3-		J1.D14	USB1+	
J1.C15	USB3+		J1.D15	GND	
J1.C16	GND		J1.D16	USB0-	
J1.C17	USB2-		J1.D17	USB0+	
J1.C18	USB2+		J1.D18	GND	
J1.C19	GND		J1.D19	ETH0_RX-	A_PCIe4_RX-
J1.C20	ETH0_TX-	A_PCIe0_RX-	J1.D20	ETH0_RX+	A_PCIe4_RX+
J1.C21	ETH0_TX+	A_PCIe0_RX+	J1.D21	GND	
J1.C22	GND		J1.D22	ETH1_RX-	A_PCIe5_RX-
J1.C23	ETH1_TX-	A_PCIe1_RX-	J1.D23	ETH1_RX+	A_PCIe5_RX+
J1.C24	ETH1_TX+	A_PCIe1_RX+	J1.D24	GND	
J1.C25	GND		J1.D25	ETH2_RX-	A_PCIe6_RX-
J1.C26	ETH2_TX-	A_PCIe2_RX-	J1.D26	ETH2_RX+	A_PCIe6_RX+
J1.C27	ETH2_TX+	A_PCIe2_RX+	J1.D27	GND	
J1.C28	GND		J1.D28	ETH3_RX-	A_PCIe7_RX-
J1.C29	ETH3_TX-	A_PCIe3_RX-	J1.D29	ETH3_RX+	A_PCIe7_RX+
J1.C30	ETH3_TX+	A_PCIe3_RX+	J1.D30	GND	
J1.C31	GND		J1.D31	USB3_SSTX-	

Table A.2: J1 Connector Rows C and D					
J1.C32	USB3_SSRX-		J1.D32	USB3_SSTX+	
J1.C33	USB3_SSRX+		J1.D33	GND	
J1.C34	GND		J1.D34	USB2_SSTX-	
J1.C35	USB2_SSRX-		J1.D35	USB2_SSTX+	
J1.C36	USB2_SSRX+		J1.D36	GND	
J1.C37	GND		J1.D37	USB1_SSTX0-	
J1.C38	USB1_SSRX0-		J1.D38	USB1_SSTX0+	
J1.C39	USB1_SSRX0+		J1.D39	GND	
J1.C40	GND		J1.D40	USB1_SSTX1-	NA
J1.C41	USB1_SSRX1-	NA	J1.D41	USB1_SSTX1+	NA
J1.C42	USB1_SSRX1+	NA	J1.D42	GND	
J1.C43	GND		J1.D43	USB0_SSTX0-	
J1.C44	USB0_SSRX0-		J1.D44	USB0_SSTX0+	
J1.C45	USB0_SSRX0+		J1.D45	GND	
J1.C46	GND		J1.D46	USB0_SSTX1-	NA
J1.C47	USB0_SSRX1-	NA	J1.D47	USB0_SSTX1+	NA
J1.C48	USB0_SSRX1+	NA	J1.D48	GND	
J1.C49	GND		J1.D49	SATA0_RX-	
J1.C50	BOOT_SPI_IO0		J1.D50	SATA0_RX+	
J1.C51	BOOT_SPI_IO1		J1.D51	GND	
J1.C52	BOOT_SPI_IO2		J1.D52	SATA0_TX-	
J1.C53	BOOT_SPI_IO3		J1.D53	SATA0_TX+	
J1.C54	BOOT_SPI_CLK		J1.D54	GND	
J1.C55	GND		J1.D55	SATA1_RX-	
J1.C56	PCIe_REF-CLK0_HI-		J1.D56	SATA1_RX+	
J1.C57	PCIe_REF-CLK0_HI+		J1.D57	GND	
J1.C58	GND		J1.D58	SATA1_TX-	
J1.C59	PCIe_REF-CLK0_LO-		J1.D59	SATA1_TX+	
J1.C60	PCIe_REF-CLK0_LO+		J1.D60	GND	
J1.C61	GND		J1.D61	PCIe00_TX-	
J1.C62	PCIe00_RX-		J1.D62	PCIe00_TX+	
J1.C63	PCIe00_RX+		J1.D63	GND	
J1.C64	GND		J1.D64	PCIe01_TX-	
J1.C65	PCIe01_RX-		J1.D65	PCIe01_TX+	
J1.C66	PCIe01_RX+		J1.D66	GND	
J1.C67	GND		J1.D67	PCIe02_TX-	
J1.C68	PCIe02_RX-		J1.D68	PCIe02_TX+	
J1.C69	PCIe02_RX+		J1.D69	GND	
J1.C70	GND		J1.D70	PCIe03_TX-	
J1.C71	PCIe03_RX-		J1.D71	PCIe03_TX+	
J1.C72	PCIe03_RX+		J1.D72	GND	
J1.C73	GND		J1.D73	PCIe04_TX-	
J1.C74	PCIe04_RX-		J1.D74	PCIe04_TX+	
J1.C75	PCIe04_RX+		J1.D75	GND	
J1.C76	GND		J1.D76	PCIe05_TX-	
J1.C77	PCIe05_RX-		J1.D77	PCIe05_TX+	
J1.C78	PCIe05_RX+		J1.D78	GND	

Table A.2: J1 Connector Rows C and D					
J1.C79	GND		J1.D79	PCIe06_TX-	
J1.C80	PCIe06_RX-		J1.D80	PCIe06_TX+	
J1.C81	PCIe06_RX+		J1.D81	GND	
J1.C82	GND		J1.D82	PCIe07_TX-	
J1.C83	PCIe07_RX-		J1.D83	PCIe07_TX+	
J1.C84	PCIe07_RX+		J1.D84	GND	
J1.C85	GND		J1.D85	NBASET0_MDI0-	
J1.C86	SMB_CLK		J1.D86	NBASET0_MDI0+	
J1.C87	SMB_DAT		J1.D87	GND	
J1.C88	SMB_ALERT#	NA	J1.D88	NBASET0_MDI1-	
J1.C89	UART0_TX		J1.D89	NBASET0_MDI1+	
J1.C90	UART0_RX		J1.D90	GND	
J1.C91	UART0_RTS#		J1.D91	NBASET0_MDI2-	
J1.C92	UART0_CTS#		J1.D92	NBASET0_MDI2+	
J1.C93	I2C0_CLK		J1.D93	GND	
J1.C94	I2C0_DAT		J1.D94	NBASET0_MDI3-	
J1.C95	I2C0_ALERT#		J1.D95	NBASET0_MDI3+	
J1.C96	I2C1_CLK		J1.D96	GND	
J1.C97	I2C1_DAT		J1.D97	NBA- SET0_LINK_-MAX#	
J1.C98	NBASET0_SDP		J1.D98	NBA-SET0_LINK_MID #	
J1.C99	NBASET0_C-TREF	NA	J1.D99	NBA-SET0_LINK_ACT #	
J1.C100	TYPE1		J1.D100	TYPE2	

Table A.3: J2 Connector Rows E and F					
Pin#	**Row E Description**	**SOM-E781 Difference**	**Pin#**	**Row F Description**	**SOM-E781 Difference**
J2.E1	RAPID_SHUT-DOWN		J2.F1	ETH2_SDP	VCC
J2.E2	GND		J2.F2	ETH3_SDP	VCC
J2.E3	RSVD	VCC	J2.F3	ETH4_SDP	VCC
J2.E4	RSVD	VCC	J2.F4	ETH5_SDP	VCC
J2.E5	GND		J2.F5	ETH6_SDP	VCC
J2.E6	RSVD	VCC	J2.F6	ETH7_SDP	VCC
J2.E7	RSVD	VCC	J2.F7	ETH4-7_I2C_- CLK	GND
J2.E8	GND		J2.F8	ETH4-7_I2C_- DAT	GND
J2.E9	RSVD	GND	J2.F9	ETH4-7_INT#	GND
J2.E10	RSVD	GND	J2.F10	ETH4-7_MDIO_-CLK	GND
J2.E11	GND		J2.F11	ETH4-7_MDIO_-DAT	A_PCIe8_RX-
J2.E12	RSVD	A_PCIe8_TX-	J2.F12	ETH4- 7_PHY_INT#	A_PCIe8_RX+
J2.E13	RSVD	A_PCIe8_TX+	J2.F13	ETH4-7_PHY_RST#	
J2.E14	GND		J2.F14	ETH4-7_PRSNT#	A_PCIe9_RX-
J2.E15	RSVD	A_PCIe9_TX-	J2.F15	RSVD	A_PCIe9_RX+
J2.E16	RSVD	A_PCIe9_TX+	J2.F16	RSVD	
J2.E17	GND		J2.F17	RSVD	A_PCIe10_RX-
J2.E18	RSVD	A_PCIe10_TX-	J2.F18	RSVD	A_PCIe10_RX+

Table A.3: J2 Connector Rows E and F				
J2.E19	RSVD	A_PCIe10_TX+	J2.F19	GND
J2.E20	GND		J2.F20	PCIe32_RX-
J2.E21	PCIe32_TX-		J2.F21	PCIe32_RX+
J2.E22	PCIe32_TX+		J2.F22	GND
J2.E23	GND		J2.F23	PCIe33_RX-
J2.E24	PCIe33_TX-		J2.F24	PCIe33_RX+
J2.E25	PCIe33_TX+		J2.F25	GND
J2.E26	GND		J2.F26	PCIe34_RX-
J2.E27	PCIe34_TX-		J2.F27	PCIe34_RX+
J2.E28	PCIe34_TX+		J2.F28	GND
J2.E29	GND		J2.F29	PCIe35_RX-
J2.E30	PCIe35_TX-		J2.F30	PCIe35_RX+
J2.E31	PCIe35_TX+		J2.F31	GND
J2.E32	GND		J2.F32	PCIe36_RX-
J2.E33	PCIe36_TX-		J2.F33	PCIe36_RX+
J2.E34	PCIe36_TX+		J2.F34	GND
J2.E35	GND		J2.F35	PCIe37_RX-
J2.E36	PCIe37_TX-		J2.F36	PCIe37_RX+
J2.E37	PCIe37_TX+		J2.F37	GND
J2.E38	GND		J2.F38	PCIe38_RX-
J2.E39	PCIe38_TX-		J2.F39	PCIe38_RX+
J2.E40	PCIe38_TX+		J2.F40	GND
J2.E41	GND		J2.F41	PCIe39_RX-
J2.E42	PCIe39_TX-		J2.F42	PCIe39_RX+
J2.E43	PCIe39_TX+		J2.F43	GND
J2.E44	GND		J2.F44	PCIe16_RX-
J2.E45	PCIe16_TX-		J2.F45	PCIe16_RX+
J2.E46	PCIe16_TX+		J2.F46	GND
J2.E47	GND		J2.F47	PCIe17_RX-
J2.E48	PCIe17_TX-		J2.F48	PCIe17_RX+
J2.E49	PCIe17_TX+		J2.F49	GND
J2.E50	GND		J2.F50	PCIe18_RX-
J2.E51	PCIe18_TX-		J2.F51	PCIe18_RX+
J2.E52	PCIe18_TX+		J2.F52	GND
J2.E53	GND		J2.F53	PCIe19_RX-
J2.E54	PCIe19_TX-		J2.F54	PCIe19_RX+
J2.E55	PCIe19_TX+		J2.F55	GND
J2.E56	GND		J2.F56	PCIe20_RX-
J2.E57	PCIe20_TX-		J2.F57	PCIe20_RX+
J2.E58	PCIe20_TX+		J2.F58	GND
J2.E59	GND		J2.F59	PCIe21_RX-
J2.E60	PCIe21_TX-		J2.F60	PCIe21_RX+
J2.E61	PCIe21_TX+		J2.F61	GND
J2.E62	GND		J2.F62	PCIe22_RX-
J2.E63	PCIe22_TX-		J2.F63	PCIe22_RX+
J2.E64	PCIe22_TX+		J2.F64	GND
J2.E65	GND		J2.F65	PCIe23_RX-
J2.E66	PCIe23_TX-		J2.F66	PCIe23_RX+
J2.E67	PCIe23_TX+		J2.F67	GND
J2.E68	GND		J2.F68	PCIe48_RX-

Table A.3: J2 Connector Rows E and F					
J2.E69	PCIe48_TX-		J2.F69	PCIe48_RX+	
J2.E70	PCIe48_TX+		J2.F70	GND	
J2.E71	GND		J2.F71	PCIe49_RX-	
J2.E72	PCIe49_TX-		J2.F72	PCIe49_RX+	
J2.E73	PCIe49_TX+		J2.F73	GND	
J2.E74	GND		J2.F74	PCIe50_RX-	
J2.E75	PCIe50_TX-		J2.F75	PCIe50_RX+	
J2.E76	PCIe50_TX+		J2.F76	GND	
J2.E77	GND		J2.F77	PCIe51_RX-	
J2.E78	PCIe51_TX-		J2.F78	PCIe51_RX+	
J2.E79	PCIe51_TX+		J2.F79	GND	
J2.E80	GND		J2.F80	PCIe52_RX-	
J2.E81	PCIe52_TX-		J2.F81	PCIe52_RX+	
J2.E82	PCIe52_TX+		J2.F82	GND	
J2.E83	GND		J2.F83	PCIe53_RX-	
J2.E84	PCIe53_TX-		J2.F84	PCIe53_RX+	
J2.E85	PCIe53_TX+		J2.F85	GND	
J2.E86	GND		J2.F86	PCIe54_RX-	
J2.E87	PCIe54_TX-		J2.F87	PCIe54_RX+	
J2.E88	PCIe54_TX+		J2.F88	GND	
J2.E89	GND		J2.F89	PCIe55_RX-	
J2.E90	PCIe55_TX-		J2.F90	PCIe55_RX+	
J2.E91	PCIe55_TX+		J2.F91	GND	
J2.E92	GND		J2.F92	PCIe_REFCLK2-	
J2.E93	PCIe_REFCLK1-		J2.F93	PCIe_REFCLK2+	
J2.E94	PCIe_REFCLK1+		J2.F94	GND	
J2.E95	GND		J2.F95	PCIe_CLKREQ3#	NA
J2.E96	PCIe_CLKREQ1#	NA	J2.F96	ETH0-3_PRSNT#	NA
J2.E97	PCIe_CLKREQ2#	NA	J2.F97	ETH0-3_PHY_RST#	NA
J2.E98	PCIe_-CLKREQ_OUT0#	NA	J2.F98	ETH0_SDP	NA
J2.E99	PCIe_-CLKREQ_OUT1#	NA	J2.F99	ETH1_SDP	NA
J2.E100	PCIe_PER-ST_IN0#		J2.F100	PCIe_PER-ST_IN1#	

Table A.4: J2 Connector Rows G and H					
Pin#	**Row G Description**	**SOM-E781 Difference**	**Pin#**	**Row H Description**	**SOM-E781 Difference**
J2.G1	RSVD	VCC_5V_SBY	J2.H1	RSVD	VCC
J2.G2	RSVD	VCC	J2.H2	RSVD	VCC
J2.G3	RSVD	VCC	J2.H3	RSVD	VCC
J2.G4	RSVD	VCC	J2.H4	RSVD	VCC
J2.G5	RSVD	VCC	J2.H5	RSVD	VCC
J2.G6	RSVD	VCC	J2.H6	RSVD	VCC
J2.G7	RSVD	VCC	J2.H7	RSVD	GND
J2.G8	RSVD	GND	J2.H8	RSVD	GND
J2.G9	RSVD	GND	J2.H9	RSVD	GND
J2.G10	RSVD	GND	J2.H10	RSVD	GND

Table A.4: J2 Connector Rows G and H					
J2.G11	RSVD	GND	J2.H11	RSVD	A_PCIe11_TX-
J2.G12	RSVD	A_PCIe11_RX-	J2.H12	RSVD	A_PCIe11_TX+
J2.G13	RSVD	A_PCIe11_RX+	J2.H13	RSVD	
J2.G14	GND		J2.H14	RSVD	A_PCIe12_TX-
J2.G15	RSVD	A_PCIe12_RX-	J2.H15	RSVD	A_PCIe12_TX+
J2.G16	RSVD	A_PCIe12_RX+	J2.H16	RSVD	
J2.G17	RSVD		J2.H17	RSVD	A_PCIe13_TX-
J2.G18	RSVD	A_PCIe13_RX-	J2.H18	RSVD	A_PCIe13_TX+
J2.G19	RSVD	A_PCIe13_RX+	J2.H19	GND	
J2.G20	GND		J2.H20	PCIe40_TX-	
J2.G21	PCIe40_RX-		J2.H21	PCIe40_TX+	
J2.G22	PCIe40_RX+		J2.H22	GND	
J2.G23	GND		J2.H23	PCIe41_TX-	
J2.G24	PCIe41_RX-		J2.H24	PCIe41_TX+	
J2.G25	PCIe41_RX+		J2.H25	GND	
J2.G26	GND		J2.H26	PCIe42_TX-	
J2.G27	PCIe42_RX-		J2.H27	PCIe42_TX+	
J2.G28	PCIe42_RX+		J2.H28	GND	
J2.G29	GND		J2.H29	PCIe43_TX-	
J2.G30	PCIe43_RX-		J2.H30	PCIe43_TX+	
J2.G31	PCIe43_RX+		J2.H31	GND	
J2.G32	GND		J2.H32	PCIe44_TX-	
J2.G33	PCIe44_RX-		J2.H33	PCIe44_TX+	
J2.G34	PCIe44_RX+		J2.H34	GND	
J2.G35	GND		J2.H35	PCIe45_TX-	
J2.G36	PCIe45_RX-		J2.H36	PCIe45_TX+	
J2.G37	PCIe45_RX+		J2.H37	GND	
J2.G38	GND		J2.H38	PCIe46_TX-	
J2.G39	PCIe46_RX-		J2.H39	PCIe46_TX+	
J2.G40	PCIe46_RX+		J2.H40	GND	
J2.G41	GND		J2.H41	PCIe47_TX-	
J2.G42	PCIe47_RX-		J2.H42	PCIe47_TX+	
J2.G43	PCIe47_RX+		J2.H43	GND	
J2.G44	GND		J2.H44	PCIe24_TX-	
J2.G45	PCIe24_RX-		J2.H45	PCIe24_TX+	
J2.G46	PCIe24_RX+		J2.H46	GND	
J2.G47	GND		J2.H47	PCIe25_TX-	
J2.G48	PCIe25_RX-		J2.H48	PCIe25_TX+	
J2.G49	PCIe25_RX+		J2.H49	GND	
J2.G50	GND		J2.H50	PCIe26_TX-	
J2.G51	PCIe26_RX-		J2.H51	PCIe26_TX+	
J2.G52	PCIe26_RX+		J2.H52	GND	
J2.G53	GND		J2.H53	PCIe27_TX-	
J2.G54	PCIe27_RX-		J2.H54	PCIe27_TX+	
J2.G55	PCIe27_RX+		J2.H55	GND	
J2.G56	GND		J2.H56	PCIe28_TX-	
J2.G57	PCIe28_RX-		J2.H57	PCIe28_TX+	
J2.G58	PCIe28_RX+		J2.H58	GND	
J2.G59	GND		J2.H59	PCIe29_TX-	
J2.G60	PCIe29_RX-		J2.H60	PCIe29_TX+	

Table A.4: J2 Connector Rows G and H					
J2.G61	PCIe29_RX+		J2.H61	GND	
J2.G62	GND		J2.H62	PCIe30_TX-	
J2.G63	PCIe30_RX-		J2.H63	PCIe30_TX+	
J2.G64	PCIe30_RX+		J2.H64	GND	
J2.G65	GND		J2.H65	PCIe31_TX-	
J2.G66	PCIe31_RX-		J2.H66	PCIe31_TX+	
J2.G67	PCIe31_RX+		J2.H67	GND	
J2.G68	GND		J2.H68	PCIe56_TX-	
J2.G69	PCIe56_RX-		J2.H69	PCIe56_TX+	
J2.G70	PCIe56_RX+		J2.H70	GND	
J2.G71	GND		J2.H71	PCIe57_TX-	
J2.G72	PCIe57_RX-		J2.H72	PCIe57_TX+	
J2.G73	PCIe57_RX+		J2.H73	GND	
J2.G73	GND		J2.H74	PCIe58_TX-	
J2.G75	PCIe58_RX-		J2.H75	PCIe58_TX+	
J2.G76	PCIe58_RX+		J2.H76	GND	
J2.G77	GND		J2.H77	PCIe59_TX-	
J2.G78	PCIe59_RX-		J2.H78	PCIe59_TX+	
J2.G79	PCIe59_RX+		J2.H79	GND	
J2.G80	GND		J2.H80	PCIe60_TX-	
J2.G81	PCIe60_RX-		J2.H81	PCIe60_TX+	
J2.G82	PCIe60_RX+		J2.H82	GND	
J2.G83	GND		J2.H83	PCIe61_TX-	
J2.G84	PCIe61_RX-		J2.H84	PCIe61_TX+	
J2.G85	PCIe61_RX+		J2.H85	GND	
J2.G86	GND		J2.H86	PCIe62_TX-	
J2.G87	PCIe62_RX-		J2.H87	PCIe62_TX+	
J2.G88	PCIe62_RX+		J2.H88	GND	
J2.G89	GND		J2.H89	PCIe63_TX-	
J2.G90	PCIe63_RX-		J2.H90	PCIe63_TX+	
J2.G91	PCIe63_RX+		J2.H91	GND	
J2.G92	GND		J2.H92	PCIe_REF-CLKIN0-	NA
J2.G93	PCIe_REFCLK3-		J2.H93	PCIe_REF-CLKIN0+	NA
J2.G94	PCIe_REFCLK3+		J2.H94	GND	
J2.G95	GND		J2.H95	PCIe_REF-CLKIN1-	NA
J2.G96	ETH0-3_I2C_CLK	NA	J2.H96	PCIe_REF-CLKIN1+	NA
J2.G97	ETH0-3_I2C_DAT	NA	J2.H97	GND	
J2.G98	ETH0-3_PHY_INT#	NA	J2.H98	ETH0-3_MDIO_-CLK	NA
J2.G99	ETH0-3_INT#	NA	J2.H99	ETH0-3_MDIO_-DAT	NA
J2.G100	PCIe_WAKE_OUT0#	NA	J2.H100	PCIe_WAKE_OUT1#	NA

Appendix B

Watchdog Timer

This appendix gives you the information about the watchdog timer programming on the SOM-E781 CPU System on Module.

Sections include:

- Programming the Watchdog Timer

B.1 Programming the Watchdog Timer

Table B.1: Programming the Watchdog Timer

Trigger Event	Note
IRQ	BIOS setting default disable**
NMI	N/A
SCI	Power button event
Power Off	Support
H/W Restart	Support
External WDT	Support

** WDT new driver support automatically selects an available IRQ number from the BIOS, and then sets it to EC. Only Win8.1 and Win10 support it.

In other OS, it will still use the IRQ number from the BIOS setting as usual. For details, please refer to the iManager & Software API User Manual.

Appendix C

Programming GPIO

This Appendix details illustration of the General Purpose Input and Output pin settings.

Sections include:

- **GPIO Register**

C.1 GPIO Register

Table C.1: GPIO Register	
GPIO Byte Mapping	**H/W Pin Name**
BIT0	GPIO0
BIT1	GPIO1
BIT2	GPIO2
BIT3	GPIO3
BIT4	GPIO4
BIT5	GPIO5
BIT6	GPIO6
BIT7	GPIO7
BIT8	GPIO8
BIT9	GPIO9
BIT10	GPIO10
BIT11	GPIO11

For details, please refer to the iManager and Software API User Manual.

Appendix D

System Assignments

This appendix gives you information about the system resource allocation on the SOM-E781 CPU System on Module.

Sections include:

- System I/O ports
- Interrupt Assignments
- 1st MB Memory Map

D.1 System I/O Ports

Table D.1: System I/O Ports

Addr. Range (Hex)	Device
0x00000299-0x0000029A	Motherboard resources
0x000002C0-0x000002DF	Motherboard resources
0x000002A0-0x000002BF	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x0000029E-0x000002AD	Motherboard resources
0x00000060-0x0000006F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x000002F0-0x000002F7	Motherboard resources
0x00000062-0x00000062	Microsoft ACPI-Compliant Embedded Controller
0x00000066-0x00000066	Microsoft ACPI-Compliant Embedded Controller
0x00000070-0x00000071	System CMOS/real time clock
0x00003000-0x00003FFF	PCI Express Root Port
0x00003000-0x00003FFF	Microsoft Basic Display Adapter
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000020-0x00000021	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x00000000-0x000002FF	PCI Express Root Complex
0x00000000-0x000002FF	Direct memory access controller
0x00000300-0x000003AF	PCI Express Root Complex
0x000003E0-0x00000CF7	PCI Express Root Complex
0x000003B0-0x000003DF	PCI Express Root Complex
0x00001000-0x00003FFF	PCI Express Root Complex
0x00004000-0x00006FFF	PCI Express Root Complex
0x00007000-0x0000FFFF	PCI Express Root Complex
0x00000040-0x00000043	System timer
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x0000006F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000B1-0x000000B1	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x000004D0-0x000004D1	Motherboard resources
0x0000040B-0x0000040B	Motherboard resources

Table D.1: System I/O Ports	
0x000004D6-0x000004D6	Motherboard resources
0x00000C00-0x00000C01	Motherboard resources
0x00000C14-0x00000C14	Motherboard resources
0x00000C50-0x00000C51	Motherboard resources
0x00000C52-0x00000C52	Motherboard resources
0x00000C6C-0x00000C6C	Motherboard resources
0x00000C6F-0x00000C6F	Motherboard resources
0x00000CD0-0x00000CD1	Motherboard resources
0x00000CD2-0x00000CD3	Motherboard resources
0x00000CD4-0x00000CD5	Motherboard resources
0x00000CD6-0x00000CD7	Motherboard resources
0x00000CD8-0x00000CDF	Motherboard resources
0x00000800-0x0000089F	Motherboard resources
0x00000B00-0x00000B0F	Motherboard resources
0x00000B20-0x00000B3F	Motherboard resources
0x00000900-0x0000090F	Motherboard resources
0x00000910-0x0000091F	Motherboard resources
0x0000FE00-0x0000FEFE	Motherboard resources
0x00000061-0x00000061	System speaker
0x00000081-0x00000083	Direct memory access controller
0x00000087-0x00000087	Direct memory access controller
0x00000089-0x0000008B	Direct memory access controller
0x0000008F-0x0000008F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller

D.2 Interrupt Assignments

Table D.2: Interrupt Assignments

Interrupt#	Interrupt Source
IRQ 4294967288	Standard SATA AHCI Controller
IRQ 7	AMD GPIO Controller
IRQ 4294967287	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967286	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967285	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967284	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967283	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967282	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967281	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967280	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967294	PCI Express Root Port
IRQ 4294967291	PCI Express Root Port
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 4294967271	Intel(R) Ethernet Controller I226-LM
IRQ 4294967270	Intel(R) Ethernet Controller I226-LM
IRQ 4294967269	Intel(R) Ethernet Controller I226-LM
IRQ 4294967268	Intel(R) Ethernet Controller I226-LM
IRQ 4294967267	Intel(R) Ethernet Controller I226-LM
IRQ 4294967266	Intel(R) Ethernet Controller I226-LM
IRQ 4294967265	Intel(R) Ethernet Controller I226-LM
IRQ 4294967264	Intel(R) Ethernet Controller I226-LM
IRQ 4294967263	Intel(R) Ethernet Controller I226-LM
IRQ 4294967262	Intel(R) Ethernet Controller I226-LM
IRQ 4294967261	Intel(R) Ethernet Controller I226-LM
IRQ 4294967260	Intel(R) Ethernet Controller I226-LM
IRQ 4294967259	Intel(R) Ethernet Controller I226-LM
IRQ 4294967258	Intel(R) Ethernet Controller I226-LM
IRQ 4294967257	Intel(R) Ethernet Controller I226-LM
IRQ 4294967256	Intel(R) Ethernet Controller I226-LM
IRQ 4294967255	Intel(R) Ethernet Controller I226-LM
IRQ 4294967254	Intel(R) Ethernet Controller I226-LM
IRQ 4294967253	Intel(R) Ethernet Controller I226-LM
IRQ 4294967252	Intel(R) Ethernet Controller I226-LM
IRQ 4294967251	Intel(R) Ethernet Controller I226-LM
IRQ 4294967250	Intel(R) Ethernet Controller I226-LM
IRQ 4294967249	Intel(R) Ethernet Controller I226-LM
IRQ 4294967248	Intel(R) Ethernet Controller I226-LM
IRQ 4294967247	Intel(R) Ethernet Controller I226-LM
IRQ 4294967246	Intel(R) Ethernet Controller I226-LM
IRQ 4294967245	Intel(R) Ethernet Controller I226-LM
IRQ 4294967244	Intel(R) Ethernet Controller I226-LM
IRQ 4294967243	Intel(R) Ethernet Controller I226-LM

Table D.2: Interrupt Assignments	
IRQ 4294967242	Intel(R) Ethernet Controller I226-LM
IRQ 4294967241	Intel(R) Ethernet Controller I226-LM
IRQ 4294967240	Intel(R) Ethernet Controller I226-LM
IRQ 4294967239	Intel(R) Ethernet Controller I226-LM
IRQ 4294967238	Intel(R) Ethernet Controller I226-LM
IRQ 4294967237	Intel(R) Ethernet Controller I226-LM
IRQ 4294967236	Intel(R) Ethernet Controller I226-LM
IRQ 4294967235	Intel(R) Ethernet Controller I226-LM
IRQ 4294967234	Intel(R) Ethernet Controller I226-LM
IRQ 4294967233	Intel(R) Ethernet Controller I226-LM
IRQ 4294967232	Intel(R) Ethernet Controller I226-LM
IRQ 4294967231	Intel(R) Ethernet Controller I226-LM
IRQ 4294967230	Intel(R) Ethernet Controller I226-LM
IRQ 4294967229	Intel(R) Ethernet Controller I226-LM
IRQ 4294967228	Intel(R) Ethernet Controller I226-LM
IRQ 4294967227	Intel(R) Ethernet Controller I226-LM
IRQ 4294967226	Intel(R) Ethernet Controller I226-LM
IRQ 4294967225	Intel(R) Ethernet Controller I226-LM
IRQ 4294967224	Intel(R) Ethernet Controller I226-LM
IRQ 4294967223	Intel(R) Ethernet Controller I226-LM
IRQ 4294967222	Intel(R) Ethernet Controller I226-LM
IRQ 4294967221	Intel(R) Ethernet Controller I226-LM
IRQ 4294967220	Intel(R) Ethernet Controller I226-LM
IRQ 4294967219	Intel(R) Ethernet Controller I226-LM
IRQ 4294967218	Intel(R) Ethernet Controller I226-LM
IRQ 4294967217	Intel(R) Ethernet Controller I226-LM
IRQ 4294967216	Intel(R) Ethernet Controller I226-LM
IRQ 4294967215	Intel(R) Ethernet Controller I226-LM
IRQ 4294967214	Intel(R) Ethernet Controller I226-LM
IRQ 4294967213	Intel(R) Ethernet Controller I226-LM
IRQ 4294967212	Intel(R) Ethernet Controller I226-LM
IRQ 4294967211	Intel(R) Ethernet Controller I226-LM
IRQ 4294967210	Intel(R) Ethernet Controller I226-LM
IRQ 4294967209	Intel(R) Ethernet Controller I226-LM
IRQ 4294967208	Intel(R) Ethernet Controller I226-LM
IRQ 4294967207	Intel(R) Ethernet Controller I226-LM
IRQ 6	Motherboard resources
IRQ 4294967292	PCI Express Root Port
IRQ 55	Microsoft ACPI-Compliant System
IRQ 56	Microsoft ACPI-Compliant System
IRQ 57	Microsoft ACPI-Compliant System
IRQ 58	Microsoft ACPI-Compliant System
IRQ 59	Microsoft ACPI-Compliant System
IRQ 60	Microsoft ACPI-Compliant System
IRQ 61	Microsoft ACPI-Compliant System
IRQ 62	Microsoft ACPI-Compliant System
IRQ 63	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 64	Microsoft ACPI-Compliant System
IRQ 65	Microsoft ACPI-Compliant System
IRQ 66	Microsoft ACPI-Compliant System
IRQ 67	Microsoft ACPI-Compliant System
IRQ 68	Microsoft ACPI-Compliant System
IRQ 69	Microsoft ACPI-Compliant System
IRQ 70	Microsoft ACPI-Compliant System
IRQ 71	Microsoft ACPI-Compliant System
IRQ 72	Microsoft ACPI-Compliant System
IRQ 73	Microsoft ACPI-Compliant System
IRQ 74	Microsoft ACPI-Compliant System
IRQ 75	Microsoft ACPI-Compliant System
IRQ 76	Microsoft ACPI-Compliant System
IRQ 77	Microsoft ACPI-Compliant System
IRQ 78	Microsoft ACPI-Compliant System
IRQ 79	Microsoft ACPI-Compliant System
IRQ 80	Microsoft ACPI-Compliant System
IRQ 81	Microsoft ACPI-Compliant System
IRQ 82	Microsoft ACPI-Compliant System
IRQ 83	Microsoft ACPI-Compliant System
IRQ 84	Microsoft ACPI-Compliant System
IRQ 85	Microsoft ACPI-Compliant System
IRQ 86	Microsoft ACPI-Compliant System
IRQ 87	Microsoft ACPI-Compliant System
IRQ 88	Microsoft ACPI-Compliant System
IRQ 89	Microsoft ACPI-Compliant System
IRQ 90	Microsoft ACPI-Compliant System
IRQ 91	Microsoft ACPI-Compliant System
IRQ 91	High Definition Audio Controller
IRQ 92	Microsoft ACPI-Compliant System
IRQ 93	Microsoft ACPI-Compliant System
IRQ 94	Microsoft ACPI-Compliant System
IRQ 95	Microsoft ACPI-Compliant System
IRQ 96	Microsoft ACPI-Compliant System
IRQ 97	Microsoft ACPI-Compliant System
IRQ 98	Microsoft ACPI-Compliant System
IRQ 99	Microsoft ACPI-Compliant System
IRQ 100	Microsoft ACPI-Compliant System
IRQ 101	Microsoft ACPI-Compliant System
IRQ 102	Microsoft ACPI-Compliant System
IRQ 103	Microsoft ACPI-Compliant System
IRQ 104	Microsoft ACPI-Compliant System
IRQ 105	Microsoft ACPI-Compliant System
IRQ 106	Microsoft ACPI-Compliant System
IRQ 107	Microsoft ACPI-Compliant System
IRQ 108	Microsoft ACPI-Compliant System
IRQ 109	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 110	Microsoft ACPI-Compliant System
IRQ 111	Microsoft ACPI-Compliant System
IRQ 112	Microsoft ACPI-Compliant System
IRQ 113	Microsoft ACPI-Compliant System
IRQ 114	Microsoft ACPI-Compliant System
IRQ 115	Microsoft ACPI-Compliant System
IRQ 116	Microsoft ACPI-Compliant System
IRQ 117	Microsoft ACPI-Compliant System
IRQ 118	Microsoft ACPI-Compliant System
IRQ 119	Microsoft ACPI-Compliant System
IRQ 120	Microsoft ACPI-Compliant System
IRQ 121	Microsoft ACPI-Compliant System
IRQ 122	Microsoft ACPI-Compliant System
IRQ 123	Microsoft ACPI-Compliant System
IRQ 124	Microsoft ACPI-Compliant System
IRQ 125	Microsoft ACPI-Compliant System
IRQ 126	Microsoft ACPI-Compliant System
IRQ 127	Microsoft ACPI-Compliant System
IRQ 128	Microsoft ACPI-Compliant System
IRQ 129	Microsoft ACPI-Compliant System
IRQ 130	Microsoft ACPI-Compliant System
IRQ 131	Microsoft ACPI-Compliant System
IRQ 132	Microsoft ACPI-Compliant System
IRQ 133	Microsoft ACPI-Compliant System
IRQ 134	Microsoft ACPI-Compliant System
IRQ 135	Microsoft ACPI-Compliant System
IRQ 136	Microsoft ACPI-Compliant System
IRQ 137	Microsoft ACPI-Compliant System
IRQ 138	Microsoft ACPI-Compliant System
IRQ 139	Microsoft ACPI-Compliant System
IRQ 140	Microsoft ACPI-Compliant System
IRQ 141	Microsoft ACPI-Compliant System
IRQ 142	Microsoft ACPI-Compliant System
IRQ 143	Microsoft ACPI-Compliant System
IRQ 144	Microsoft ACPI-Compliant System
IRQ 145	Microsoft ACPI-Compliant System
IRQ 146	Microsoft ACPI-Compliant System
IRQ 147	Microsoft ACPI-Compliant System
IRQ 148	Microsoft ACPI-Compliant System
IRQ 149	Microsoft ACPI-Compliant System
IRQ 150	Microsoft ACPI-Compliant System
IRQ 150	Trusted Platform Module 2.0
IRQ 151	Microsoft ACPI-Compliant System
IRQ 152	Microsoft ACPI-Compliant System
IRQ 153	Microsoft ACPI-Compliant System
IRQ 154	Microsoft ACPI-Compliant System
IRQ 155	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 156	Microsoft ACPI-Compliant System
IRQ 157	Microsoft ACPI-Compliant System
IRQ 158	Microsoft ACPI-Compliant System
IRQ 159	Microsoft ACPI-Compliant System
IRQ 160	Microsoft ACPI-Compliant System
IRQ 161	Microsoft ACPI-Compliant System
IRQ 162	Microsoft ACPI-Compliant System
IRQ 163	Microsoft ACPI-Compliant System
IRQ 164	Microsoft ACPI-Compliant System
IRQ 165	Microsoft ACPI-Compliant System
IRQ 166	Microsoft ACPI-Compliant System
IRQ 167	Microsoft ACPI-Compliant System
IRQ 168	Microsoft ACPI-Compliant System
IRQ 169	Microsoft ACPI-Compliant System
IRQ 170	Microsoft ACPI-Compliant System
IRQ 171	Microsoft ACPI-Compliant System
IRQ 172	Microsoft ACPI-Compliant System
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IRQ 174	Microsoft ACPI-Compliant System
IRQ 175	Microsoft ACPI-Compliant System
IRQ 176	Microsoft ACPI-Compliant System
IRQ 177	Microsoft ACPI-Compliant System
IRQ 178	Microsoft ACPI-Compliant System
IRQ 179	Microsoft ACPI-Compliant System
IRQ 180	Microsoft ACPI-Compliant System
IRQ 181	Microsoft ACPI-Compliant System
IRQ 182	Microsoft ACPI-Compliant System
IRQ 183	Microsoft ACPI-Compliant System
IRQ 184	Microsoft ACPI-Compliant System
IRQ 185	Microsoft ACPI-Compliant System
IRQ 186	Microsoft ACPI-Compliant System
IRQ 187	Microsoft ACPI-Compliant System
IRQ 188	Microsoft ACPI-Compliant System
IRQ 189	Microsoft ACPI-Compliant System
IRQ 190	Microsoft ACPI-Compliant System
IRQ 191	Microsoft ACPI-Compliant System
IRQ 192	Microsoft ACPI-Compliant System
IRQ 193	Microsoft ACPI-Compliant System
IRQ 194	Microsoft ACPI-Compliant System
IRQ 195	Microsoft ACPI-Compliant System
IRQ 196	Microsoft ACPI-Compliant System
IRQ 197	Microsoft ACPI-Compliant System
IRQ 198	Microsoft ACPI-Compliant System
IRQ 199	Microsoft ACPI-Compliant System
IRQ 200	Microsoft ACPI-Compliant System
IRQ 201	Microsoft ACPI-Compliant System
IRQ 202	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 203	Microsoft ACPI-Compliant System
IRQ 204	Microsoft ACPI-Compliant System
IRQ 256	Microsoft ACPI-Compliant System
IRQ 257	Microsoft ACPI-Compliant System
IRQ 258	Microsoft ACPI-Compliant System
IRQ 259	Microsoft ACPI-Compliant System
IRQ 260	Microsoft ACPI-Compliant System
IRQ 261	Microsoft ACPI-Compliant System
IRQ 262	Microsoft ACPI-Compliant System
IRQ 263	Microsoft ACPI-Compliant System
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IRQ 300	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 301	Microsoft ACPI-Compliant System
IRQ 302	Microsoft ACPI-Compliant System
IRQ 303	Microsoft ACPI-Compliant System
IRQ 304	Microsoft ACPI-Compliant System
IRQ 305	Microsoft ACPI-Compliant System
IRQ 306	Microsoft ACPI-Compliant System
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IRQ 347	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 348	Microsoft ACPI-Compliant System
IRQ 349	Microsoft ACPI-Compliant System
IRQ 350	Microsoft ACPI-Compliant System
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IRQ 390	Microsoft ACPI-Compliant System
IRQ 391	Microsoft ACPI-Compliant System
IRQ 392	Microsoft ACPI-Compliant System
IRQ 393	Microsoft ACPI-Compliant System
IRQ 394	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 395	Microsoft ACPI-Compliant System
IRQ 396	Microsoft ACPI-Compliant System
IRQ 397	Microsoft ACPI-Compliant System
IRQ 398	Microsoft ACPI-Compliant System
IRQ 399	Microsoft ACPI-Compliant System
IRQ 400	Microsoft ACPI-Compliant System
IRQ 401	Microsoft ACPI-Compliant System
IRQ 402	Microsoft ACPI-Compliant System
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IRQ 407	Microsoft ACPI-Compliant System
IRQ 408	Microsoft ACPI-Compliant System
IRQ 409	Microsoft ACPI-Compliant System
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IRQ 411	Microsoft ACPI-Compliant System
IRQ 412	Microsoft ACPI-Compliant System
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IRQ 438	Microsoft ACPI-Compliant System
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IRQ 440	Microsoft ACPI-Compliant System
IRQ 441	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 442	Microsoft ACPI-Compliant System
IRQ 443	Microsoft ACPI-Compliant System
IRQ 444	Microsoft ACPI-Compliant System
IRQ 445	Microsoft ACPI-Compliant System
IRQ 446	Microsoft ACPI-Compliant System
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IRQ 460	Microsoft ACPI-Compliant System
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IRQ 470	Microsoft ACPI-Compliant System
IRQ 471	Microsoft ACPI-Compliant System
IRQ 472	Microsoft ACPI-Compliant System
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IRQ 474	Microsoft ACPI-Compliant System
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IRQ 476	Microsoft ACPI-Compliant System
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IRQ 479	Microsoft ACPI-Compliant System
IRQ 480	Microsoft ACPI-Compliant System
IRQ 481	Microsoft ACPI-Compliant System
IRQ 482	Microsoft ACPI-Compliant System
IRQ 483	Microsoft ACPI-Compliant System
IRQ 484	Microsoft ACPI-Compliant System
IRQ 485	Microsoft ACPI-Compliant System
IRQ 486	Microsoft ACPI-Compliant System
IRQ 487	Microsoft ACPI-Compliant System
IRQ 488	Microsoft ACPI-Compliant System

Table D.2: Interrupt Assignments	
IRQ 489	Microsoft ACPI-Compliant System
IRQ 490	Microsoft ACPI-Compliant System
IRQ 491	Microsoft ACPI-Compliant System
IRQ 492	Microsoft ACPI-Compliant System
IRQ 493	Microsoft ACPI-Compliant System
IRQ 494	Microsoft ACPI-Compliant System
IRQ 495	Microsoft ACPI-Compliant System
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IRQ 497	Microsoft ACPI-Compliant System
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IRQ 501	Microsoft ACPI-Compliant System
IRQ 502	Microsoft ACPI-Compliant System
IRQ 503	Microsoft ACPI-Compliant System
IRQ 504	Microsoft ACPI-Compliant System
IRQ 505	Microsoft ACPI-Compliant System
IRQ 506	Microsoft ACPI-Compliant System
IRQ 507	Microsoft ACPI-Compliant System
IRQ 508	Microsoft ACPI-Compliant System
IRQ 509	Microsoft ACPI-Compliant System
IRQ 510	Microsoft ACPI-Compliant System
IRQ 511	Microsoft ACPI-Compliant System
IRQ 4294967290	PCI Express Root Port
IRQ 4294967289	PCI Express Root Port
IRQ 4294967279	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967278	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967277	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967276	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967275	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967274	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967273	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967272	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 0	System timer
IRQ 4294967293	PCI Express Root Port
IRQ 44	Tiered Memory Page Migration
IRQ 10	AMD I2C Controller
IRQ 11	AMD I2C Controller
IRQ 14	AMD I2C Controller
IRQ 15	AMD I2C Controller

D.3 1st MB Memory Map

Table D.3: 1st MB Memory Map

Addr. Range (Hex)	Device
0xCB500000-0xCB5007FF	Standard SATA AHCI Controller
0xCB500000-0xCB5007FF	PCI Express Root Port
0xFED81500-0xFED818FF	AMD GPIO Controller
0xBA300000-0xBA3FFFFF	AMD USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
0xBA300000-0xBA3FFFFF	PCI Express Root Port
0x80F00000-0x80FFFFFF	PCI Express Root Port
0xCA000000-0xCB0FFFFF	PCI Express Root Port
0xCA000000-0xCB0FFFFF	PCI Express Root Complex
0xCA000000-0xCB0FFFFF	Microsoft Basic Display Adapter
0x0000-0x11FFFFFF	PCI Express Root Port
0x0000-0x11FFFFFF	Microsoft Basic Display Adapter
0xBA100000-0xBA1FFFFF	Intel(R) Ethernet Controller I226-LM
0xBA200000-0xBA203FFF	Intel(R) Ethernet Controller I226-LM
0x0000-0xFFFFFFF	System board
0xA0000-0xBFFFF	PCI Express Root Complex
0xC0000-0xDFFFF	PCI Express Root Complex
0xBA000000-0xBA3FFFFF	PCI Express Root Complex
0xBA000000-0xBA3FFFFF	PCI Express Root Port
0x20F00000-0x20FFFFFF	PCI Express Root Port
0xCB200000-0xCB4FFFFF	PCI Express Root Port
0x12100000-0x121FFFFF	PCI Express Root Port
0xCB300000-0xCB3FFFFF	AMD USB 3.10 extensible Host Controller - 1.20 (Microsoft)
0xFED40000-0xFED44FFF	Trusted Platform Module 2.0
0xB9410500-0xB94FFFFF	Tiered Memory Page Migration
0xFEDC2000-0xFEDC2FFF	AMD I2C Controller
0xFEDC3000-0xFEDC3FFF	AMD I2C Controller
0xFEDC6000-0xFEDC6FFF	AMD I2C Controller
0xFEDCB000-0xFEDCBFFF	AMD I2C Controller
0xFEDC0000-0xFEDC0FFF	Motherboard resources
0xFEE00000-0xFEE00FFF	Motherboard resources
0xFED80000-0xFED814FF	Motherboard resources
0xFED81900-0xFED8FFFF	Motherboard resources
0xFEC10000-0xFEC10FFF	Motherboard resources
0xFF000000-0xFFFFFFFF	Motherboard resources
0x10000000-0x11FFFFFF	Microsoft Basic Display Adapter
0xCB0FC000-0xCB0FFFFF	High Definition Audio Controller

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Please verify specifications before quoting. This guide is intended for reference purposes only.