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Industrial DRAM module

i-DIMM
INDUSTRIAL DRAM MODULE

Approval Sheet

Customer	
Product Number	**M2SK-2GHJ5C06-A (2GB)**
Module speed	**PC2-6400**
Pin	**200 Pin**
CL-tRCD-TRP	**6-6-6**
SDRAM Operating Temp	**0**°C ~ **85**°C
Date	**21st October 2010**

Approval by Customer

P/N:

Signature:

Date:

Sales: **Sr.Technical Manager: John Hsieh**

i-DIMM

1. Features

Key Parameter

Industry Nomenclature	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
	CL=4	CL=5	CL=6			
PC2-5300	533	667	800	15	15	60

- JEDEC Standard 200-pin Dual In-Line Memory Module
- Intend for 800 Mbps applications
- Inputs and Outputs are SSTL-18 compatible
- VDD=VDDQ= 1.8 Volt ± 0.1
- Differential clock input
- All inputs are sampled at the positive going edge of the system clock
- Bi-Directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge.
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Automatic and controlled precharge commands.
- 14/10/1 Addressing (row/column/rank)-2GB
- Auto & self refresh 7.8μs ($T_A \leq +85°C$)
- Gold Contact
- DRAM Operation Temperature *(Note 1)*
  - $0°C \leq T_A \leq +85°C$
- Programmable Device Operation:
  - Burst Type: Sequential or Inteleave
  - Operation: Burst Read and Write
  - Device CAS# Latency: 6
  - Burst Length: 4, 8
- RoHS Compliant *(Section 15)*

Note:*1. The refresh rate is required to double when T_C exceeds 85°C.*

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +60	°C	3
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	1
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR2 DRAM component specification..

3. Ordering Information

SODIMM						
Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC
M2SK-2GHJ5C06-A	2GB	PC2-6400	256M x8	8	1	N/A

i-DIMM

4. Pin Configurations (Front side/Back side)

–x64 SODIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	101	A1	26	DM1	126	DQ37	51	DQS2	151	DQ42	76	DQ31	176	DQ55
2	V_{SS}	102	A0	27	V_{SS}	127	V_{SS}	52	DM2	152	DQ46	77	V_{SS}	177	V_{SS}
3	V_{SS}	103	V_{DD}	28	V_{SS}	128	V_{SS}	53	V_{SS}	153	DQ43	78	V_{SS}	178	V_{SS}
4	DQ4	104	V_{DD}	29	/DQS1	129	/DQS4	54	V_{SS}	154	DQ47	79	CKE0	179	DQ56
5	DQ0	105	A10/AP	30	CK0	130	DM4	55	DQ18	155	V_{SS}	80	NC/CKE1	180	DQ60
6	DQ5	106	BA1	31	DQS1	131	DQS4	56	DQ22	156	V_{SS}	81	V_{DD}	181	DQ57
7	DQ1	107	BA0	32	/CK0	132	V_{SS}	57	DQ19	157	DQ48	82	V_{DD}	182	DQ61
8	V_{SS}	108	/RAS	33	V_{SS}	133	V_{SS}	58	DQ23	158	DQ52	83	NC [2]	183	V_{SS}
9	V_{SS}	109	/WE	34	V_{SS}	134	DQ38	59	V_{SS}	159	DQ49	84	NC [3]	184	V_{SS}
10	DM0	110	/S0	35	DQ10	135	DQ34	60	V_{SS}	160	DQ53	85	NC [3]	185	DM7
11	/DQS0	111	V_{DD}	36	DQ14	136	DQ39	61	DQ24	161	V_{SS}	86	NC [3]	186	/DQS7
12	V_{SS}	112	V_{DD}	37	DQ11	137	DQ35	62	DQ28	162	V_{SS}	87	V_{DD}	187	V_{SS}
13	DQS0	113	/CAS	38	DQ15	138	V_{SS}	63	DQ25	163	NC,TEST	88	V_{DD}	188	DQS7
14	DQ6	114	ODT0	39	V_{SS}	139	V_{SS}	64	DQ29	164	CK1	89	A12	189	DQ58
15	V_{SS}	115	NC [4]	40	V_{SS}	140	DQ44	65	V_{SS}	165	V_{SS}	90	A11	190	V_{SS}
16	DQ7	116	NC [4]	41	V_{SS}	141	DQ40	66	V_{SS}	166	/CK1	91	A9	191	DQ59
17	DQ2	117	V_{DD}	42	V_{SS}	142	DQ45	67	DM3	167	/DQS6	92	A7	192	DQ62
18	V_{SS}	118	V_{DD}	43	DQ16	143	DQ41	68	/DQS3	168	V_{SS}	93	A8	193	V_{SS}
19	DQ3	119	NC [4]	44	DQ20	144	V_{SS}	69	NC [1]	169	DQS6	94	A6	194	DQ63
20	DQ12	120	NC [4]	45	DQ17	145	V_{SS}	70	DQS3	170	DM6	95	V_{DD}	195	SDA
21	V_{SS}	121	V_{SS}	46	DQ21	146	/DQS5	71	V_{SS}	171	V_{SS}	96	V_{DD}	196	V_{SS}
22	DQ13	122	V_{SS}	47	V_{SS}	147	DM5	72	V_{SS}	172	V_{SS}	97	A5	197	SCL
23	DQ8	123	DQ32	48	V_{SS}	148	DQS5	73	DQ26	173	DQ50	98	A4	198	SA0
24	V_{SS}	124	DQ36	49	/DQS2	149	V_{SS}	74	DQ30	174	DQ54	99	A3	199	V_{DDSPD}
25	DQ9	125	DQ33	50	/Event	150	V_{SS}	75	DQ27	175	DQ51	100	A2	200	SA1

NC = No Connect, RFU = Reserved for Future Use
1. Pin69 is optional /Reset
2. Pin83 is optional /S2
3. Pin84(85 & 86) is optional /A15(/BA2 & A14)
4. Pin115(116, 119 & 120) is optional /S1(/A13, ODT1 & /S3)

5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	CK0 - CK2 CK0# - CK2#	SDRAM Clocks
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS#	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS#	SDRAM column address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
WE#	SDRAM write enable	V_{DD}	Power (1.8V)
S0# - S1#	DIMM Rank Select Lines	V_{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V_{REF}	SDRAM I/O Reference supply
ODT0, ODT1	Active termination control lines	V_{SS}	Ground
DQ0 – DQ63	DIMM memory data bus	V_{DDSPD}	Serial EEPROM positive power supply
CB0 – CB7	DIMM ECC check bit	NC	Spare Pin
DQS0 – DQS8 DQS0# - DQS8#	SDRAM data strobes	Reset	NOT use on UDIMM
DM0 – DM8	SDRAM data masks/high data strobe (x8 base x72 bit module use only)		

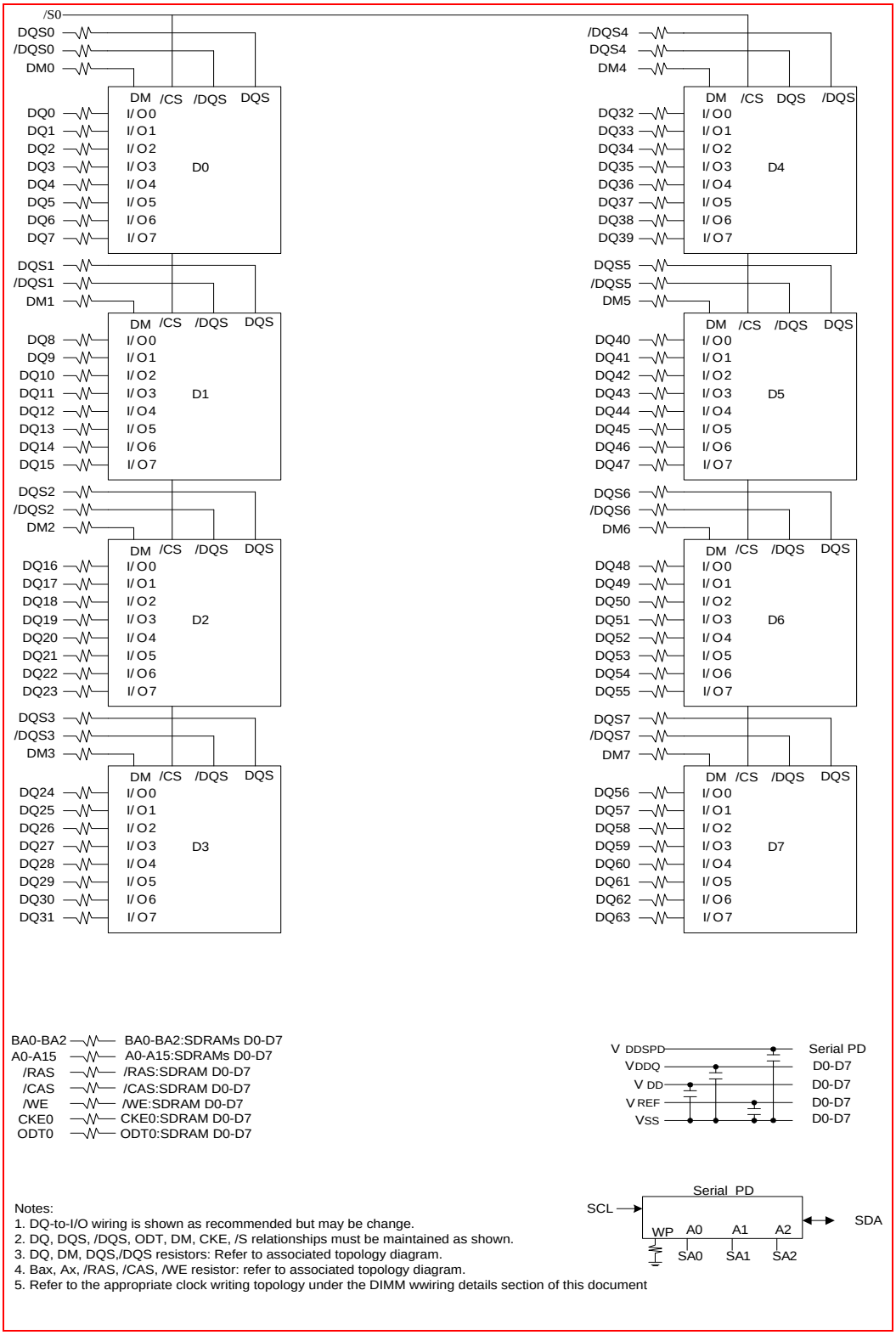
6. Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
CK0#, CK1#, CK2#	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CKE0#, CKE1#	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, RAS#, CAS#, WE# define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 – A9 A10/AP A11 – A13	(SSTL)	-	During a Bank Activate command cycle, A0-A14 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic

DQS0 – DQS8 DQS0# – DQS8#	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
SA0 – SA2	-	-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA	-	-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL	-	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply.

7. Function Block Diagram:

- 2GB SODIMM (1 Rank, x8 DDR2 base SDRAM Module)



Notes:
1. DQ-to-I/O wiring is shown as recommended but may be change.
2. DQ, DQS, /DQS, ODT, DM, CKE, /S relationships must be maintained as shown.
3. DQ, DM, DQS,/DQS resistors: Refer to associated topology diagram.
4. Bax, Ax, /RAS, /CAS, /WE resistor: refer to associated topology diagram.
5. Refer to the appropriate clock writing topology under the DIMM wwiring details section of this document

8. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to 2.3	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +2.3	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.5 to +2.3	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

9. AC & DC Operating Conditions

- AC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

Symbol	Parameter	Value	Units	Notes
VREF	Input Reference Voltage	0.5 * VDDQ	V	1
VSWING (MAX)	Input signal maximum peak to peak swing	1.7	V	1
SLEW	Input signal minimum slew rate	0	V	2,3
VIH (AC)	Input High (Logic1) Voltage	VREF + 0.125	V	
VIL (AC)	Input Low (Logic0) Voltage	-0.3	V	

Note::

1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(AC) min for rising edges and the range from VREF to VIL(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(AC) to VIH(AC) on the positive transitions and VIH(AC) to VIL(AC) on the negative transitions.

- SDRAM DC operating Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 85	°C	1,2

Note:

1. Case temperature is measured at top and center side of any DRAMs.
2. t_{CASE} > 85°C ➔ t_{REFI} = 3.9 µs All DRAM specification only support 0°C < t_{CASE} < 85°C

- DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

Symbol	Parameter	Min	Max	Units	Notes
VDD	Supply Voltage	1.7	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.9	V	1
VDDQ	I/O Supply Voltage	1.7	1.9	V	1
VREF	I/O Reference Voltage	0.49VDDQ	0.51VDDQ	V	1, 2
VTT	Termination Voltage	VREF-0.04	VREF+0.04	V	31
VIH (DC)	Input High (Logic1) Voltage	VREF + 0.125	VDDQ + 0.3	V	1
VIL (DC)	Input Low (Logic0) Voltage	-0.3	VREF - 0.125	V	1

Note:

1. Inputs are not recognized as valid until VREF stabilizes.
2. VREF is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
3. VTT of transmitting device must track VREF of receiving device.

10. Operating, Standby, and Refresh Currents

- 2GB SODIMM (1Ranks, 256Mx8 DDR2 SDRAMs T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.8V ± 0.1V)

Symbol	Parameter/Condition	PC2-6400	Unit
I_{DD0}	Operating Current: one bank; active/precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1200	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; tRC = tRC (MIN); CL=2.5; tCK = tCK (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle	1360	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ VIL (MAX); tCK = tCK (MIN)	160	mA
I_{DD2N}	Idle Standby Current: CS ≥ VIH (MIN); all banks idle; CKE ≥ VIH (MIN); tCK = tCK (MIN); address and control inputs changing once per clock cycle	720	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; is HIGH; CKE is HIGH; t_{CK} = $t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	520	mA
I_{DD3PF}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	400	mA
I_{DD3PS}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	200	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ VIH (MIN); CKE ≥ VIH (MIN); tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	880	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; tCK = tCK (MIN)	2880	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; tCK = tCK (MIN); IOUT = 0mA	1720	mA
I_{DD5}	Auto-Refresh Current: tRC = tRFC (MIN)	2880	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	160	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; tRC = tRC (min); IOUT = 0mA.	3600	mA

11. AC Timing Specifications

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	PC2-6400		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.40	+0.40	ns
tDQSCK	DQS output access time from CK/CK#	-0.35	+0.35	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	tCH or tCL	-	tCK
tCK	Clock Cycle Time	2.5	8	ns
tDS	DQ and DM input setup time(differential data strobe)	0.05	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.125	-	ns
tIPW	Input pulse width	0.6	-	tCK
tDIPW	DQ and DM input pulse width (each input)	0.35	-	tCK
tHZ	Data-out high-impedance time from CK, /CK	-	tACmax	ns
tLZ(DQS)	DQS low-impedance time from CK, /CK	tACmin	tACmax	ns
tLZ(DQ)	DQ low-impedance time from CK, /CK	$2t_{AC}$ min	t_{AC} max	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.20	ns
tQHS	Data hold Skew Factor	-	0.30	ns
tQH	Data output hold time from DQS	tHP - tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	-0.25	+0.25	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.2	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.2	-	tCK
tMRD	Mode register set command cycle time	2	-	tCK

t_{WPST}	Write postamble	0.40	0.60	t_{CK}
t_{WPRE}	Write preamble	0.35	-	t_{CK}
t_{IH}	Address and control input hold time	250	-	ps
t_{IS}	Address and control input setup time	175	-	ps
t_{RPRE}	Read preamble	0.90	1.10	t_{CK}
t_{RPST}	Read postamble	0.40	0.60	t_{CK}
t_{RRD}	Active bank A to Active bank B command	7.5	-	ns
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	$t_{IS} + t_{CK} + t_{IH}$	-	ns
t_{REFI}	Average Periodic Refresh Interval ($85ºC < T_{CASE} \leq 95ºC$)	3.9		µs
	Average Periodic Refresh Interval ($0ºC \leq T_{CASE} \leq 85ºC$)	7.8		µs
t_{OIT}	OCD drive mode output delay	0	12	ns
t_{CCD}	/CAS to /CAS delay	2		t_{CK}
t_{WR}	Write recovery time without Auto-Precharge	15	-	ns
WR	Write recovery time with Auto-Precharge	t_{WR}/t_{CK}	-	t_{CK}
t_{DAL}	Auto precharge write recovery + precharge time	$WR+t_{RP}$	-	t_{CK}
t_{WTR}	Internal write to read command delay	7.5	-	ns
t_{RTP}	Internal read to precharge command delay	7.5		ns
t_{XSNR}	Exit self refresh to a Non-read command	$t_{RFC}+10$		ns
t_{XSRD}	Exit self refresh to a Read command	200		t_{CK}
t_{XP}	Exit precharge power down to any Non- read command	2	-	t_{CK}
t_{XARD}	Exit active power down to read command	2	-	t_{CK}
t_{XARDS}	Exit active power down to read command	8-AL		t_{CK}
t_{CKE}	CKE minimum pulse width	3		t_{CK}

Symbol	Parameter	PC2-6400		Unit
		Min.	Max.	
tAOND	ODT turn-on delay	2	2	tCK
tAON	ODT turn-on	tAC (min)	tAC (max) +0.7	ns
tAONPD	ODT turn-on (Power down mode)	tAC (min) +2	2tCK + tAC(max) +1	ns
tAOFD	ODT turn-off delay	2.5	2.5	tCK
tAOF	ODT turn-off	tAC(min)	tAC(max) +0.6	ns
tAOFPD	ODT turn-off (Power down mode)	tAC (min)+2	2.5tCK + tAC(max) +1	ns
tANPD	ODT to power down entry latency	3		tCK
tAXPD	ODT power down exit latency	8		tCK

12. Speed Grade Definition

Symbol	Parameter	PC2-6400		Unit
		Min	Max	
tRAS	Row Active Time	45	70,000	ns
tRC	Row Cycle Time	60	-	ns
tRCD	RAS to CAS delay	15	-	ns
tRP	Row Precharge Time	15	-	ns

13. SPD
Serial Presence Detect – Part 1

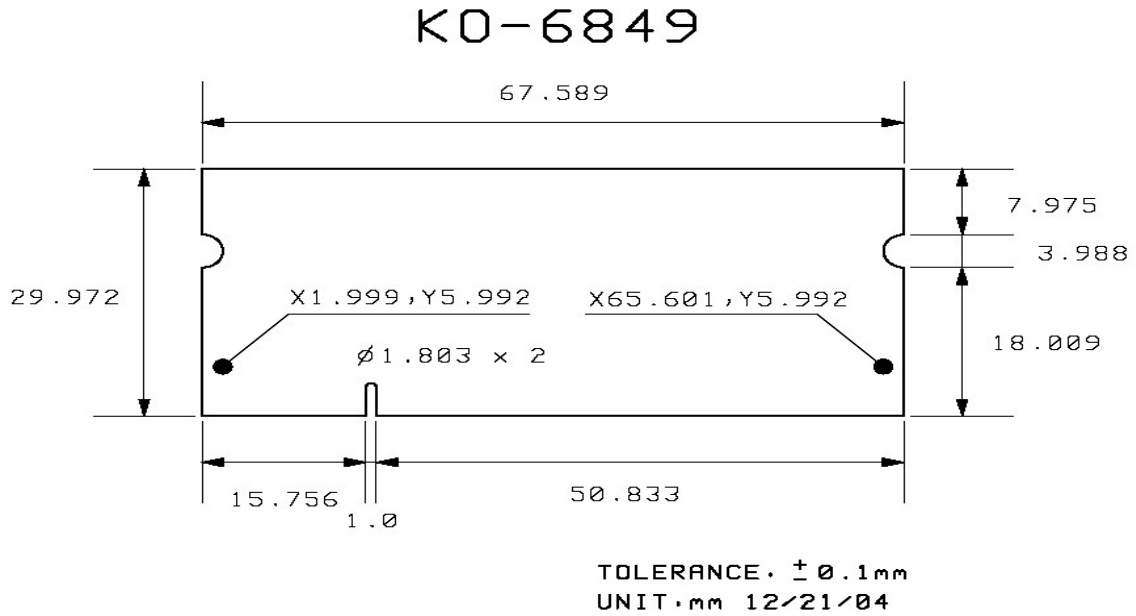
Byte	Description	M2SK-2GHJ5C06-A	Note
0	Number of Serial PD Bytes Written during Production	80	
1	Total Number of Bytes in Serial PD device	08	
2	Fundamental Memory Type	08	
3	Number of Row Addresses on Assembly	0E	
4	Number of Column Addresses on Assembly	0A	
5	Number of DIMM Bank, Package, and Height	60	
6	Data Width of this Assembly	40	
7	Reserved	00	
8	Voltage Interface Level of this Assembly	05	
9	DDR2 SDRAM Cycle Time at CL=5 (ns)	25	
10	DDR2 SDRAM Access Time from Clock at CL=5 (ns)	40	
11	DIMM Configuration Type	00	
12	Refresh Rate/Type	82	
13	Primary DDR2 SDRAM Width	08	
14	Error Checking DDR2 SDRAM Device Width	00	
15	Reserved	00	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	0C	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	08	
18	DDR2 SDRAM Device Attributes: /CAS Latencies Supported	70	
19	Reserved	01	
20	DDR2 SDRAM DIMM Type Information	04	
21	DDR2 SDRAM Module Attributes:	00	
22	DDR2 SDRAM Device Attributes: General	07	

Byte	Description	M2SK-2GHJ5C06-A	
23	Minimum Clock Cycle at CL=4	30	
24	Maximum Data Access Time (t_{ac}) from Clock at CL=4 (ns)	45	
25	Minimum Clock Cycle Time at CL=3 (ns)	3D	
26	Maximum Data Access Time (t_{ac}) from Clock at CL=3 (ns)	50	
27	Minimum Row Precharge Time (t_{RP}) (ns)	3C	
28	Minimum Row Active to Row Active delay (t_{RRD})	1E	
29	Minimum RAS to CAS delay (t_{RCD}) (ns)	3C	
30	Minimum RAS Pulse Width (t_{RAS})	2D	
31	Module Bank Density	01	
32	Address and Command Setup Time Before Clock (t_{IS}) (ns)	17	
33	Address and Command Hold Time After Clock (t_{IH}) (ns)	25	
34	Data Input Setup Time Before Clock (t_{DS})	05	
35	Data Input Hold Time After Clock (t_{DH}) (ns)	12	
36	Write Recovery Time (t_{WR})	3C	
37	Internal Write to Read Command delay (t_{WTR})	1E	
38	Internal Read to Precharge delay (t_{RTP})	1E	
39	Memory Analysis Probe Characteristics	00	
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	06	
41	Minimum Core Cycle Time (t_{RC}) (ns)	3C	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	7F	
43	Maximum Clock Cycle Time (t_{CK})	80	
44	Max. DQS-DQ Skew Factor (t_{DQS}) (ns)	14	
45	Read Data Hold Skew Factor (t_{QHS}) (ns)	1E	

Byte	Description	M2SK-2GHJ5C06-A	
46	PLL Relock Time	00	
47	Tcasemax DT4R4W Delta	00	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi-T-A DRAM)	00	
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	00	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	00	
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P)	00	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	00	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	00	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	00	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	00	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (ST5B)	00	
57	DRAM Case Temperature Rise from Ambient due to Bank interleave Reads with Auto-Precharge (DT7)	00	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00	

Byte	Description	M2SK-2GHJ5C06-A	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00	
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00	
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00	
62	SPD Reversion	12	
63	Checksum for byte 0-62	E2	
64-71	Manufacture's JEDEC ID Code	7F 7F 7F 7F 7F 7F F1 00	
72	Module Manufacturing Location	02	
73-91	Module Part number	69 2D 44 49 4D 4D FF 00 00 00 00 00 00 00 00 00 00	
92-255	Reserved	-	

14. Physical Dimension



15. RoHS Declaration

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Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M2SK-2GHJ5C06-A complies with the requirement of RoHS directives 2002/95/EC

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI（Cr+6）	< 1000 ppm
Polybromodiphenyl ether（PBDE）	< 1000 ppm
Polybrominated Biphenyls（PBB）	< 1000 ppm

Date issued : 2010/09/23

Manufacturer: : InnoDisk Co., Ltd.
Address : 9F, No. 100, Sec.1 Xintai 5th Rd., Xizhi City, Taipei 221, Taiwan

Authorized Signature :

QA Dept. Director - Terry Hsu

Revision Log

Rev	Date	Modification
0.1	27th May 2010	Preliminary Edition
1.0	9th Aug. 2010	Official Release
1.1	21st Oct. 2010	Added RoHS Declaration.