Approval Sheet

Customer	
Product Number	**ACT8GHR72P8J1333S**
Module speed	**PC3-10600**
Pin	**240pin**
Cl-tRCD-tRP	**9-9-9**
Date	**25th April 2016**

Approval by Customer

P/N:
Signature:
Date:

Sales: **Sr. Technical Manager: John Hsieh**

ACT8GHR72P8J1333S

8GB DDR3-1333 Registered ECC Module Specification

Description

ACTICA ACT8GHR72P8J1333S is a high speed 8GB DDR3-1333 Registered ECC DIMM. It is designed for mission critical application memory solution. This DIMM includes Error Checking and Correcting (ECC) for maximum reliability. The modules is constructed using 512Mx8 SDRAMs, and is fully compliant with JEDEC specifications. Decoupling capacitors are mounted on the PCB board for better signal integrity. The DIMM feature serial presence detect (SPD) based on a serial EEPROM device using the 2-pin I2C protocol.

Features

- 240-pin Registered Dual Inline Memory Module (RDIMM)
- Memory Module Organization 1Gx72
- Height: 30 mm
- CL-tRCD-tRP : 9-9-9
- JEDEC standard 1.5V (± 0.075V)
- VDDQ = 1.5V (± 0.075V)
- 8 independent internal bank
- Burst Length: 4, 8(Interleave/nibble sequential)
- Bi-directional Differential Data-Strobe
- On Die Termination (ODT)
- Eight-bit prefetch architecture
- Average Refresh Period 7.8us at lower than a T_{CASE} 85°C, 3.9us at 85°C < TCASE < 95 °C
- Programmable CAS Latency: 6,7,8,9
- RoHS Compliant

Address Range

Module Organization	Row address	Column Address	Bank Address	Auto Precharge
1Gx72	A0-A15	A0-A9	BA0-BA2	A10/AP

Pin Description

Pin Name	Description	Pin Name	Description
Ck0	Clock Input, positive line	Par_In	Parity bit for the Address and Control bus
CK0/	Clock Input, negative line	Err_Out	Parity error found on the Address and Control bus
		ODT[0]	On Die Termination Inputs
		DQ[63:0]	Data Input/Output
CKE[1:0]	Clock Enables	CB[7:0]	Data check bits Input/Output
TEST	Memory bus test toll (Not Connected and Not Usable on DIMMs)	DQS[8:0]	Data strobes
RAS/	Row Address Strobe	DQS/[8:0]	Data strobes, negative line
CAS/	Column Address Strobe	DM[8:0]/ DQS[17:9] TDQS[17:9]	Data Masks/ Data strobes, Termination data strobes
WE/	Write Enable	DQS/[17:9] TDQS/[17:9]	Data strobes, negative line, Termination data strobes
S[3:0]	Chip Selects	EVENT/	Reserved for optional hardware temperature sensing
		RESET/	Register and SDRAM control pin
A[9:0],A11, A[15:13]	Address Inputs	VDD	Power Supply
A10/AP	Address Input/Autoprecharge	VSS	Ground
A12/BC	Address Input/Burst chop	VREFDQ	Reference Voltage for DQ
BA[2:0]	SDRAM Bank Addresses	VREFCA	Reference Voltage for CA
SCL	Serial Presence Detect (SPD) Clock Input	VTT	Termination Voltage
SDA	SPD Data Input/Output	VDDSPD	SPD Power
SA[2:0]	SPD Address Inputs	RFU	Reserved for Future Use

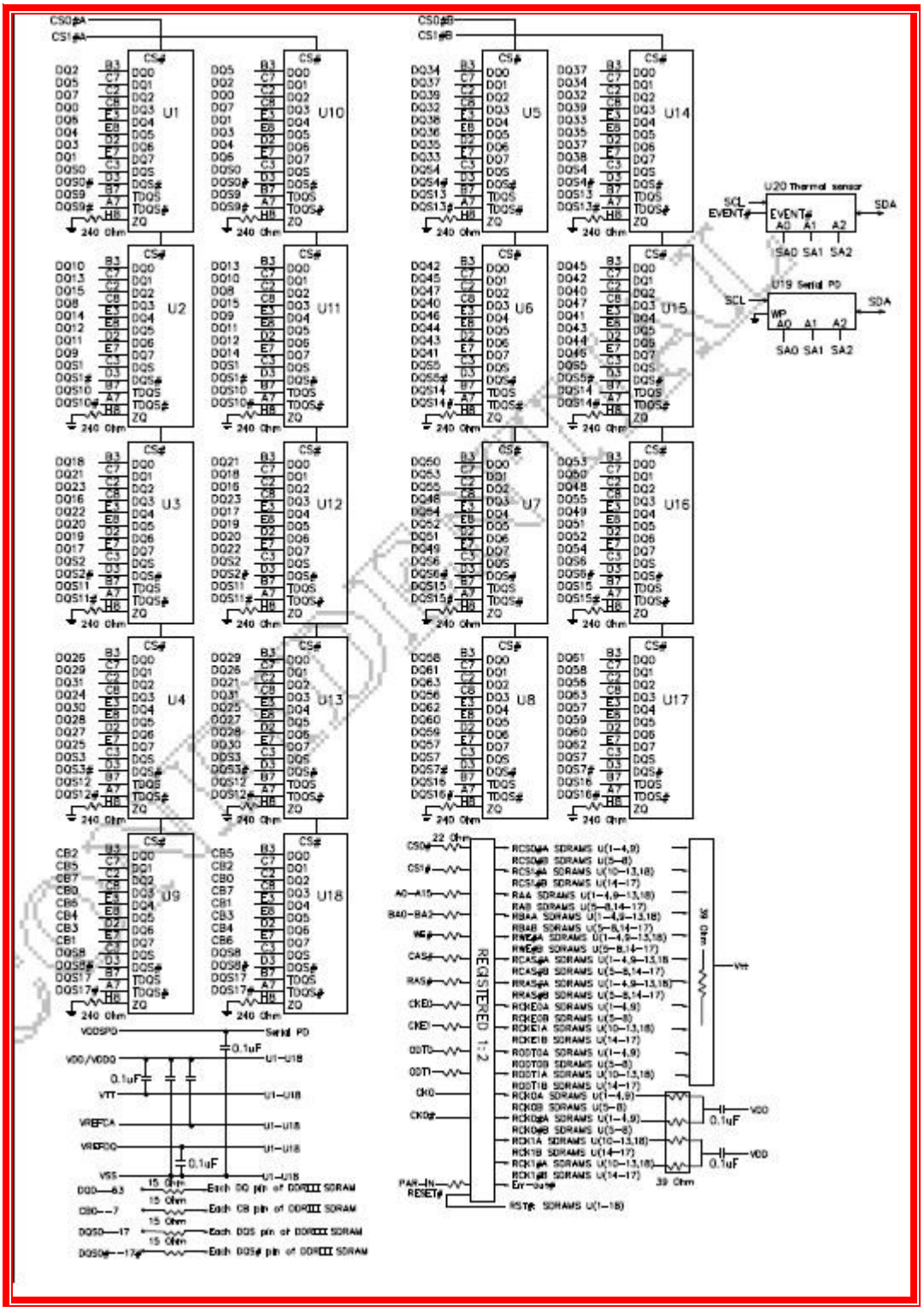
Pin Configuration (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	121	VSS	31	DQ25	151	VSS	60	VDD	180	A3	91	DQ41	211	VSS
2	VSS	122	DQ4	32	VSS	152	DM3,DQS12,TDQS12	61	A2	181	A1	92	VSS	212	DM5,DQS14,TDQS14
3	DQ0	123	DQ5	33	/DQS3	153	NC,DQS12,/TDQS12	62	VDD	182	VDD	93	/DQS5	213	NC,DQS14,/TDQS14
4	DQ1	124	VSS	34	DQS3	154	VSS	63	NC,CK1	183	VDD	94	DQS5	214	VSS
5	VSS	125	DM0,DQS9,TDQS9	35	VSS	155	DQ30	64	NC,/CK1	184	CK0	95	VSS	215	DQ46
6	/DQS0	126	NC,DQS9,/TDQS9	36	DQ26	156	DQ31	65	VDD	185	/CK0	96	DQ42	216	DQ47
7	DQS0	127	VSS	37	DQ27	157	VSS	66	VDD	186	VDD	97	DQ43	217	VSS
8	VSS	128	DQ6	38	VSS	158	CB4,NC	67	VREFCA	187	/EVENT,NC	98	VSS	218	DQ52
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC	68	NC/PAR_IN	188	A0	99	DQ48	219	DQ53
10	DQ3	130	VSS	40	CB0,NC	160	VSS	69	VDD	189	VDD	100	DQ49	220	VSS
11	VSS	131	DQ12	41	VSS	161	DM8,DQS17,TDQS17,NC	70	A10/AP	190	BA1	101	VSS	221	DM6,DQS15,TDQS15
12	DQ8	132	DQ13	42	/DQS8	162	NC,DQS17,/TDQS17	71	BA0	191	VDD	102	/DQS6	222	NC,DQS15,/TDQS15
13	DQ9	133	VSS	43	DQS8	163	VSS	72	VDD	192	/RAS	103	DQS6	223	VSS
14	VSS	134	DM1,DQS10,TDQS10	44	VSS	164	CB6,NC	73	/WE	193	/S0	104	VSS	224	DQ54
15	/DQS1	135	NC,DQS10,/TDQS10	45	CB2,NC	165	CB7,NC	74	/CAS	194	VDD	105	DQ50	225	DQ55
16	DQS1	136	VSS	46	CB3,NC	166	VSS	75	VDD	195	ODT0	106	DQ51	226	VSS
17	VSS	137	DQ14	47	VSS	167	NC(TEST)	76	/S1,NC	196	A13	107	VSS	227	DQ60
18	DQ10	138	DQ15	48	VTT,NC	168	/RESET	77	ODT1,NC	197	VDD	108	DQ56	228	DQ61
19	DQ11	139	VSS			KEY		78	VDD	198	/S3,NC	109	DQ57	229	VSS
20	VSS	140	DQ20	49	VTT,NC	169	CKE1,NC	79	/S2,NC	199	VSS	110	VSS	230	DM7,DQS16,TDQS16
21	DQ16	141	DQ21	50	CKE0	170	VDD	80	VSS	200	DQ36	111	/DQS7	231	DM7,DQS16,/TDQS16
22	DQ17	142	VSS	51	VDD	171	NC	81	DQ32	201	DQ37	112	DQS7	232	VSS
23	VSS	143	DM2,DQS11,TDQS11	52	BA2	172	A14	82	DQ33	202	VSS	113	VSS	233	DQ62
24	/DQS2	144	NC,DQS11,/TDQS11	53	/ERR_OUT/NC	173	VDD	83	VSS	203	DM4,DQS13,TDQS13	114	DQ58	234	DQ63
25	DQS2	145	VSS	54	VDD	174	A12 / /BC	84	/DQS4	204	NC,DQS13,/TDQS13	115	DQ59	235	VSS
26	VSS	146	DQ22	55	A11	175	A9	85	DQS4	205	VSS	116	VSS	236	VDDSPD
27	DQ18	147	DQ23	56	A7	176	VDD	86	VSS	206	DQ38	117	SA0	237	SA1
28	DQ19	148	VSS	57	VDD	177	A8	87	DQ34	207	DQ39	118	SCL	238	SDA
29	VSS	149	DQ28	58	A5	178	A6	88	DQ35	208	VSS	119	SA2	239	VSS
30	DQ24	150	DQ29	59	A4	179	VDD	89	VSS	209	DQ44	120	VTT	240	VTT
								90	DQ40	210	DQ45				

Ordering Information

DDR3 RDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
ACT8GHR72P8J1333S	8GB	PC3-10600	1Gx72	18	2	Y

Block Diagram



IDD Specification Parameter

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions	Value	Units
IDD0	**Operating one bank active-precharge current;** CKE: High; External clock: On; tCK, nRC, nRAS, CL; BL: 8[a]; AL: 0; CS: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling ; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details	522	mA
IDD1	**Operating one bank active-read-precharge current;** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL; BL: 8[a]; AL: 0; CS: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling ; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0;	720	mA
IDD2P0	**Precharge power-down current;** CKE: Low; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO:MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit	198	mA
IDD2P1	**Precharge power-down current;** CKE: Low; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO:MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit	198	mA
IDD2Q	**Precharge quiet standby current;** CKE: High; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	216	mA
IDD2N	**Precharge standby current;** CKE: High; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	234	mA
IDD3P	**Active power-down current;** CKE: Low; External clock: On; tCK, CL: AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO:MID-LEVEL;DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	198	mA
IDD3N	**Active standby current;** CKE: High; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	378	mA
IDD4W	**Operating burst write current;** CKE: High; External clock: On; AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	1170	mA
IDD4R	**Operating burst read current;** CKE: High; External clock: On; AL: 0; CS: High between RD; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM:stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	1170	mA
IDD5B	**Burst refresh current;** CKE: High; External clock: On; AL: 0; CS: High between REF; Command, Address, Bank Address Inputs: partially toggling ; Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	3600	mA
IDD6	**Self refresh current;** TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled[d]; Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and CK: LOW; AL: 0; CS, Command, Address, Bank Address, Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: MID-LEVEL	270	mA
IDD7	**Operating bank interleave read current;** CKE: High; External clock: On; AL: CL-1; CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM:stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	2358	mA
IDD8	**RESET Low Current** RESET : Low; External clock : off; CK and CK : LOW; CKE : FLOATING ; CS, Command, Address, Bank Address, Data IO : FLOATING ; ODT Signal : FLOATING	270	mA

Absolute Maximum DC ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4V ~ 1.975V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4V ~ 1.975V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4V ~ 1.975V	V	1
T_{STG}	Storage Temperature	-55 ~ +100	^{0}C	1, 2

Note:
1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3) 3. VDD and VDDQ must be within 300mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

AC and DC Operating Conditions

Recommended DC Operating Conditions (SSTL - 1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1,2

Note :
1) Under all conditions VDDQ must be less than or equal to VDD.
2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Input/Output Capacitance

Symbol	Parameter	Max.	Units
C_{CK}	Input capacitance, CK and /CK	1.4	pF
C_I	Input capacitance (All other input only pins)	1.2	
C_{ZQ}	Input/output capacitance of ZQ pin	3	
C_{IO}	Input/output capacitance (DQ, DM, DQS, /DQS, TDQS, /TDQS)	2.2	

Timing Parameters

(TCASE = 0 °C ~ 70 °C; VDDQ = VDD , See AC Characteristics)

Symbol	Parameter	PC3-10600		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.5	3.3	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-80	80	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-70	70	Ps
JIT (CC)	Cycle to Cycle Period Jitter	160		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	140		Ps
TJIT (duty)		-	-	Ps
TERR (2per)	Cumulative error across 2 cycle	-118	118	Ps
TERR (3per)	Cumulative error across 3 cycle	-140	140	Ps
TERR (4per)	Cumulative error across 4 cycle	-155	155	Ps
TERR (5per)	Cumulative error across 5 cycle	-168	168	Ps
TERR (6per)	Cumulative error across 6 cycle	-177	177	Ps
TERR (7per)	Cumulative error across 7 cycle	-186	186	Ps
TERR (8per)	Cumulative error across 3 cycle	-193	193	Ps
TERR (9per)	Cumulative error across 4 cycle	-200	200	Ps

TERR (10per)	Cumulative error across 5 cycle	-205	205	Ps
TERR (11per)	Cumulative error across 6 cycle	-210	210	Ps
TERR (12per)	Cumulative error across 7 cycle	-215	215	Ps
TERR (nper)	Cumulative error across 13~50 cycle	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		Ps
Data Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDSQ	DQS, DQS# to DQ skew, per group, per access	-	125	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-500	250	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	250	Ps
tDS(base) AC150	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	30	-	Ps
tDH(base) DC 100	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	65	-	Ps
Data Strobe Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)

tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps
tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.4	0.6	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.4	0.6	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.25	0.25	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.2	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.2	-	tCK(avg)
Command and Address Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			

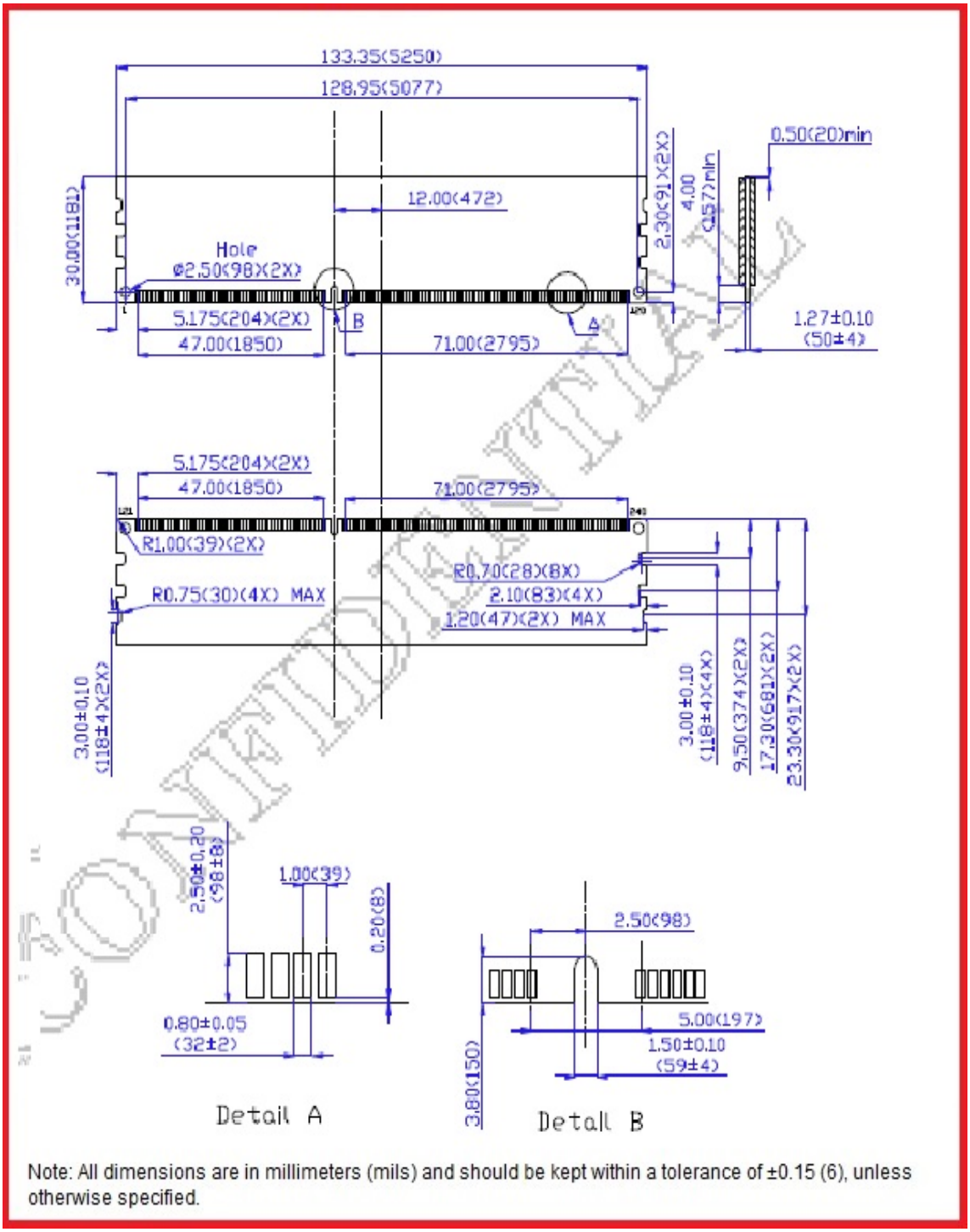
tCCD		4	-	nCK
tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	36	9 tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4 nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4 nCK, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	45	-	ns
tIS (base)	Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	65		ns
tIH(base)	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	140		ps
tIS(base) AC150	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	65+125		ps
Calibration Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tZQinit	Power-up and RESET calibration time	512	-	nCK
tZQoper	Normal operation Full calibration time	256	-	nCK
tZQCS	Normal operation Short calibration time	64	-	nCK
Reset Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXPR	Exit Reset from CKE HIGH to a valid command	max(5 nCK,tRFC(min) +10ns)	-	

Self Refresh Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5 nCK), tRFC(min)+ 10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE 9min) +1nC K	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5 nCK,1 0ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5 nCK,1 0ns)	-	
Power Down Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3 nC K, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(1 0nCK CK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3 nC K,5ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCK(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK

tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD (min)	-	nCK
ODT Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	1	9	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	1	9	ns
tAON	RTT-turn-on	-250	250	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)

Write Leveling Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	195	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	195	-	ps
tWLO	Write leveling output delay	0	9	ns
tWLOE	Write leveling output error	0	2	ns

Physical Dimension (drawing not in scale) Units : in Millimeters



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI（Cr+6）	< 1000 ppm
Polybromodiphenyl ether（PBDE）	< 1000 ppm
Polybrominated Biphenyls（PBB）	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Richard Lee 李鐘亮

Company Representative Title 公司代表人職稱： CEO 執行長

Date 日期： 2014 / 07 / 29

(Company Stamp/公司大小章)

SPD

Byte	Function Described	Data (HEX)
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	92
1	SPD Revision	13
2	Key Byte / DRAM Device Type	0B
3	Key Byte / Module Type	01
4	SDRAM Density and Banks	04
5	SDRAM Addressing	21
6	Module Nominal Voltage, VDD	00
7	Module Organization	09
8	Module Memory Bus Width	0B
9	Fine Timebase (FTB) Dividend / Divisor	11
10	Medium Timebase (MTB) Dividend	01
11	Medium Timebase (MTB) Divisor	08
12	SDRAM Minimum Cycle Time (tCKmin)	0C
13	Reserved	00
14	CAS Latencies Supported, Least Significant Byte	3C
15	CAS Latencies Supported, Most Significant	00
16	Minimum CAS Latency Time (tAAmin)	69
17	Minimum Write Recovery Time (tWRmin)	78
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	30
20	Minimum Row Precharge Delay Time (tRPmin)	69
21	Upper Nibbles for tRAS and tRC	11
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	20
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	89
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	20
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	08
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	3C
28	Upper Nibble for tFAW	00
29	Minimum Four Activate Window Delay Time (tFAWmin)	F0
30	SDRAM Optional Features	83
31	SDRAM Thermal and Refresh Options	01
32	Module Thermal Sensor	80
33	SDRAM Device Type	00
34	Fine Offset for SDRAM Minimum Cycle Time (tCKmin)	00
35	Fine Offset for Minimum CAS Latency Time (tAAmin)	00
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)	00
37	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	00
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	00
39~40	Reserved, General Section	00
41	SDRAM Maximum Activate Count (MAC) Value	88

42~59	Reserved, General Section	00
60	Module Nominal Height	0F
61	Module Maximum Thickness	11
62	Reference Raw Card Used	21
63	Address Mapping from Edge Connector to DRAM	05
64	RDIMM Thermal Heat Spreader Solution	00
65	Register Manufacturer ID Code, Least Significant Byte	04
66	Register Manufacturer ID Code, Most Significant Byte	B3
67	Register Revision Number	21
68	Register Type	00
69	RC1 (MS Nibble) / RC0 (LS Nibble)	00
70	RC3 (MS Nibble) / RC2 (LS Nibble) - Drive Strength, Command/Address	50
71	RC5 (MS Nibble) / RC4 (LS Nibble) - Drive Strength, Control and Clock	00
72	RC7 (MS Nibble) / RC6 (LS Nibble)	00
73	RC9 (MS Nibble) / RC8 (LS Nibble)	00
74	RC11 (MS Nibble) / RC10 (LS Nibble)	00
75	RC13 (MS Nibble) / RC12 (LS Nibble)	00
76	RC15 (MS Nibble) / RC14 (LS Nibble)	00
77-116	Reserved	00
117~118	Module ID: Module Manufacturer's JEDEC ID Code	06 F1
119	Module ID: Module Manufacturing Location	-
120~121	Module ID: Module Manufacturing Date	-
122~125	Module ID: Module Serial Number	-
126~127	Cyclical Redundancy Code	36 F7
128~145	Module Part Number	-
146~147	Module Revision Code	-
148~149	DRAM Manufacturer's JEDEC ID Code	-
150-175	Manufacturer's Specific Data	-
176-255	Open for customer use	-