規格書
SPECIFICATION

品名
STYLE NAME ： SWITCHING POWER SUPPLY

型號
MODEL NO. ： P1H-5500G

料號
PART NO. ：

版次
REVISION ： A1

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Revision

Rev.	Page	Item	Date	Description

MODEL NO. P1H-5500G

1.0 Scope

This specification defines the performance characteristics of a grounded, AC input,500 watts，5 output level power supply. This specification also defines world wide safety requirements and manufactures process test requirements.

2.0 Input requirements

2.1 Voltage (sinusoidal) : 100～240 VAC full range (With ±10% tolerance).

2.2 Frequency

The input frequency range will be 47hz～63hz.

2.3 Steady-state current

7A/3A at any low/high range input voltage.

2.4 Inrush current

40/60Amps @ 115/230 VAC (at 25 degrees ambient cold start)

2.5 Power factor correction

The power supply shall incorporate universal power input with active power factor correction, which shall reduce line harmonics in accordance with the IEC61000-3-2 standards.

PFC can reach the target of 90% @115VAC,Full load.

3.0 Output requirements

3.1 DC load requirements

Normal	Load current(A)		Regulation tolerance	
Output voltage	Min.	Max.	Max.	Min.
+5V	0.5A	18A	+5%	-5%
+12V	2A	40A	+5%	-5%
-12V	0A	0.5A	+5%	-5%
+3.3V	0.5A	18A	+5%	-5%
+5Vsb	0.1A	3A	+5%	-5%

* The output current of +5V and +3.3V not exceed 100W ***

*** Total power:500W

3.2 Regulation

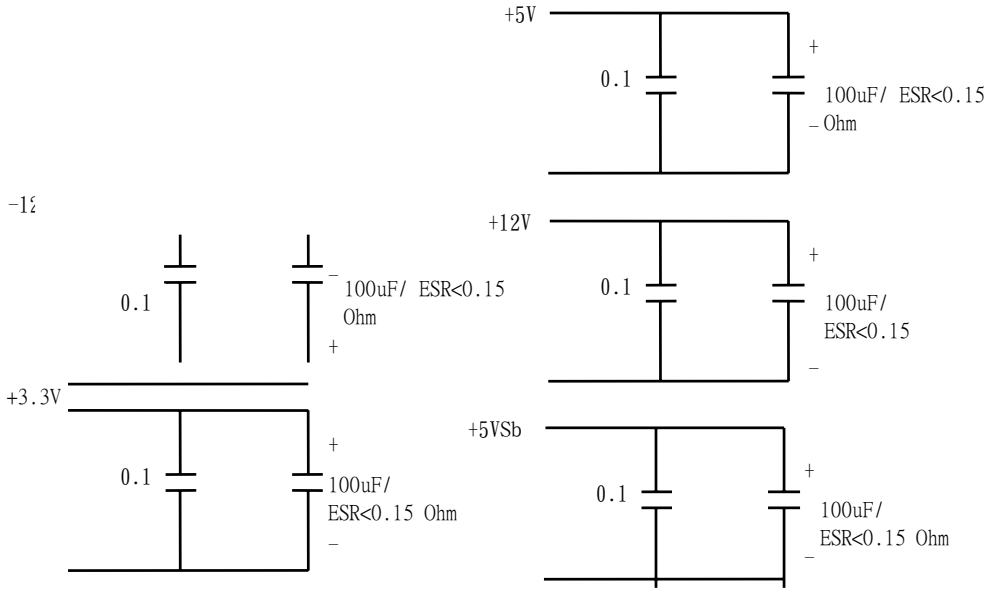
Output DC voltage	Line regulation
+5V	±50mV
+12V	±120mV
-12V	±120mV
+3.3V	±50mV
+5Vsb	±50mV

3.3 Ripple and noise

3.3.1 Specification

Parameter	Ripple	Ripple+Noise
+5V	50mV (P-P)	60mV (P-P)
+12V	120mV (P-P)	120mV (P-P)
-12V	120mV (P-P)	120mV (P-P)
+3.3V	50mV (P-P)	60mV (P-P)
+5Vsb	50mV (P-P)	60mV (P-P)

3.3.2 Ripple voltage test circuit



0.1uf is ceramic the other is tantalum.
Noise bandwidth is from DC to 20MHz

3.4 Overshoot

Any overshoot at turn on or turn off shall be less 10% of the nominal voltage value，all output shall be within the regulation limit of section 3.2 before issuing the power good signal of section 6.0.

3.5 Efficiency

Power supply efficiency typical >87% at 115V FULL LOAD
(Any difference either on the DC output cable (i.e., length, wire gauge) or on the accurate of instruments will conclude different test result.)

4.0 Protection

4.1 Input (primary)

The input power line must have an over power protection device in accordance with safety requirement of section 8.0

4.2 Output (secondary)

4.2.1 Over power protection

The power supply shall provide over power protection on the power supply latches all DC output into a shutdown state. Over power of this type shall cause no damage to power supply，after over load is removed and a power on/off cycle is initiated，the power supply will restart.

Trip point total power min. 110%，max. 160%.

4.2.2 Over voltage protection

If an over voltage fault occurs，the power supply will latch all DC output into a shutdown state.

	Min	Typical	Max
+3.3V	3.6V	4.1V	4.3V
+5V	5.6V	6.1V	6.5V
+12V	13.2V	14.3V	15.0V

4.2.3 Over current protection

If an over current fault occurs，the power supply will latch all DC output into a shutdown state.

	Min	Typical	Max
+3.3V	19.8A	22.5A	27A
+5V	19.8A	22.5A	27A
+12V	44A	52A	60A

4.2.4 Short circuit

A: A short circuit placed on any DC output to DC return shall cause no damage.

B: The power supply shall be latched in case any short circuit is taken place at +5V,+3.3V,+12V output.

C: The power supply shall be auto-recovered in case any short circuit is taken place at +5VSB.

5.0 Power supply sequencing

5.1 Power on (see Fig.1)

5.2 Hold up time

When AC source shutdown DC output must be maintain 16msec in regulation limit at. normal input voltage (AC115V)

5.3 Power off sequence (see Fig. 1)

6.0 Signal requirements

6.1 Power good signal (see Fig. 1)

The power supply shall provide a "power good" signal to reset system logic，indicate proper operation of the power supply.

At power on，the power good signal shall have a turn on delay of at least 100ms but not greater than 500ms after the output voltages have reached their respective minimum sense levels.

7.0 Environment

7.1 Temperature

Operating temperature: 0 to 50 degrees centigrade(90～264 VAC)

Non-Operating temperature: -20 to 80 degrees centigrade

7.2 Humidity

Operating humidity	20% to 80%
Non-operating humidity	10% to 90%

7.3 Insulation resistance

Primary to secondary	: 100 meg. Ohm min. 500 VDC
Primary to FG	: 100 meg. Ohm min. 500VDC

7.4 Dielectric withstanding voltage

Primary to secondary	: 3K VAC for 60 Second.
Primary to FG	: 1500 VAC for 60 Second.

7.5 Leakage current

3.5 mA max. at nominal voltage VAC

8.0 Safety

8.1 Underwriters laboratory (UL).

The power supply designed to meet UL 60950-1,2nd.

8.2 Canadian standards association (CUL)

The power supply designed to meet CSA 1402C & CSA 950.

8.3 TUV

The power supply shall be designed to meet TUV EN-60950.

8.4 CCC Standards

The power supply shall be designed to meet GB4943-1995,GB9254-1998, GB17625.1-1998.

9.0 Reliability

9.1 Burn in

All products shipped to customer must be processed by burn-in. The burn- in shall be performed for 1 hour at full load.

10.0 Mechanical requirements

10.1 Physical dimension : 225mm (D) x 100mm (W) x 40.5mm (H)

11.0 Output voltage Timing

Item	Description	MIN	MAX	UNITS
Tsb_on_delay	Delay from AC being applied to 5VSB being within regulation.		1500	ms
Tac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	ms
Tvout_holdup	Time all output voltages stay within regulation after loss of AC.	16		ms
Tpwok_holdup	Delay from loss of AC to deassertion of PWOK.	15		ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
Tpson_pwok	Delay from PSON# deactive to PWOK being deasserted.		50	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
Tpwok_off	Delay from PWOK deasserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		ms
Tsb_vout	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	5	1000	ms
Tsb_holdup	Time 5VSB output voltage stays within regulation after loss of AC.	70		ms
Tvout_rise	Output voltage rise time from each main output.	5	50	ms

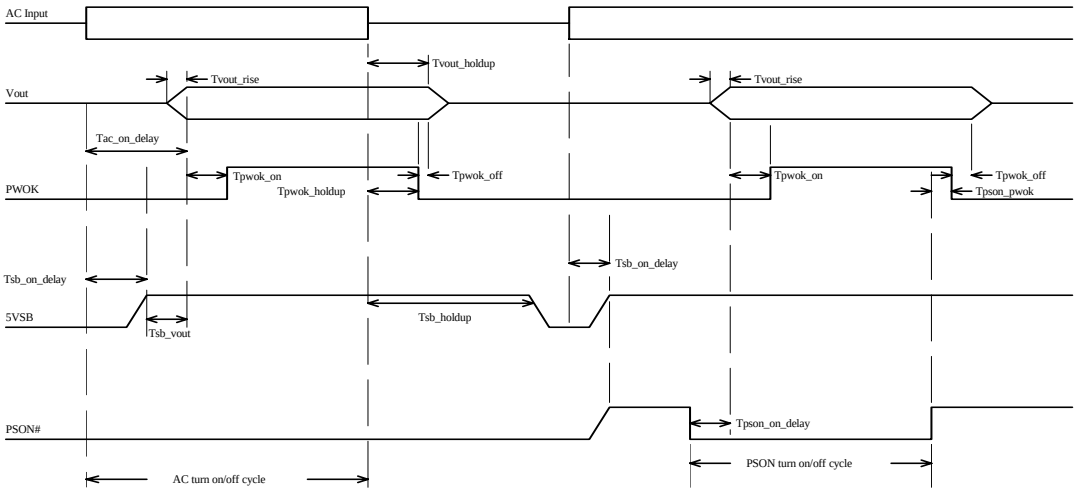


Fig.1