The Total Solution For Industrial Flash Storage

Customer	
Product Number	**M2CK-1GMFRC06-M**
Module speed	**PC2-6400**
Pin	**240 Pin**
CL-tRCD-tRP	**6-6-6**
Operating Temp	**0**°C **~ 85**°C
Date	**29th January 2018**

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=4	CL=5	CL=6			
PC2-6400	K	533	667	800	15	15	60

- JEDEC Standard 240-pin Dual In-Line Memory Module
- Intend for 400MHz applications
- Inputs and Outputs are SSTL-18 compatible
- VDD=VDDQ= 1.8 Volt ± 0.1
- Differential clock input
- All inputs are sampled at the positive going edge of the system clock
- Bi-Directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge.
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Automatic and controlled precharge commands.
- 14/10/1 Addressing (row/column/rank)-1GB
- Auto & self refresh 7.8μs ($T_C \leq +85°C$)
- ECC function
- Gold Plating Thickness 30μ"
- SDRAM Operation Temperature *(Note 1)*
  - $0°C \leq T_C \leq +85°C$
- Programmable Device Operation:
  - Burst Type: Sequential or Inteleave
  - Operation: Burst Read and Write
  - Device CAS# Latency: 4,5,6
  - Burst Length: 4, 8
- RoHS Compliant *(Section 14)*

Note:*1. The refresh rate is required to double when T_C exceeds 85°C.*

2. Environmental Requirements

DDR2 UDIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +55	°C	3
HOPR	Operating Humidity (relative)	10 to 90	%	
TSTG	Storage Temperature	-50 to +100	°C	1
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR2 DRAM component specification..
Following JEDEC specifications.

3. Ordering Information

DDR2 ECC UDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M2CK-1GMFRC06-M	1GB	PC2-6400	128M x72	9	1	Y

4. Pin Configurations (Front side/Back side)

–x72 UDIMM

Front								Back							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5
2	VSS	32	VSS	62	VDDQ	92	/DQS5	122	DQ4	152	DQ28	182	A3	212	NC
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	65	VSS	95	DQ42	125	DM0	155	DM3	185	CK0	215	DQ47
6	/DQS0	36	/DQS3	66	VSS	96	DQ43	126	NC	156	NC	186	/CK0	216	VSS
7	DQS0	37	DQS3	67	VDD	97	VSS	127	VSS	157	VSS	187	VDD	217	DQ52
8	VSS	38	VSS	68	NC	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	VSS
10	DQ3	40	DQ27	70	A10	100	VSS	130	VSS	160	VSS	190	BA1	220	CK2
11	VSS	41	VSS	71	BA0	101	SA2	131	DQ12	161	NC	191	VDDQ	221	/CK2
12	DQ8	42	NC	72	VDDQ	102	NC	132	DQ13	162	NC	192	/RAS	222	VSS
13	DQ9	43	NC	73	/WE	103	VSS	133	VSS	163	VSS	193	/S0	223	DM6
14	VSS	44	VSS	74	/CAS	104	/DQS6	134	DM1	164	NC	194	VDDQ	224	NC
15	/DQS1	45	NC	75	VDD	105	DQS6	135	NC	165	NC	195	ODT0	225	VSS
16	DQS1	46	NC	76	NC	106	VSS	136	VSS	166	VSS	196	NC/A13	226	DQ54
17	VSS	47	VSS	77	NC	107	DQ50	137	CK1	167	NC	197	VDD	227	DQ55
18	NC	48	NC	78	VDDQ	108	DQ51	138	/CK1	168	NC	198	VSS	228	VSS
19	NC	49	NC	79	VSS	109	VSS	139	VSS	169	VSS	199	DQ36	229	DQ60
20	VSS	50	VSS	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	NC	201	VSS	231	VSS
22	DQ11	52	CKE0	82	VSS	112	VSS	142	VSS	172	VDD	202	DM4	232	DM7
23	VSS	53	VDD	83	/DQS4	113	/DQS7	143	DQ20	173	NC	203	NC	233	NC
24	DQ16	54	NC/BA2	84	DQS4	114	DQS7	144	DQ21	174	NC/A14	204	VSS	234	VSS
25	DQ17	55	NC	85	VSS	115	VSS	145	VSS	175	VDDQ	205	DQ38	235	DQ62
26	VSS	56	VDDQ	86	DQ34	116	DQ58	146	DM2	176	A12	206	DQ39	236	DQ63
27	/DQS2	57	A11	87	DQ35	117	DQ59	147	NC	177	A9	207	VSS	237	VSS
28	DQS2	58	A7	88	VSS	118	VSS	148	VSS	178	VDD	208	DQ44	238	VDDSPD
29	VSS	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	VSS	240	SA1

Note:

1. Pin 196 is NC for 512MB, or A13 for 1GB.
2. Pin 54 is NC for 1GB; BA2 for 2GB, 4GB.
3. Pin 174 is NC for 1GB, 2GB; A14 for 4GB.

5. Architecture

Pin Definition

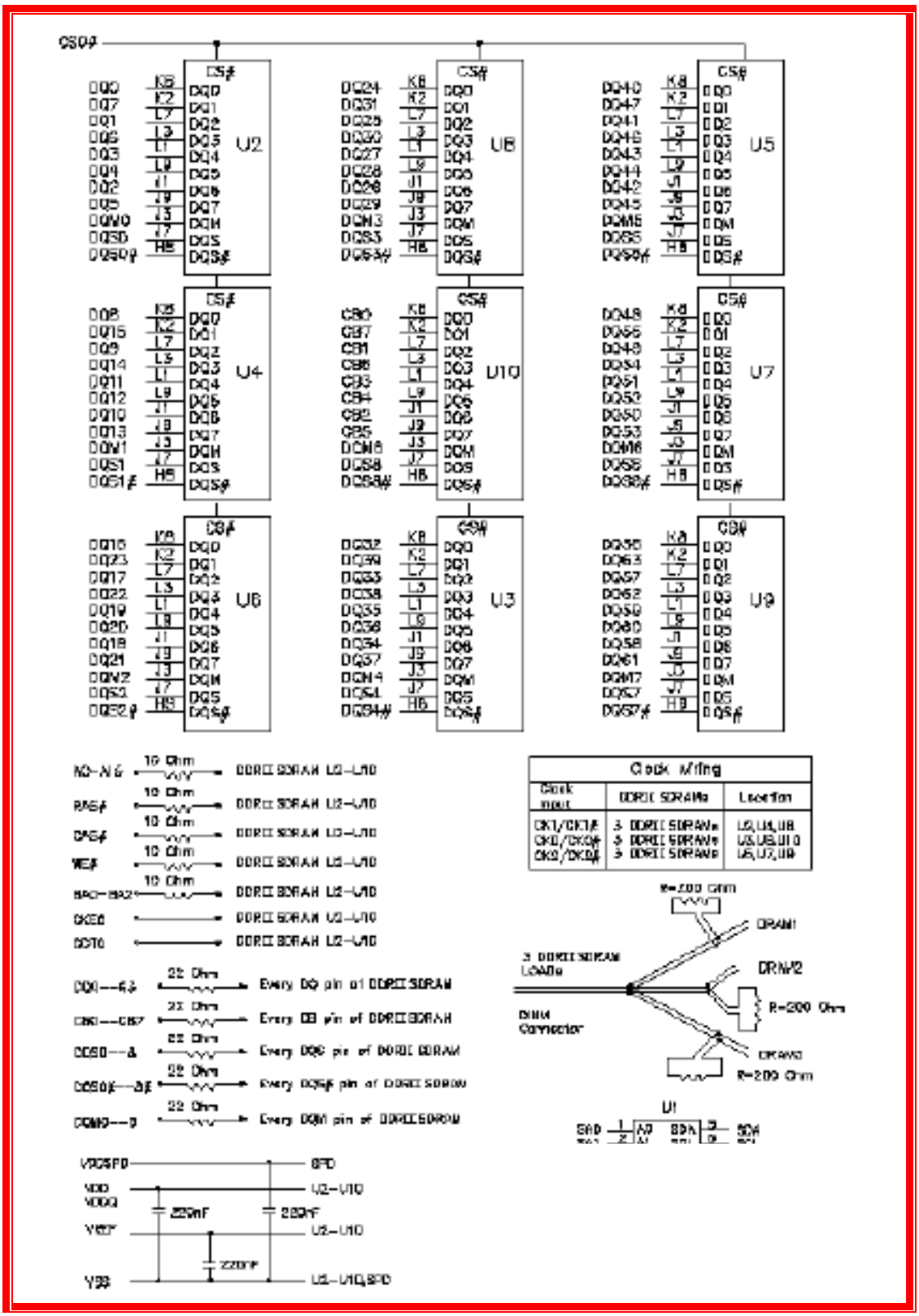
Pin Name	Description	Pin Name	Description
A0–A15	SDRAM address bus	CK0–CK2	SDRAM clocks (positive line of differential pair)
BA0–BA2	SDRAM bank select	/CK0–/CK2	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	SCL	I^2C serial bus clock for EEPROM
/CAS	SDRAM column address strobe	SDA	I^2C serial bus data line for EEPROM
/WE	SDRAM write enable	SA0-SA2	I^2C slave address select for EEPROM
/S0-/S1	DIMM Rank Select Lines	V_{DD}*	SDRAM core power supply
CKE0–CKE1	SDRAM clock enable lines	V_{DDQ}*	SDRAM I/O Driver power supply
ODT0–ODT1	On-die termination control lines	V_{REF}	SDRAM I/O reference supply
DQ0–DQ63	DIMM memory data bus	V_{SS}	Power supply return (ground)
CB0–CB7	DIMM ECC check bits	V_{DDSPD}	Serial EEPROM positive power supply
DQS0–DQS8	SDRAM data strobes (positive line of differential pair)	NC	Spare pins (no connect)
/DQS0–/DQS8	SDRAM data strobes (negative line of differential pair)	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
DM0–DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	RESET	Not used on UDIMM
*The V_{DD} and $V_{DD}Q$ pins are tied common to a single power-plane on these designs.			

6. Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0 - CK2 /CK0 - /CK2	SSTL	Differential crossing	CK and /CK are differential clock inputs. All the DDR2 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of /CK. Output (read) data is reference to the crossing of CK and /CK (Both directions of crossing)
CKE0 - CKE1	SSTL	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode
/S0 - /S1	SSTL	Active High	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks
/RAS, /CAS, /WE	SSTL	Active High	/RAS, /CAS, and /WE (ALONG WITH /S) define the command being entered.
ODT0 - ODT1	SSTL	Active High	When high, termination resistance is enabled for all DQ, DQS, /DQS and DM pins, assuming this function is enabled in the Extended Mode Register Set (EMRS).
V_{REF}	Supply		Reference voltage for SSTL18 inputs.
V_{DDQ}	Supply		Power supply for the DDR2 SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins.
BA0 - BA2	SSTL	—	Selects which SDRAM bank of eight is activated.
A0 - A15	SSTL		During a Bank Activate command cycle, Address input defines the row address (RA0-RA15) During a Read or Write command cycle, Address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled.During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	SSTL		Data and Check Bit Input/Output pins.
DM0 - DM8	SSTL	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR2 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules.
DQS0 - DQS8 /DQS0 - /DQS8	SSTL	Differential crossing	Data strobe for input and output data. For Rawcards using x16 organized DRAMs, DQ0-7 connect to the LDQS pin of the DRAMs and DQ8-15 connect to the UDQS pin of the DRAM
SA0 - SA2		—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor must be connected from the SDA bus line to V_{DDSPD} to act as a pullup on the system board.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to V_{DDSPD} to act as a pullup on the system board.
V_{DD}SPD	Supply		Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 1.7V to 3.6V.

7. Function Block Diagram:

- (1 Rank, 128Mx8 DDR2 base SDRAM Module)



8. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	NOTE
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-1.0V~2.3V	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.5V~2.3V	V	1
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	-0.5V~2.3V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5V~2.3V	V	1
T_{STG}	Storage Temperature	-55 to +100	℃	1,2

NOTE:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than 0.6 x V_{DDQ}. When V_{DD} and V_{DDQ} and V_{DDL} are less than 500mV, V_{REF} may be equal to or less than 300mV.
4. Voltage on any input or I/O may not exceed voltage on V_{DDQ}.

9. AC & DC Operating Conditions

9.1 Recommended DC operating Conditions

Symbol	Parameter	Rating			Units	NOTE
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	4
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	4
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1,2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

NOTE : There is no specific device V_{DD} supply voltage requirement for SSTL-1.8 compliance. However under all conditions V_{DDQ} must be less than or equal to VDD.

1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed +/-2% V_{REF}(DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

9.2 DRAM Operating Temperature Condition

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operating Temperature Range	Normal Temperature	0 to 85	°C	1,2

Note:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM.
2. T_{CASE} > 85°C ➔ T_{REFI} = 3.9µs. All DRAM specification only support 0°C < T_{CASE} < 85°C

9.3 Input DC / AC Logic Level

Symbol	Parameter	Min.	Max.	Units	Note
V_{IH}(DC)	DC input logic high	V_{REF}+0.125	V_{DDQ}+0.3	V	
V_{IL}(DC)	DC input logic low	-0.3	V_{REF}-0.125	V	
V_{IH}(AC)	AC input logic high	V_{REF}+0.200	-	V	1
V_{IL}(AC)	AC input logic low	-	V_{REF}-0.200	V	1

NOTE :

1. For information related to VPEAK value, Refer to overshoot/undershoot specification in device operation and timing datasheet; maximum peak amplitude allowed for overshoot and undershoot.

9.4 AC Input Test Conditions

Symbol	Condition	Value	Units	NOTE
V_{REF}	Input reference voltage	0.5*V_{DDQ}	V	1
V_{SWING}(MAX)	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2,3

NOTE:

1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}$(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(AC) min for rising edges and the range from V_{REF} to V_{IL}(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V_{IL}(AC) to V_{IH}(AC) on the positive transitions and V_{IH}(AC) to V_{IL}(AC) on the negative transitions.

10. Operating, Standby, and Refresh Currents

- 1GB ECC UDIMM(1Rank, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-6400	Unit
I_{DD0}	Operating Current: one bank; active/precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	585	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; tRC = tRC (MIN); CL=2.5; tCK = tCK (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle	675	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ VIL (MAX); tCK = tCK (MIN)	90	mA
I_{DD2N}	Idle Standby Current: CS ≥ VIH (MIN); all banks idle; CKE ≥ VIH (MIN); tCK = tCK (MIN); address and control inputs changing once per clock cycle	252	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; is HIGH; CKE is HIGH; $t_{CK} = t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	216	mA
I_{DD3PF}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	270	mA
I_{DD3PS}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	180	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ VIH (MIN); CKE ≥ VIH (MIN); tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	297	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; tCK = tCK (MIN)	1125	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; tCK = tCK (MIN); IOUT = 0mA	1080	mA
I_{DD5}	Auto-Refresh Current: tRC = tRFC (MIN)	1395	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	63	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; tRC = tRC (min); IOUT = 0mA.	1890	mA

11. AC Timing Specifications

Symbol	Parameter	PC2-6400		Unit
		Min.	Max.	
t_{AC}	DQ output access time from CK/CK#	-0.40	+0.40	ns
t_{DQSCK}	DQS output access time from CK/CK#	-0.35	+0.35	ns
t_{CH}	CK high-level width	0.48	0.52	t_{CK}
t_{CL}	CK low-level width	0.48	0.52	t_{CK}
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time	t_{CH} or t_{CL}	-	t_{CK}
t_{CK}	Clock Cycle Time	2.5	8	ns
t_{DS}	DQ and DM input setup time(differential data strobe)	0.05	-	ns
t_{DH}	DQ and DM input hold time(differential data strobe)	0.125	-	ns
t_{IPW}	Input pulse width	0.6	-	t_{CK}
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	-	t_{CK}
t_{HZ}	Data-out high-impedance time from CK/XK	-	t_{ACmax}	ns
$t_{LZ(DQS)}$	DQS low-impedance time from CK/XK	t_{ACmin}	t_{ACmax}	ns
$t_{LZ(DQ)}$	DQ low-impedance time from CK/XK	$2*t_{AC}$ min	t_{AC} max	ns
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	-	0.20	ns
t_{QHS}	Data hold Skew Factor	-	0.30	ns
t_{QH}	Data output hold time from DQS	t_{HP} - t_{QHS}	-	ns
t_{DQSS}	Write command to 1st DQS latching transition	-0.25	+0.25	t_{CK}
$t_{DQSL,(H)}$	DQS input low (high) pulse width (write cycle)	0.35	-	t_{CK}
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.2	-	t_{CK}
t_{MRD}	Mode register set command cycle time	2	-	t_{CK}
t_{WPST}	Write postamble	0.40	0.60	t_{CK}

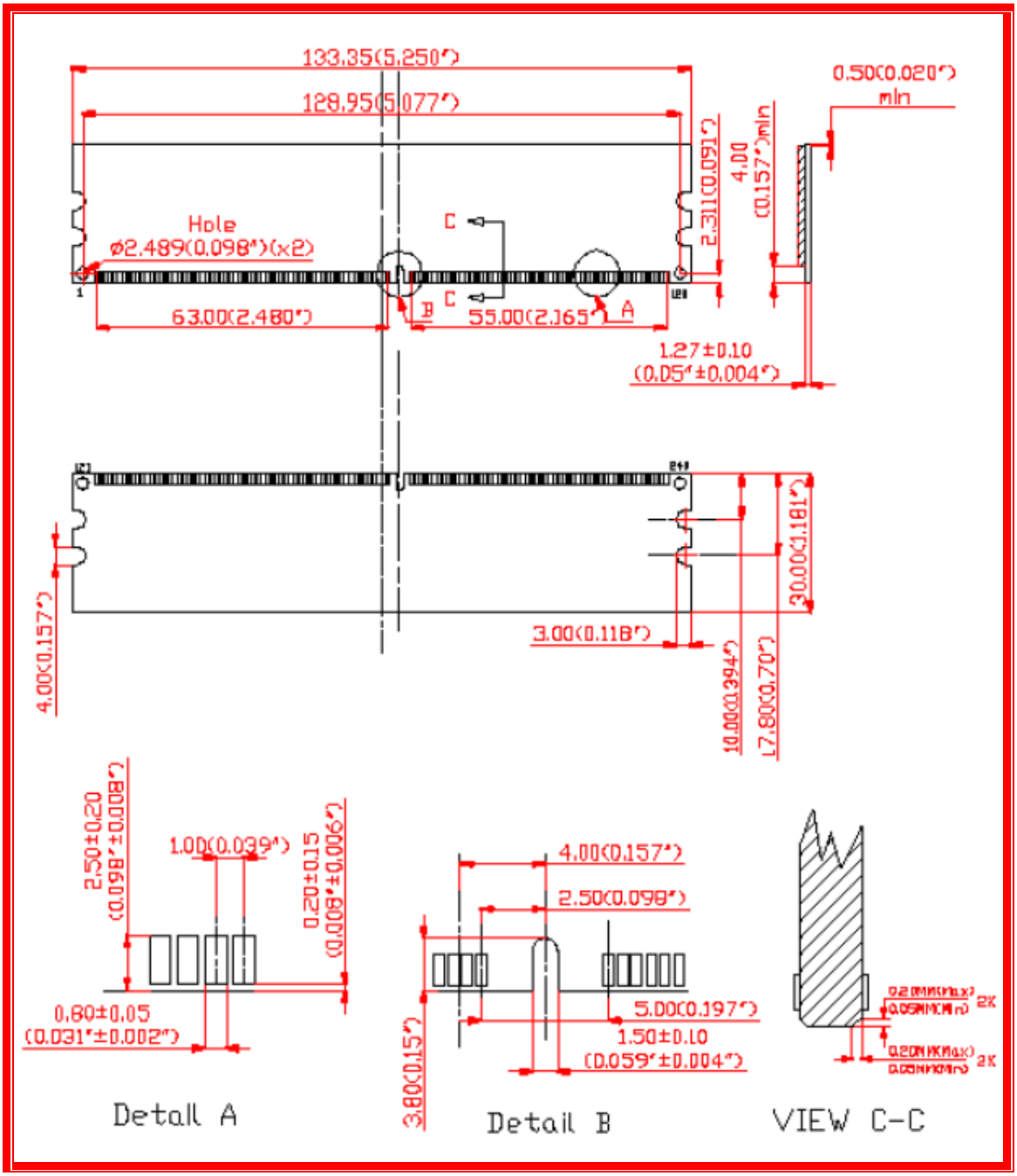
tWPRE	Write preamble	0.35	-	tCK
tIH	Address and control input hold time	250	-	Ps
tIS	Address and control input setup time	175	-	Ps
tRPRE	Read preamble	0.90	1.10	tCK
tRPST	Read postamble	0.40	0.60	tCK
tRRD	Active bank A to Active bank B command	7.5	-	Ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	tIS + tCK + tIH	-	Ns
tREFI	Average Periodic Refresh Interval ($85^oC < T_{CASE} \leq 95^oC$)	3.9		Ms
	Average Periodic Refresh Interval ($0^oC \leq T_{CASE} \leq 85^oC$)	7.8		Ms
tOIT	OCD drive mode output delay	0	12	Ns
tCCD	CAS# to CAS# delay	2		tCK
tWR	Write recovery time without Auto-Precharge	15	-	Ns
tDAL	Auto precharge write recovery + precharge time	WR+tRP	-	tCK
tWTR	Internal write to read command delay	7.5	-	Ns
tRTP	Internal read to precharge command delay	7.5		Ns
tXSNR	Exit self refresh to a Non-read command	tRFC+10		Ns
tXSRD	Exit self refresh to a Read command	200		tCK
tXP	Exit precharge power down to any Non- read command	2	-	tCK
tXARD	Exit active power down to read command	2	-	tCK
tXARDS	Exit active power down to read command	8-AL		tCK
tCKE	CKE minimum pulse width	3		tCK
tAOND	ODT turn-on delay	2	2	tCK
tAON	ODT turn-on	tAC (min)	tAC (max) +0.7	Ns
tAONPD	ODT turn-on (Power down mode)	tAC (min) +2	2tCK + tAC(max) +1	Ns

t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}
t_{AOF}	ODT turn-off	$t_{AC(min)}$	$t_{AC(max)}$ +0.6	Ns
t_{AOFPD}	ODT turn-off (Power down mode)	$t_{AC\ (min)}$+2	2.5t_{CK} + $t_{AC(max)}$ +1	Ns
t_{ANPD}	ODT to power down entry latency	3		t_{CK}
t_{AXPD}	ODT power down exit latency	8		t_{CK}

12. Speed Grade Definition

Symbol	Parameter	PC2-6400		Unit
		Min	Max	
t_{RAS}	Row Active Time	45	70,000	ns
t_{RC}	Row Cycle Time	60	-	ns
t_{RCD}	RAS to CAS delay	15	-	ns
t_{RP}	Row Precharge Time	15	-	ns

13. Physical Dimension



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified

14. RoHS Declaration

innodisk

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Innodisk Corporation

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RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯 (DEHP)	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯 (BBP)	< 1000 ppm
鄰苯二甲酸二丁酯 (DBP)	< 1000 ppm
鄰苯二甲酸二異丁酯 (DIBP)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2017 / 01 / 18

15. SPD

Byte	Function Described	Data (HEX)
0	Number of Serial PD Bytes	80
1	Total number of Bytes in Serial PD device	08
2	Memory Type	08
3	Number of Row Addresses on this assembly	0E
4	Number of Column Addresses on this assembly	0A
5	Number of DIMM Ranks	60
6	Data Width of this assembly	48
7	Reserved	00
8	Voltage Interface Level of this assembly	05
9	SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X	25
10	SDRAM Access from Clock	40
11	DIMM configuration type (Non-parity, Parity or ECC)	02
12	Refresh Rate/Type	82
13	Primary SDRAM Width	08
14	Error Checking SDRAM Width	08
15	Reserved	00
16	SDRAM Device Attributes: Burst Lengths Supported	0C
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	08
18	SDRAM Device Attributes: CAS Latency	70
19	DIMM Mechanical Characteristics	01
20	DIMM Type Information	02
21	SDRAM Module Attributes	00
22	SDRAM Device Attributes: General	07
23	Minimum Clock Cycle at CLX-1	30
24	Maximum Data Access Time (tAC) from Clock at CLX-1	45
25	Minimum Clock Cycle at CLX-2	3D
26	Maximum Data Access Time (tAC) from Clock at CLX-2	50
27	Minimum Row Precharge Time (tRP)	3C
28	Minimum Row Active to Row Active delay (tRRD)	1E
29	Minimum RAS to CAS delay (tRCD)	3C
30	Minimum Active to Precharge Time (tRAS)	2D
31	Module Rank Density	01
32	Address and Command Input Setup Time Before Clock (tIS)	17
33	Address and Command Input Hold Time After Clock (tIH)	25
34	Data Input Setup Time Before Strobe (tDS)	05

35	Data Input Hold Time After Strobe (tDH)	12
36	Write recovery time (tWR)	3C
37	Internal write to read command delay (tWTR)	1E
38	Internal read to precharge command delay (tRTP)	1E
39	Memory Analysis Probe Characteristics	00
40	Extension of Byte 41 tRC and Byte 42 tRFC	06
41	SDRAM Device Minimum Active to Active/Refresh Time (tRC)	3C
42	SDRAM Device Minimum Refresh to Active/Refresh Command Period (tRFC)	7F
43	SDRAM Device Maximum device cycle time (tCKmax)	80
44	SDRAM Device maximum skew between DQS and DQ signals (tDQSQ)	14
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	1E
46	PLL Relock Time	00
47	Tcasemax Delta	00
48	PSIT- A DRAM	00
49	DT0/MODE BITS	00
50	DT2N/DTQ	00
51	DT2P	00
52	DT3N	00
53	DT3Pfast	00
54	DT3Pslow	00
55	DT4R/Mode Bit	00
56	DT5B	00
57	DT7	00
58	PSIT- A PLL	00
59	PSIT-A REG	00
60	DT PLL ACTIVE	00
61	REGSTR ACTIVE/MODE BIT	00
62	SPD REVISION	13
63	CHECKSUM FOR BYTES 0 THRU 62	F3
64	MANUFACTURERS JEDEC ID CODE	7F
65~71	MANUFACTURERS JEDEC ID CODE (CONTINUED)	7F 7F 7F 7F 7F F1 00
72	MANUFACTURING LOCATION	02
73~90	Module Part Number	69 2D 44 49 4D 4D 20 20 20 20 20 20 20 20 20 20

91~92	Module Revision Code	-
93~94	Module Manufacturing Date	-
95~98	Module Serial Number	-
99~127	Manufacturer's Specific Data	-
128~255	Open for customer use	-

Revision Log

Rev	Date	Modification
0.1	29th January 2018	Preliminary Edition
1.0	29th January 2018	Official Release