Customer	
Product Number	**M2SK-1GMF5IJ5-M**
Module speed	**PC2-5300**
Pin	**200 Pin**
CL-tRCD-tRP	**5-5-5**
SDRAM Operating Temp	**-40**°C ~ **95**°C
Date	**9th May 2017**

Rev 1.0

The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
	CL=3	CL=4	CL=5			
PC2-5300	400	533	667	15	15	55

- JEDEC Standard 200-pin Dual In-Line Memory Module
- Intend for 333MHz applications
- Inputs and Outputs are SSTL-18 compatible
- VDD=VDDQ= 1.8 Volt ± 0.1
- Differential clock input
- All inputs are sampled at the positive going edge of the system clock
- Bi-Directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge.
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Automatic and controlled precharge commands.
- 14/10/1 Addressing (row/column/rank)-1GB
- Auto & self refresh 7.8μs (Tc ≤ +85°C)
- Golden Contactor
- SDRAM Operation Temperature
  - -40°C ≤ Tc ≤ +95°C
- Programmable Device Operation:
  - Burst Type: Sequential or Inteleave
  - Operation: Burst Read and Write
  - Device CAS# Latency: 3,4,5
  - Burst Length: 4, 8
- RoHS Compliant *(Section 15)*

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2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	-40 to +85	°C	3
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	1
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR2 DRAM component specification..

3. Ordering Information

W/T DDR2 SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M2SK-1GMF5IJ5-M	1GB	PC2-5300	128M x64	8	1	N/A

4. Pin Configurations (Front side/Back side)

–x64 SODIMM

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{REF}	2	V_{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V_{SS}	4	DQ4	53	V_{SS}	54	V_{SS}	103	V_{DD}	104	V_{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V_{SS}	156	V_{SS}
7	DQ1	8	V_{SS}	57	DQ19	58	DQ23	107	BA0	108	$\overline{RAS}$	157	DQ48	158	DQ52
9	V_{SS}	10	DM0	59	V_{SS}	60	V_{SS}	109	$\overline{WE}$	110	$\overline{S0}$	159	DQ49	160	DQ53
11	$\overline{DQS0}$	12	V_{SS}	61	DQ24	62	DQ28	111	V_{DD}	112	V_{DD}	161	V_{SS}	162	V_{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	$\overline{CAS}$	114	ODT0	163	NC,TEST	164	CK1
15	V_{SS}	16	DQ7	65	V_{SS}	66	V_{SS}	115	NC/ $\overline{S1}$	116	NC / A13	165	V_{SS}	166	$\overline{CK1}$
17	DQ2	18	V_{SS}	67	DM3	68	$\overline{DQS3}$	117	V_{DD}	118	V_{DD}	167	$\overline{DQS6}$	168	V_{SS}
19	DQ3	20	DQ12	69	**NC**	70	DQS3	119	NC / ODT1	120	**NC**	169	DQS6	170	DM6
21	V_{SS}	22	DQ13	71	V_{SS}	72	V_{SS}	121	V_{SS}	122	V_{SS}	171	V_{SS}	172	V_{SS}
23	DQ8	24	V_{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	V_{SS}	78	V_{SS}	127	V_{SS}	128	V_{SS}	177	V_{SS}	178	V_{SS}
29	$\overline{DQS1}$	30	CK0	79	CKE0	80	NC / CKE1	129	$\overline{DQS4}$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK0}$	81	V_{DD}	82	V_{DD}	131	DQS4	132	V_{SS}	181	DQ57	182	DQ61
33	V_{SS}	34	V_{SS}	83	**NC**	84	NC / A15	133	V_{SS}	134	DQ38	183	V_{SS}	184	V_{SS}
35	DQ10	36	DQ14	85	NC / BA2	86	NC / A14	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS7}$
37	DQ11	38	DQ15	87	V_{DD}	88	V_{DD}	137	DQ35	138	V_{SS}	187	V_{SS}	188	DQS7
39	V_{SS}	40	V_{SS}	89	A12	90	A11	139	V_{SS}	140	DQ44	189	DQ58	190	V_{SS}
41	V_{SS}	42	V_{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V_{SS}	193	V_{SS}	194	DQ63
45	DQ17	46	DQ21	95	V_{DD}	96	V_{DD}	145	V_{SS}	146	$\overline{DQS5}$	195	SDA	196	V_{SS}
47	V_{SS}	48	V_{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS2}$	50	**NC**	99	A3	100	A2	149	V_{SS}	150	V_{SS}	199	V_{DD}SPD	200	SA1

Note: NC = No Connect; NC,TEST(pin 163) is for bus analysis tool and is not connected on normal memory modules.

5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	CK0 - CK2 CK0# - CK2#	SDRAM Clocks
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS#	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS#	SDRAM column address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
WE#	SDRAM write enable	V_{DD}	Power (1.8V)
S0# - S1#	DIMM Rank Select Lines	V_{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V_{REF}	SDRAM I/O Reference supply
ODT0, ODT1	Active termination control lines	V_{SS}	Ground
DQ0 – DQ63	DIMM memory data bus	V_{DDSPD}	Serial EEPROM positive power supply
CB0 – CB7	DIMM ECC check bit	NC	Spare Pin
DQS0 – DQS8 DQS0# - DQS8#	SDRAM data strobes	Reset	NOT use on UDIMM
DM0 – DM8	SDRAM data masks/high data strobe (x8 base x72 bit module use only)		

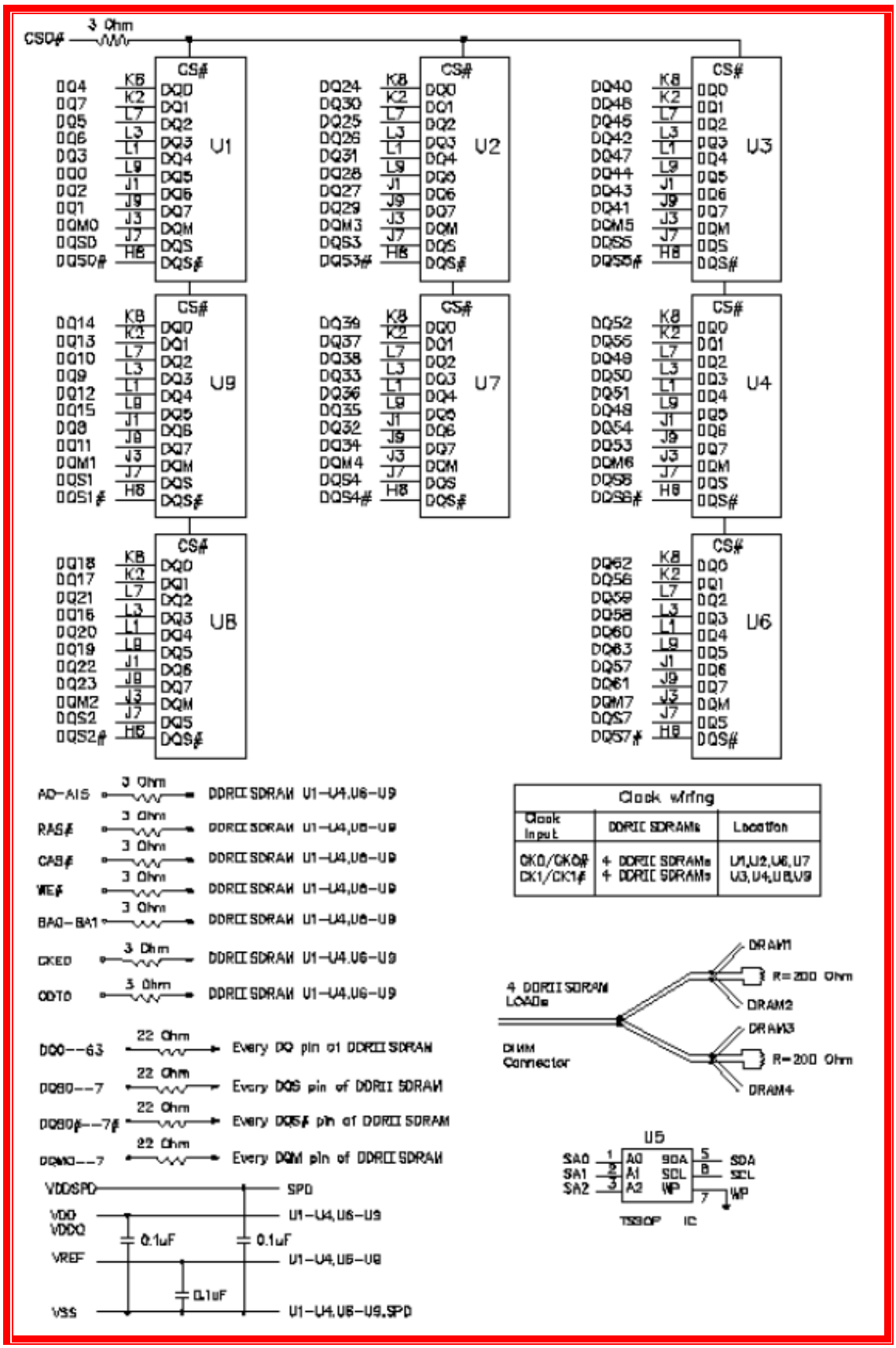
6. Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
CK0#, CK1#, CK2#	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CKE0#, CKE1#	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, RAS#, CAS#, WE# define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 – A9 A10/AP A11 – A13	(SSTL)	-	During a Bank Activate command cycle, A0-A14 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic

DQS0 – DQS8 DQS0# – DQS8#	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
SA0 – SA2	-	-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA	-	-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL	-	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply.

7. Function Block Diagram:

- (1 Rank, 128Mx8 DDR2 SODIMM)



Rev 1.0

May 2017

8. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to 2.3	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +2.3	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.5 to +2.3	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

9. AC & DC Operating Conditions

- AC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Value	Units	Notes
VREF	Input Reference Voltage	0.5 * VDDQ	V	1
VSWING (MAX)	Input signal maximum peak to peak swing	1.7	V	1
SLEW	Input signal minimum slew rate	0	V	2,3
VIH (AC)	Input High (Logic1) Voltage	VREF + 0.125	V	
VIL (AC)	Input Low (Logic0) Voltage	-0.3	V	

Note::

1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(AC) min for rising edges and the range from VREF to VIL(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(AC) to VIH(AC) on the positive transitions and VIH(AC) to VIL(AC) on the negative transitions.

- SDRAM DC operating Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature	-40 to 95	°C	1,2

Note:

1. Case temperature is measured at top and center side of any DRAMs.
2. t_{CASE} > 85°C ➔ t_{REFI} = 3.9 µs All DRAM specification only support 0°C < t_{CASE} < 85°C

- DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.7	1.9	V	1
V_{DDL}	Supply Voltage for DLL	1.7	1.9	V	1
V_{DDQ}	I/O Supply Voltage	1.7	1.9	V	1
V_{REF}	I/O Reference Voltage	0.49V_{DDQ}	0.51V_{DDQ}	V	1, 2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}+0.04	V	31
V_{IH} (DC)	Input High (Logic1) Voltage	V_{REF} + 0.125	V_{DDQ} + 0.3	V	1
V_{IL} (DC)	Input Low (Logic0) Voltage	-0.3	V_{REF} - 0.125	V	1

Note:

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} of transmitting device must track V_{REF} of receiving device.

10. Operating, Standby, and Refresh Currents

- 1GB SODIMM (1Rank, 128Mx8 DDR2 SDRAMs; V_{DDQ} = V_{DD} = 1.8V ± 0.1V)

Symbol	Parameter/Condition	PC2-5300	Unit
I_{DD0}	Operating Current: one bank; active/precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	480	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; tRC = tRC (MIN); CL=2.5; tCK = tCK (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle	560	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ VIL (MAX); tCK = tCK (MIN)	80	mA
I_{DD2N}	Idle Standby Current: CS ≥ VIH (MIN); all banks idle; CKE ≥ VIH (MIN); tCK = tCK (MIN); address and control inputs changing once per clock cycle	192	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; is HIGH; CKE is HIGH; t_{CK} = $t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	192	mA
I_{DD3PF}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	224	mA
I_{DD3PS}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	160	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ VIH (MIN); CKE ≥ VIH (MIN); tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	240	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; tCK = tCK (MIN)	920	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; tCK = tCK (MIN); IOUT = 0mA	880	mA
I_{DD5}	Auto-Refresh Current: tRC = tRFC (MIN)	1200	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	56	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; tRC = tRC (min); IOUT = 0mA.	1480	mA

11. AC Timing Specifications

(V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	PC2-5300		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.45	+0.45	ns
tDQSCK	DQS output access time from CK/CK#	-0.40	+0.40	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	tCH or tCL	-	tCK
tCK	Clock Cycle Time	3	8	ns
tDS	DQ and DM input setup time(differential data strobe)	0.1	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.175	-	ns
tIPW	Input pulse width	0.6	-	tCK
tDIPW	DQ and DM input pulse width (each input)	0.35	-	tCK
tHZ	Data-out high-impedance time from CK/XK	-	tACmax	ns
tLZ(DQS)	DQS low-impedance time from CK/XK	tACmin	tACmax	ns
tLZ(DQ)	DQ low-impedance time from CK/XK	$2t_{AC}$ min	t_{AC} max	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.24	ns
tQHS	Data hold Skew Factor	-	0.34	ns
tQH	Data output hold time from DQS	tHP - tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	-0.25	+0.25	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.2	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.2	-	tCK
tMRD	Mode register set command cycle time	2	-	tCK

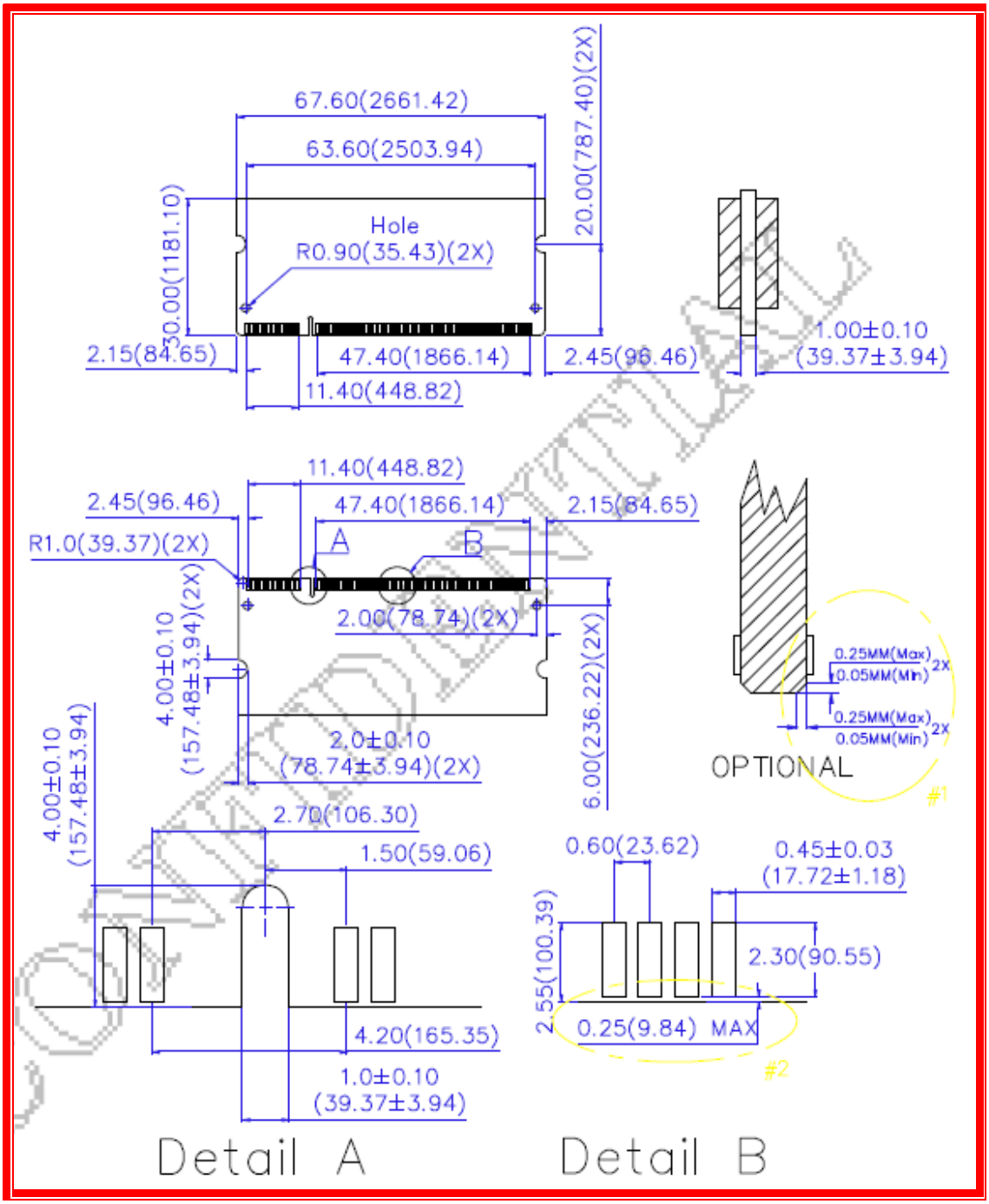
tWPST	Write postamble	0.40	0.60	tCK
tWPRE	Write preamble	0.35	-	tCK
tIH	Address and control input hold time	275	-	Ps
tIS	Address and control input setup time	200	-	Ps
tRPRE	Read preamble	0.90	1.10	tCK
tRPST	Read postamble	0.40	0.60	tCK
tRRD	Active bank A to Active bank B command	7.5	-	Ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	tIS + tCK + tIH	-	Ns
tREFI	Average Periodic Refresh Interval ($85ºC < T_{CASE} \leq 95ºC$)	3.9		Ms
	Average Periodic Refresh Interval ($0ºC \leq T_{CASE} \leq 85ºC$)	7.8		Ms
tOIT	OCD drive mode output delay	0	12	Ns
tCCD	CAS# to CAS# delay	2		tCK
tWR	Write recovery time without Auto-Precharge	15	-	Ns
WR	Write recovery time with Auto-Precharge	tWR/tCK	-	tCK
tDAL	Auto precharge write recovery + precharge time	WR+tRP	-	tCK
tWTR	Internal write to read command delay	7.5	-	Ns
tRTP	Internal read to precharge command delay	7.5		Ns
tXSNR	Exit self refresh to a Non-read command	tRFC+10		Ns
tXSRD	Exit self refresh to a Read command	200		tCK
tXP	Exit precharge power down to any Non- read command	2	-	tCK
tXARD	Exit active power down to read command	2	-	tCK
tXARDS	Exit active power down to read command	7-AL		tCK
tCKE	CKE minimum pulse width	3		tCK

Symbol	Parameter	PC2-5300		Unit
		Min.	Max.	
t_{AOND}	ODT turn-on delay	2	2	t_{CK}
t_{AON}	ODT turn-on	t_{AC} (min)	t_{AC} (max) +0.7	Ns
t_{AONPD}	ODT turn-on (Power down mode)	t_{AC} (min) +2	2t_{CK} + t_{AC}(max) +1	Ns
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}
t_{AOF}	ODT turn-off	t_{AC}(min)	t_{AC}(max) +0.6	Ns
t_{AOFPD}	ODT turn-off (Power down mode)	t_{AC} (min)+2	2.5t_{CK} + t_{AC}(max) +1	Ns
t_{ANPD}	ODT to power down entry latency	3		t_{CK}
t_{AXPD}	ODT power down exit latency	8		t_{CK}

12. Speed Grade Definition

Symbol	Parameter	PC2-5300		Unit
		Min	Max	
t_{RAS}	Row Active Time	45	70,000	ns
t_{RC}	Row Cycle Time	55	-	ns
t_{RCD}	RAS to CAS delay	15	-	ns
t_{RP}	Row Precharge Time	15	-	ns

13. Physical Dimension



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

14. RoHS Declaration

innodisk

宜鼎國際股份有限公司

Innodisk Corporation

Page 1/1

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2016 / 08 / 04

Revision Log

Rev	Date	Modification
0.1	9th May 2017	Preliminary Edition
1.0	9th May 2017	Official Release